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A LOW NOISE Ga-As FET AMPLIFIER AT 1.4 GHz

Low Noise Ga-As FET amplifier at 1.4 GHz

Contents

I. Introduction and Perspective:

This report describes the design and construction of both bipolar and Ga-As fet amplifiers around 1.4 GHz, with the aim of gaining acquaintance with high frequency devices and low noise design techniques. The end use of the amplifiers is in the first I.F. stage of a millimeter wave radio astronomical receiver currently under construction at RRI

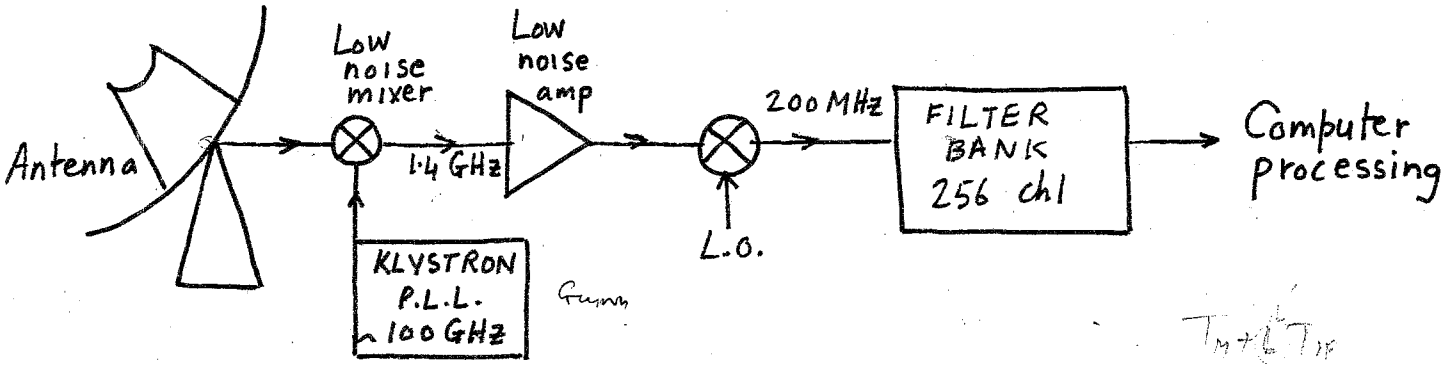


FIG 1.1 MM WAVE RECEIVER SYSTEM, 70-140 GHz

1.1 Amplifier Requirements:

Sources in radio astronomy can be either continuous in frequency (thermal, synchrotron mechanisms) or discrete. Some lines of interest are given:

molecule	freq. (GHz)	molecule	freq. (GHz)
Methyl Alcohol CH_3OH	84.52	Carbon monoxide CO	110.2, 115.3
Carbonyl Sulphide OCS	85.13, 97.30	Cyanide ion CN	130.3
Hydrogen Cyanide HCN	88.63	Silicon monoxide SiO	130.3

These are seen mainly in emission.

For a line source at frequency f_o = 100 GHz, (3 mm λ) moving at velocity v, typically 100 km/sec, the doppler bandwidth $\Delta f = \left(\frac{v}{c} \cdot f_o\right) = 100$ MHz. Signal energies are extremely low, eg: -140 dBm/ K in a 1 MHz band for a thermal emitter. Given an integration time τ on a system of noise temperature T_s, the minimum detectable signal $T_{min} \propto \frac{T_s}{\sqrt{\tau}}$. Cryogenic masers, paramps or tunnel diode amplifiers are used to minimize T_s. A front end consisting of a low noise (diode) mixer, followed by a cooled Ga-As fet amplifier * at the I.F. is a potential replacement which offers simplicity (no pump source is needed), lower cost, and relativity large bandwidth. T_s is then dependent on the IF noise and the mixer conversion loss. Problems with the FET include (i) high input Q , preventing a broadband characteristic (ii) poor stability and (iii) difficulty in obtaining simultaneous noise and power match.

1.2 Summary of report:

Principles of operation of the MESFET are presented in chapter 2, along with a technique (FUKUI, Ref 2 and 3) of determining the microwave noise figure from measured dc parameters. Using the scattering matrix approach summarized in Appendix A, the design of amplifiers is described in chapter 3. The bipolar amplifier, a trial attempt, gave 11 dB gain with 3.7 dB noise figure at 1.4 GHz, while the FET amplifier had a gain of 17 dB and noise figure 1.3 dB (100 °K) at 1.35 GHz and room temperature (300 ° K).

* Ref 4, 8, 9.

2. Ga-As- MESFET basics:

2.1 Device physics and circuit model.

Figure 2.1 depicts the metal-semiconductor fet in outline

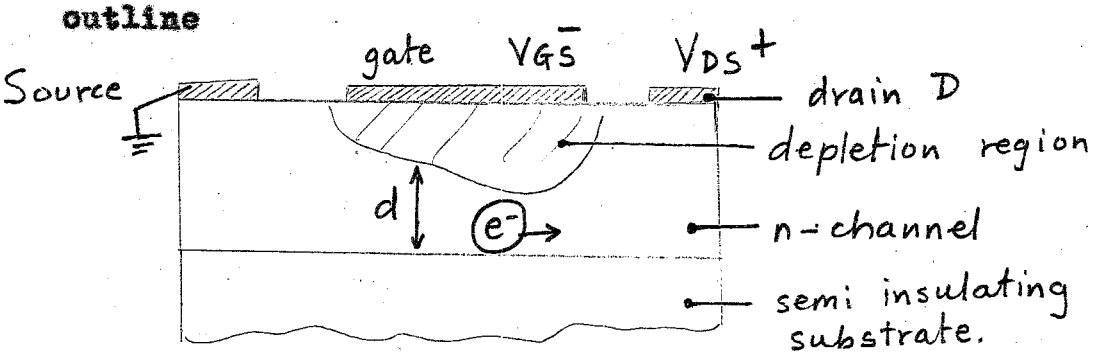


FIG 2.1 MESFET STRUCTURE

S = Source, D = drain, G = gate. Aluminium metallization on n-type Ga-As.

d = conduction channel depth

Operation:

Majority carriers (e-) flow from S to D in the n type channel. A negative V_{GS} causes a depletion layer below the gate electrode. The gate-channel interface is a Schottky barrier with more reverse bias across it at the positive D end than at the S end, so the depletion is deeper at the drain, and d is less.

Drain current $I_{DS} \propto n(x).\ V(x).\ d(x)$

where n = carrier concentration

V = carrier drift velocity

x = Coordinate from S to D

For low V_{DS}, the channel electric field E is less than E_p (fig 2) and n(x) is just the equilibrium donor concentration, N_D.

Fig 2

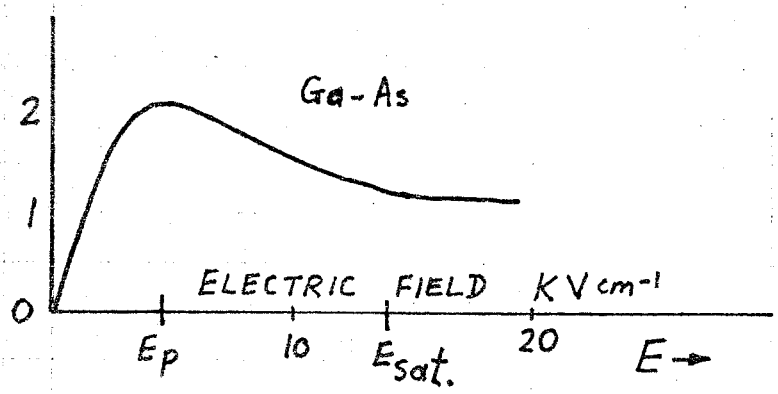


Fig 3

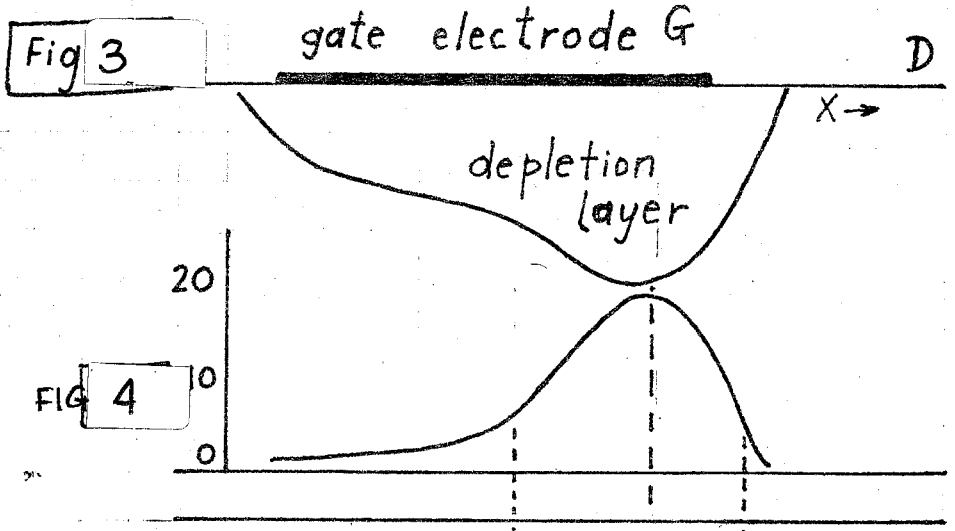


FIG 4

FIG 5

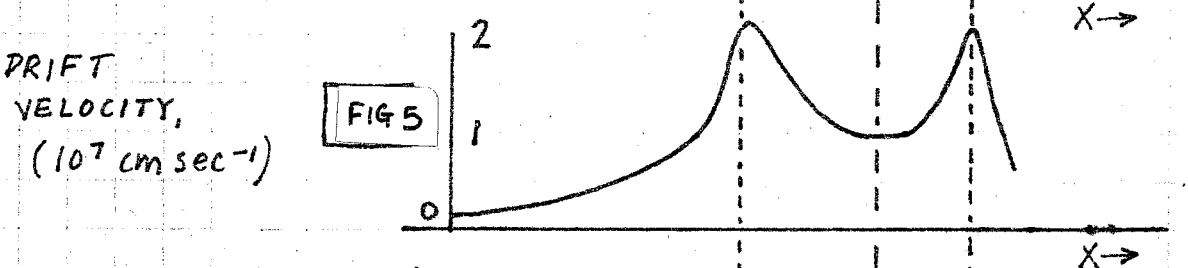
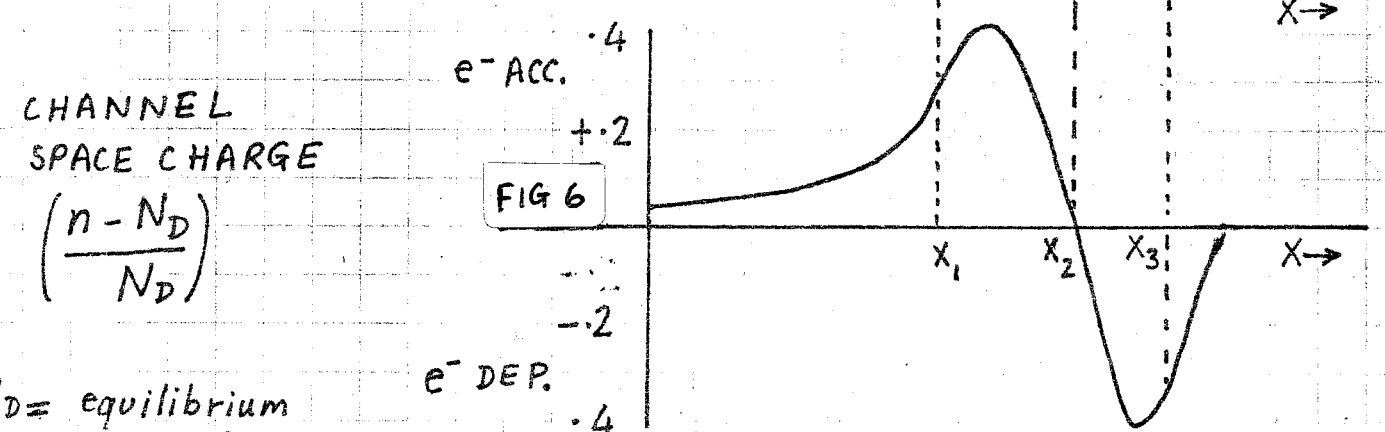


FIG 6



N_D = equilibrium donor Conc.

Since d is smaller near the drain, $\mathcal{V}$ is higher at the drain than at the source end, to maintain continuity of the current I_{DS}. If V_{DS} is now increased, the reverse bias across the junction increases further at the drain end, so d decreases and the length of the highly depleted region expands. The channel electric field E is now higher than E_p in the region x_1 to x_3 (fig.5). Hence, according to the E-$\mathcal{V}$ plot in fig 2, the $\mathcal{V}$ should reach $\mathcal{V}_p$ at x and decrease in the region x_1 to x_2, where it approaches saturation value $\mathcal{V}_s$ where E is highest.(fig. 4). In this region, x_1 to x_2, both $\mathcal{V}$ and d are decreasing so now n must increase to preserve I_{DS}, ie., a heavy space change accumulation occurs in the x_1 x_2 region under the gate. The reverse process is taking place from x_2 to x_3, and an electron depletion region results (fig 6).

For short gate length devices, ($L < 3\mu$) the behaviour of electrons is complicated since E is more than E_p over an appreciable fraction of the length. The charge transport mechanism is a non-equilibrium one, with slow electrons from regions where $E < E_p$ suddenly increasing their velocities before relaxing towards saturation. Since a larger number of electrons are injected into the velocity saturated region with increasing V_{DS}, a finite drain source resistance results even after 'saturation'. Measured characteristics are displayed in fig 7.

A lumped element small signal model for the MESFET operating in the current saturation region is shown in fig 8, and the physical origin of the circuit is indicated in fig 9.

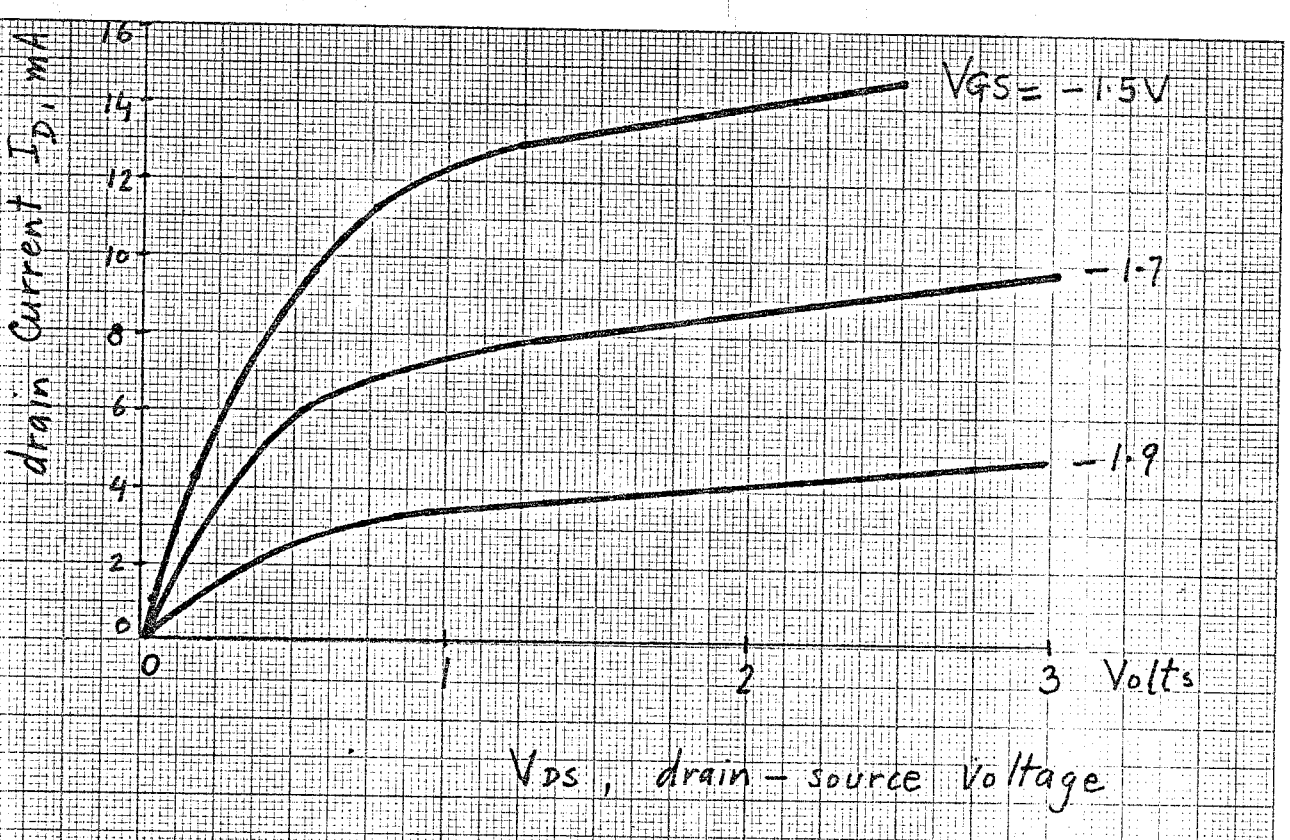
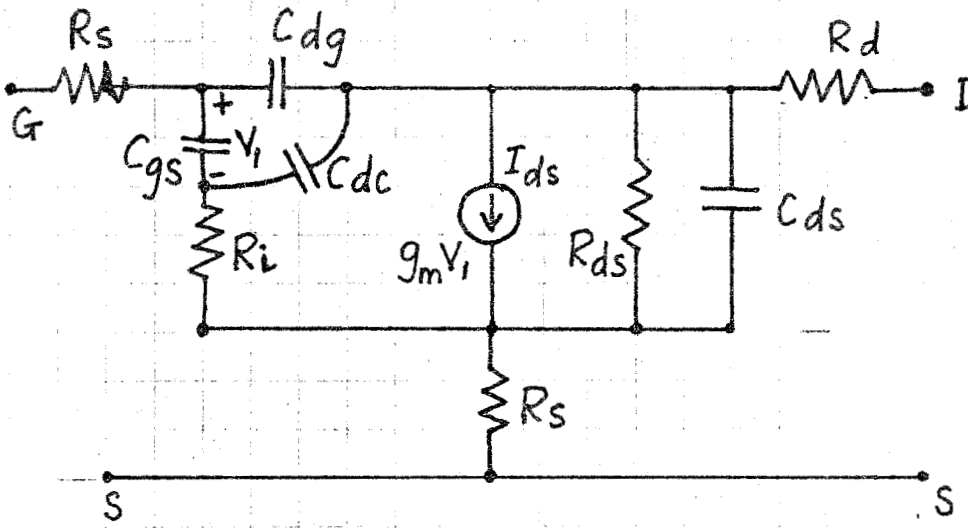
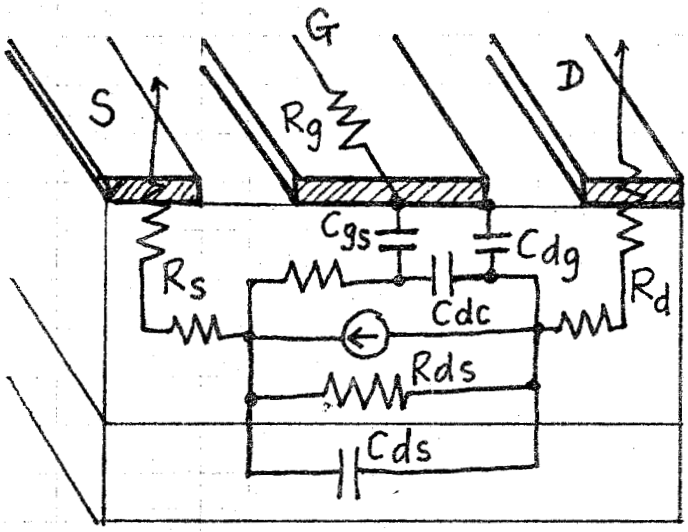


FIG 7



LUMPED ELEMENT MODEL, VALID TO 12 GHz

FIG 8



ORIGIN OF CIRCUIT ELEMENTS

(TYPICAL VALUES)

FIG 9

$C_{gs}+C_{gd}$ Total gate-channel capacitance (·35 pF)

C_{dc} dipole layer cap. (·5 pF) C_{ds} substrate cap (·05 pF)

R_i, R_{ds} channel resistances (2 Ω, 400 Ω)

R_g, R_d, R_s Contact and spreading resistances (~5 Ω each)

f_T Unity current gain frequency $\approx \frac{1}{2\pi} \frac{g_m}{C_{gs}}$ (13 GHz)

2.2 Geometric and material parameters for microwave performance.

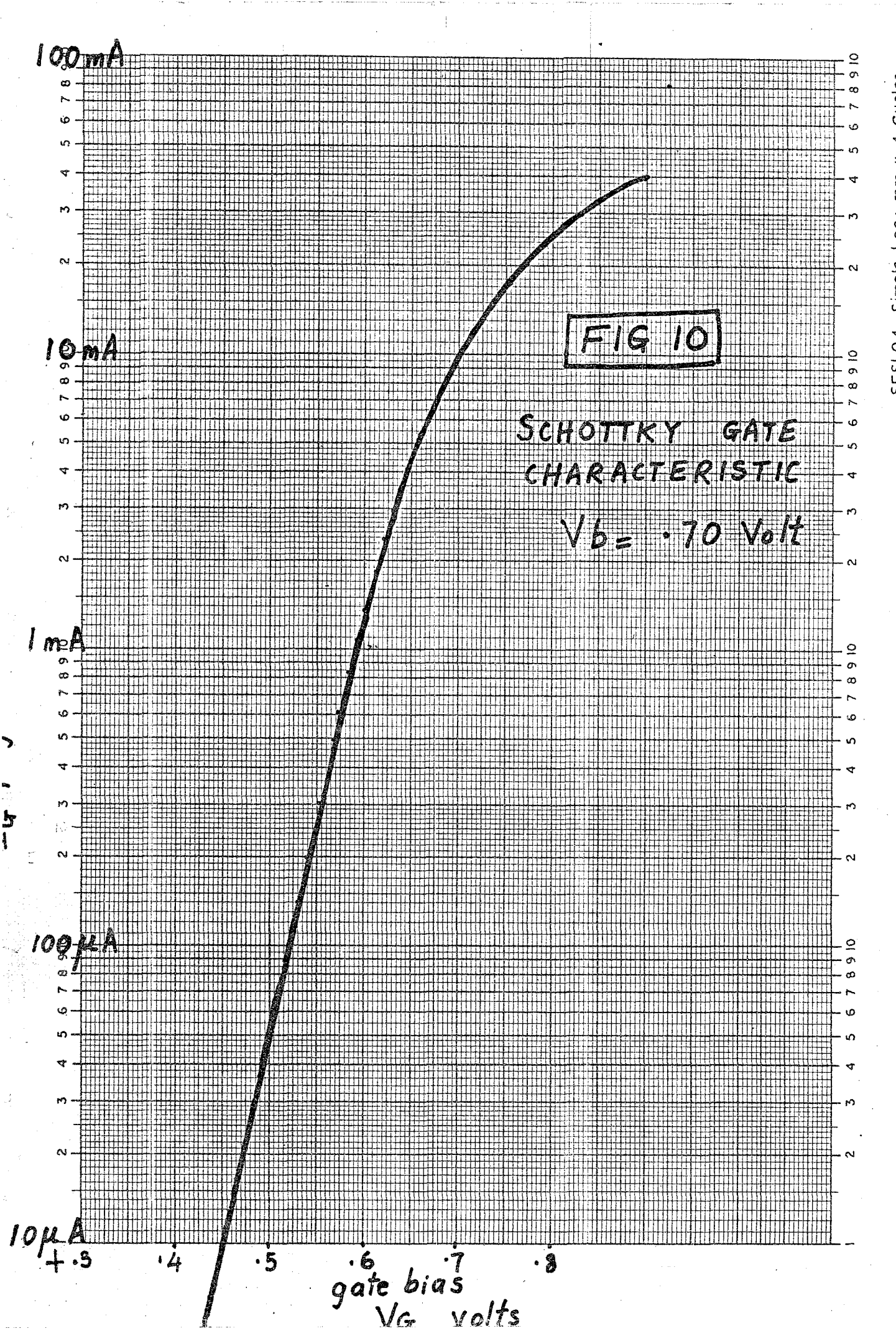
Parameter	Ga As	Silicon
Low field mobility	Electrons : 8800 holes : 400 $cm^2/V.sec$	1350 $cm^2/V.sec$
max.drift velocity (electrons)	2.2×10^7 cm/sec	1×10^7 cm/sec
Saturated drift velocity	1×10^7 cm/sec	1×10^7 cm/sec

n type Ga As is thus the obvious choice for highest frequency performance.

Mesfets are planar devices with an epitoxial conducting layer less than a micron thick on a thicker semi-insulating GaAs substrate. Parasitic resistances and capacitances are decreased and trans conductance g_m is increased by reducing gate length and hence the transit time.Gain bandwidth $f_T \propto L^{-1}$. Currently L is under 1 micron and f_T above 10 GHz.

d.C. parameters and measurements:

Empirical formulae have been derived (ref.2,3) for the prediction of the microwave noise performance from measured dc values of active and parasitic mesfet parameters. Measurements on the schottky gate allow determination of the barrier voltage V_b and the parasitics Rg, Rd, Rs (fig 8 and 9). These, together with the pinch off voltage of the channel, V_p the g_m and L are used to calculate expected noise figure.


100 mA
10 mA
1 mA
100 μA
10 μA
+.3
.4
.5
.6
.7
.8
gate bias
VG volts
FIG 10
SCHOTTKY GATE
CHARACTERISTIC
Vb = .70 Volt
SESLO4 - Simple Log: mm x 4 Cycles

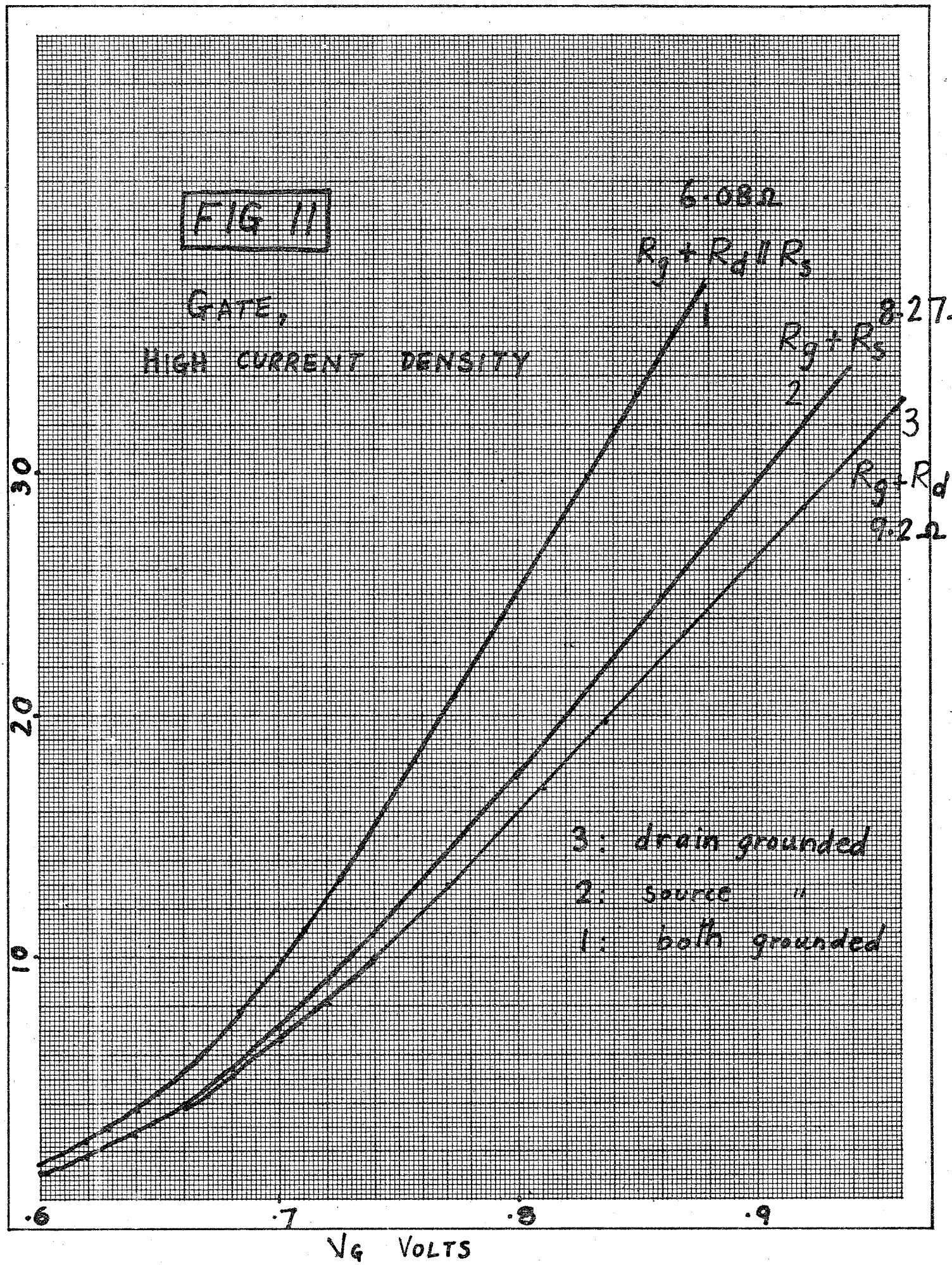
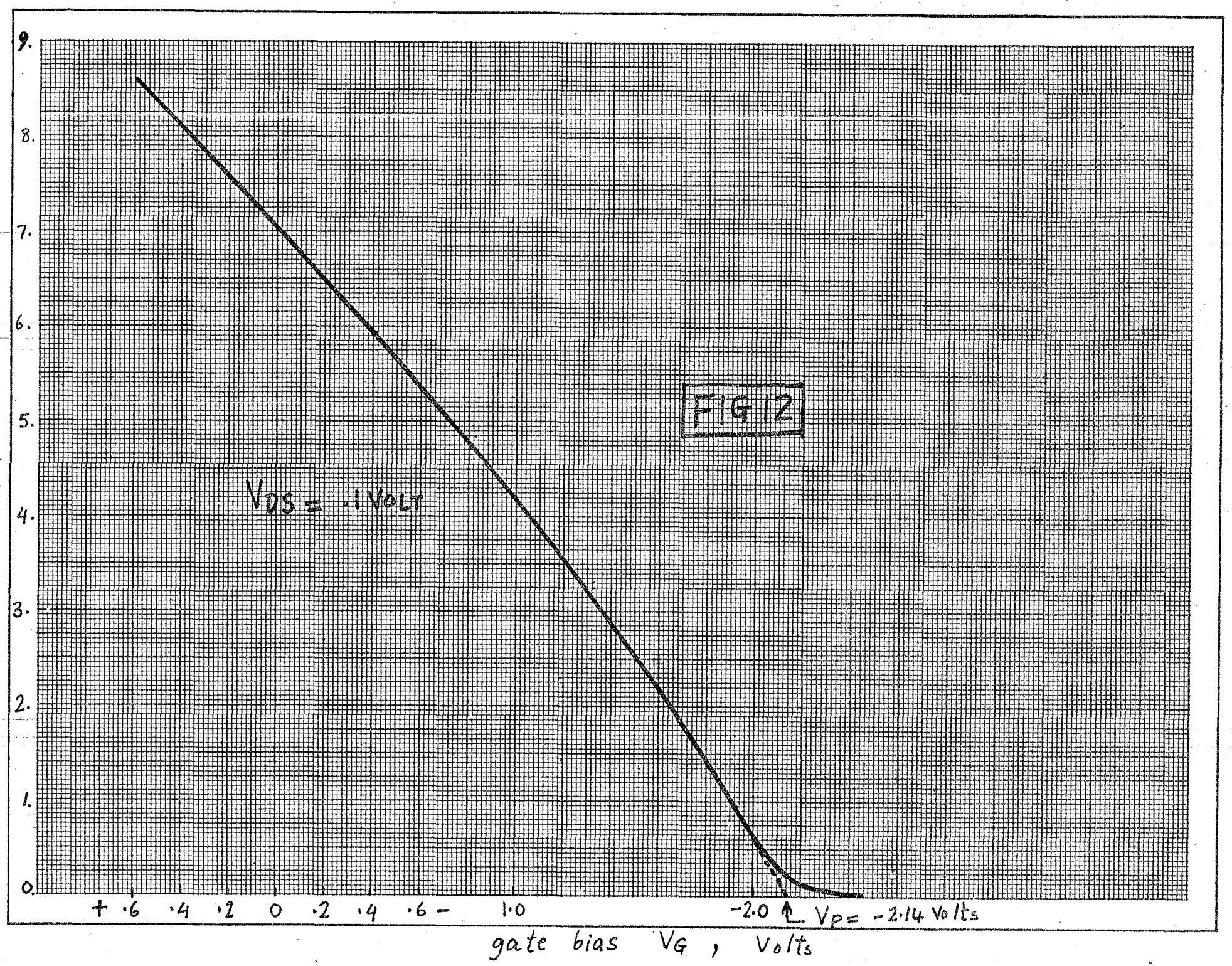


FIG 11
GATE,
HIGH CURRENT DENSITY
6.08Ω
$R_g + R_d \| R_s$
1
8.27Ω
$R_g + R_s$
2
3
$R_g + R_d$
9.22Ω
3: drain grounded
2: source "
1: both grounded
30
20
10
I_G, mA
.6
.7
.8
.9
V_G VOLTS


9.
8.
7.
6.
5.
4.
3.
2.
1.
0.
drain current I_D, mA
V_{DS} = .1 VOLT
FIG 2
+ .6 .4 .2 0 .2 .4 .6 – 1.0 -2.0
V_P = -2.14 Volts
gate bias V_G, Volts

(a) Schottky gate characteristics:

Conditions	Parameter determined
(i) low current exponential region, drain and source grounded	V_b, barrier voltage
(ii) high current density region gate current limited only by parasitic resistances (see fig 8)	Slope of I-V plot (fig 11) gives:
Source, drain both grounded	$R_g + (R_d \parallel R_s)$
Source grounded, drain open	$R_g + R_s$
Drain grounded, source open	$R_g + R_d$

(b) $I_D - V_{GS}$ plot, with V_{DS} fixed in linear region, (see fig 12).

Conditions	Parameter
V_{DS} = .1 volt Channel resistance varies linearly with V_{GS}	(i) V_p channel pinch off voltage. (ii) $R_d + R_s$ total channel parasitic resistance (i) (ii) found as described below.

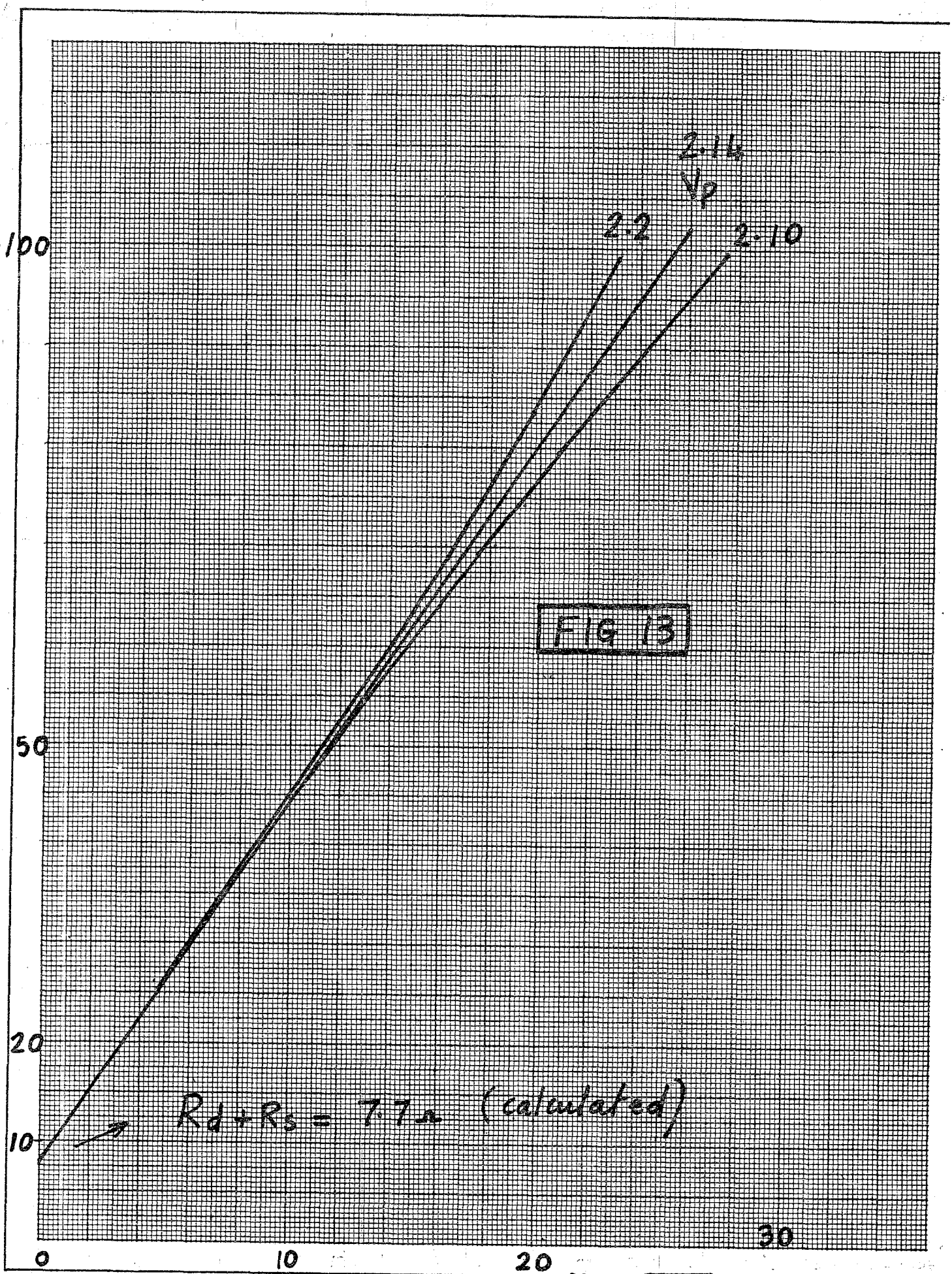
(i) An initial value of V_p is determined from fig 12 by extrapolating the linear part of the curve to 0 drain current

(ii) I_{DS} in fig 12 is used to calculate the total drain-source resistance, $R_{ds} = \frac{V_{DS}}{I_{DS}}$

(iii) Using the initial estimate of V_p, R_{ds} is plotted against

$$X = \left(1 - \sqrt{\frac{V_b - V_{gs}}{V_b + V_p}} \right)^{-1}.$$

If V_p as found in (i) is not exact, this plot will deviate from a straight line (see fig 13). The final va lue of V_p



$$X = \left[1 - \sqrt{\frac{V_b - V_{gs}}{V_b - V_P}}\right]^{-1}$$

is the one which gives a linear plot.

(iv) If the slope of the line in (iii) is R_o, then R_o X represents the active channel component of the total drain-source resistance at that value of X (ie. at that value of V_{gs}). At X = 0 therefore, the active component is 0 and the Y-intercept is the remnant parasitic, Rd + R_s.

The above analysis yields the foll. results

Rd = 4.3

Rg = 4.2

R_s = 3.4

V_p = -2.14 volts

$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$, measured = 27 mmho

$(g_m = \frac{g_m'}{1+g_m' R_s})$

g_m' = actual transconductance

= 30 mmho

Using the empirical relation for mimimum noise figure,

$$F_o = 1 + K \cdot L \cdot f \sqrt{g_m'(R_g+R_s)}$$

where f = frequency of operation, GHz.

K = fitting constant = .3

L = effective gate length, = physical gate metalligation length for planar devices.

g_m' in mhos

Results

F_o (1.4 GHz) = 0.80 dB , F_o (1.9 GHz) = 1.05 dB

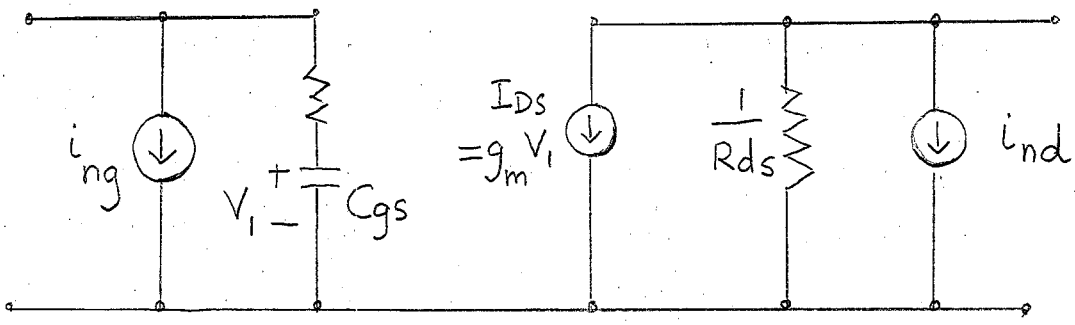
data sheet gives F_o (1.9) = 0.9 dB

2.3 Fet noise theory:

Dominant sources of FET noise include the following:
1. Thermal noise: Charge carriers in each volume element of the channel are in thermal equilibrium with the lattice at $T > 0^{\circ}K$ and generate a noise voltage which modulates the depletion layer width, and appears as an amplified noise at the drain. Parasitic resistances also generate thermal noise.
2. Hot electron noise: In short gate length devices, especially in Ga As, the current transport mechanism is complex. Transit time is shortened by the velocity peaking effect (see page 4) and e^- do not have time to relax to thermal equilibrium with the lattice. The electrons however, are at equilibrium among themselves, at a higher noise temperature.
3. Intervalley scattering noise: In ga as, electrons in the low energy conduction band have high mobility. As the electric field in the channel increases beyond E_p, e^- transfer to higher energy satellite conduction bands where their effective mass is much larger (fig 2). Random transfer of charge carriers between 2 conduction states leads to current fluctuations which further increase the noise temperature.
4. High field diffusion noise: Conduction is non-ohmic in the region of the channel where electrons have acquired saturation velcoity and changes in the electric field do not affect the drift velocity. Noise current in this region has a mean square value dependent on the high field diffusion coefficient of the semiconductor, and is linearly preportional to the drain current.

Between ≈ 20 mHz and 3 GHz, there are, in addition less well understood sources which contribute to the overall noise temperature.

Simplified noise model of intrinsic mesfet:



1. i_{nd} = channel noise in drain-source region in band Δf

   $\overline{i^2}_{nd} = (4kT_o \Delta f g_m) P$, P depends on device geometry and bias. For 0 drain voltage, $\overline{i^2}_{nd} = (4kTG_{ds} \cdot \Delta f)$ is the thermal noise in the drain conductance G_{ds}. P is then $\frac{G_{ds}}{g_m}$

   T_o = channel temp.

2. Noise voltage in channel varies the depletion layer width and hence the depletion charge. This induces a charge fluctuation at the gate described by i_{ng}

$$\overline{i^2}_{ng} = 4kT_o \Delta f \cdot \frac{w^2 C_{gs}^2}{g_m} \cdot R.$$

R depends on geometry and bias, Cgs is the gate source capacitor causing the coupling of the noise sources in the drain to the gate. i_{ng} and i_{nd} are caused by same noise voltages in the channel. They are therefore correlated and the correlation coeff = jc = $(\overline{i^*_{ng} \cdot i_{nd}}) / (\overline{i^2}_{ng} \cdot \overline{i^2}_{nd})^{\frac{1}{2}}$ is purely imaginary due to the capacitive coupling.

Low temperature performance: Fet's being majority carrier devices, can operate at much lower temperature than bipolars. For S_i, e^- are *frozen* out of the conduction band at 125° K. In Ga as the donor levels are just 3-6 mV below the conduction band and no freeze out occurs. Output thermal noise $\propto T_A/gm$ where T_A is the ambient temperature. At reduced temperature g_m increases, since carrier mobility increases due to reduced scattering. Noise due to parasitic resistances also cools with temperature.

3. Amplifier design with potentially unstable active elements:

Both bipolar and fet transistors can be potentially unstable over part of their usable frequency range. To get familiar with high frequency design techniques using scattering parameters, and to understand the problems in working with unstable devices, the design of a bipolar transister amplifier was undertaken before attempting to build the fet amplifier.

3.1 Bipolar Transistor amplifier design:

requirements : Centre frequency : 1400 MHz
3dB bandwidth : 200 MHz
gain : maximum consistent with minimum noise figure.

Transistor used : HP - 35821 E (see data sheet p10A)
Measurement of the transistor scattering parameters not being accurately possible with available equipment at 1.4 GHz the manufacturer's data sheet has to be relied upon. However parameters ~~these~~ are given for a bias corresponding to V_{CE} and I_C for gain, not those for minimum noise. The design is carried out with available parameters and final adjustments

P. 10A

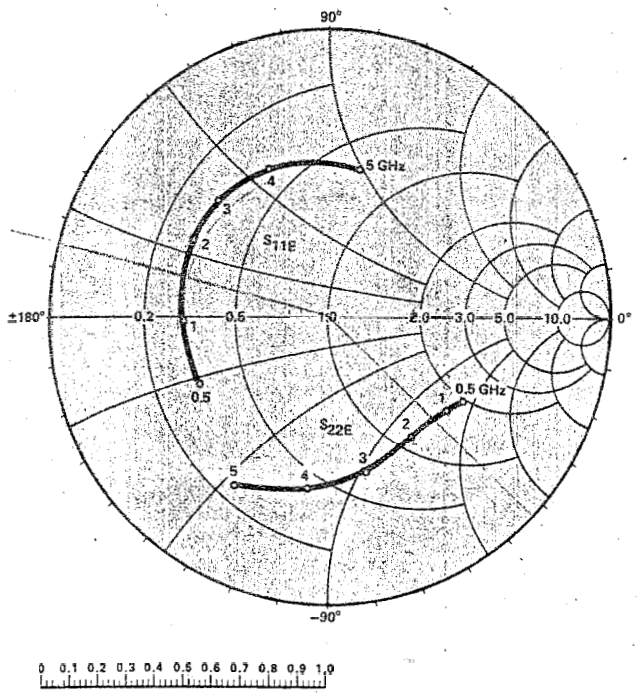


Figure 4. Typical S_{11} and S_{22} vs. Frequency for the 35821E for V_{CE} = 15V, I_C = 15 mA.

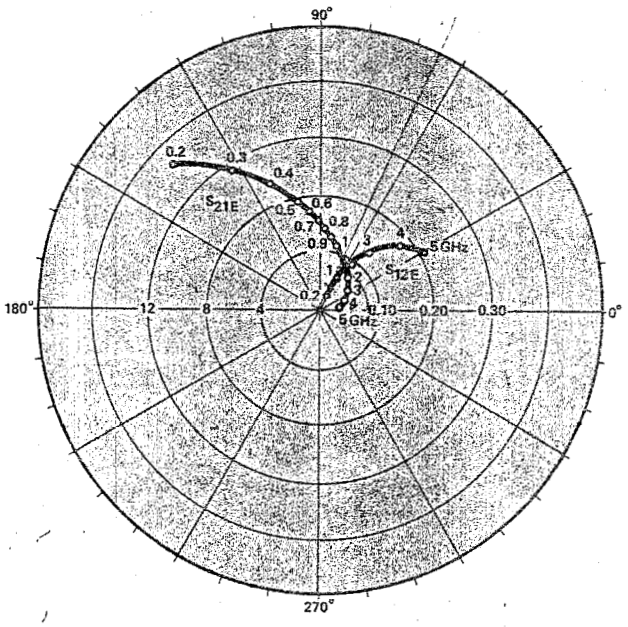
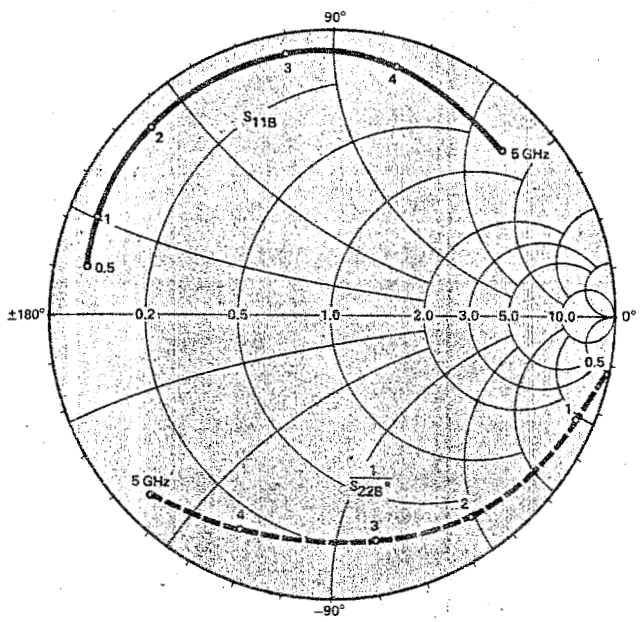


Figure 5. Typical S_{21} and S_{12} vs. Frequency for the 35821E for V_{CE} = 15V, I_C = 15 mA.

COMMON EMITTER S-PARAMETERS



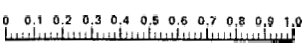


Figure 6. Typical S_{11} and S_{22} vs. Frequency for the 35821B for V_{CB} = 15V, I_C = 15 mA.

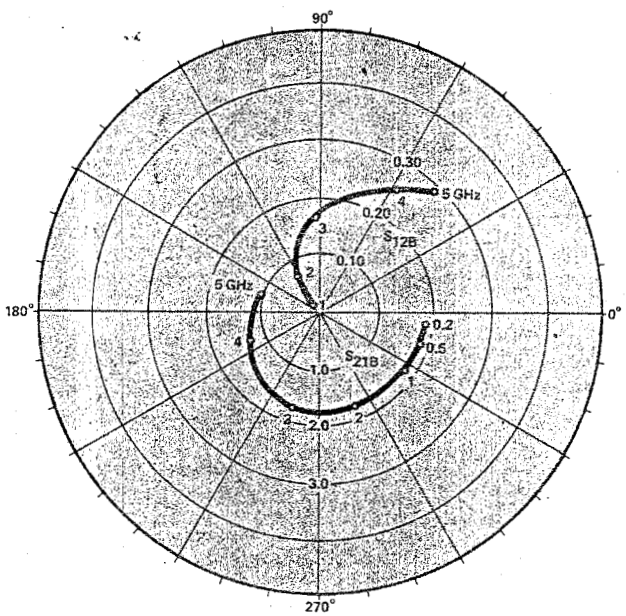


Figure 7. Typical S_{21} and S_{12} vs. Frequency for the 35821B for V_{CB} = 15V, I_C = 15 mA.

made on the bias circuit to achieve lowest noise.

Scattering parameters at 1.0 GHz $= \begin{bmatrix} .52\angle 180^\circ & .06\angle 63^\circ \\ 4.1\angle 68^\circ & .53\angle -35^\circ \end{bmatrix}$

1.4 GHz $= \begin{bmatrix} .5\angle 165^\circ & .08\angle 60^\circ \\ 3.2\angle 65^\circ & .52\angle 43^\circ \end{bmatrix}$

2.0 GHz $= \begin{bmatrix} .52\angle 152^\circ & .10\angle 60^\circ \\ 2.3\angle 70^\circ & .52\angle -55^\circ \end{bmatrix}$

from the scattering parameters, the following quantities are calculated (for definition and formulas, see appendix A)

a. K, stability factor $K > 1 \Rightarrow$ absolute stability

$K < 1 \Rightarrow$ potential instability, dependent on load and source.

1 GHz : K = .92, } G_{max} undefined since conjugatety matching
1.4 & K = .90 } input and output causes instability.

2.0 : K = 1.07 G_{max} 11.9 dB, conjugate match possible.

b. Stability circles, boundaries between stable and unstable terminations on ~~Smith chart~~ Smith Chart for both input and output.

(C_i, C_o centres, ρ_i, ρ_o radii)

1.4 GHz : $C_o = 1.9\angle 42^\circ$ $C_i = 1.96\angle 166^\circ$

$o = .95$ $i = .98$

1.0 GHz $C_o = 1.85\angle 39^\circ$ $C_i = 1.98\angle 171$

$= .90$ $i = 1.02$

2.0 GHz since K > 1 stability circles lie entirely outside the smith chart, ie no passive impedance causes instability.

c. Constant gain circles, loci of load impedances giving constant gain, are calculated at 1.4 GHz.

a, b, c are all plotted on the smith chart No.1.

A load impedance lying well in the stable region is chosen giving about 14 dB gain and a matching network found to

Chhenna Corporation, Delhi-6.

NAME V. Dhawan	TITLE HP-35821-E AMPLIFIER	DWG. NO.
		DATE 1 april 1980

IMPEDANCE OR ADMITTANCE COORDINATES

OUTPUT STABILITY centre 1.9 rad. 0.95.

STABLE

OUTPUT 1.4 GHz

UNSTABLE

42°

16

15

14

13

12

11 dB

10

Γ_L

CONSTANT GAIN (dB)

Γ_S

INPUT STABILITY CIRCLE centre 1.9 ∠66° rad = 0.95

STABLE

INPUT 1.4 GHz

UNSTABLE

RESISTANCE COMPONENT $\left(\frac{R}{Z_0}\right)$, OR CONDUCTANCE COMPONENT $\left(\frac{G}{Y_0}\right)$

INDUCTIVE REACTANCE COMPONENT $\left(\frac{+jX}{Z_0}\right)$, OR CAPACITIVE SUSCEPTANCE COMPONENT $\left(\frac{+jB}{Y_0}\right)$

CAPACITIVE REACTANCE COMPONENT $\left(\frac{-jX}{Z_0}\right)$, OR INDUCTIVE SUSCEPTANCE COMPONENT $\left(\frac{-jB}{Y_0}\right)$

WAVELENGTHS TOWARD GENERATOR

WAVELENGTHS TOWARD LOAD

ANGLE OF REFLECTION COEFFICIENT IN DEGREES

CHART 1

RADIALLY SCALED PARAMETERS

STANDING WAVE VOL. RATIO

TRANSM. LOSS IN DB STEPS

LOSS COEFF.

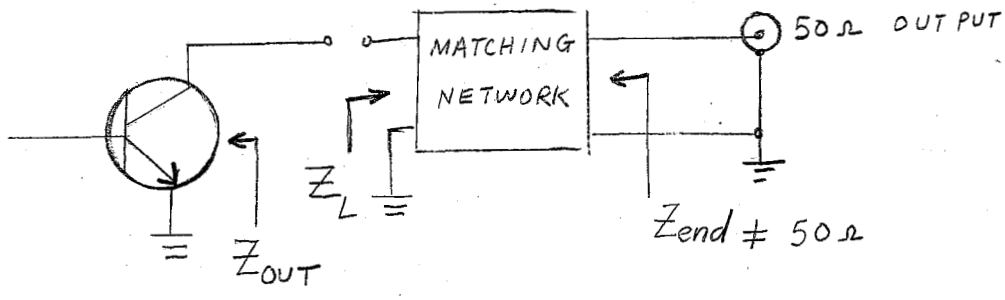
TOWARD GENERATOR →

← TOWARD LOAD

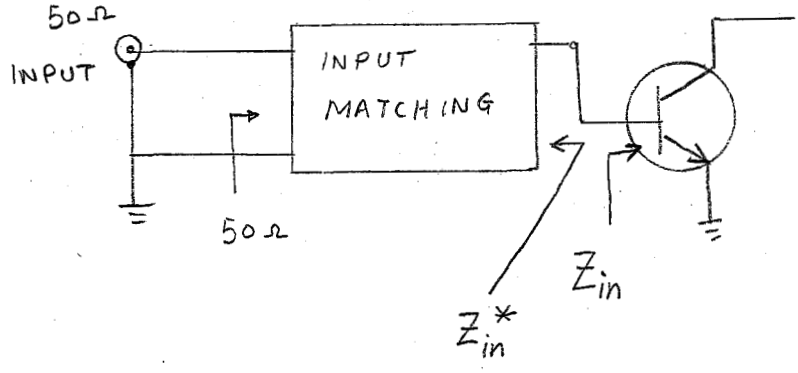
REFLECTION COEFF. VOL. PWR. RETN/REFL. LOSS IN DB

CENTER

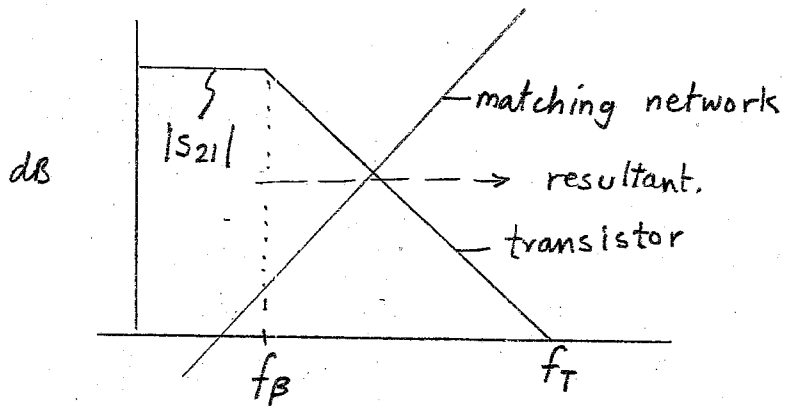
transform the 50Ω load to present this chosen impedance at the transistor output.



Because conjugate matching has been avoided, the impedance Z_{end} at the matching network output is not 50Ω and so gives rise to an output VSWR. Choice of a load closer to the unstable boundary (ie closer to the conjugately matched but unstable condition) gives higher gain, lower VSWR but is relatively less stable and more sensitive to variations in S parameters. A compromise is made with acceptable VSWR. (calculated value : SWR = 3, R.L. = 6dB). The transistor at these frequencies is non-unilateral, so the choice of load affects the input impedance. With the load chosen, the Z_{in} is calculated and a matching network synthesized to transform the 50Ω source to Z_{in}^*



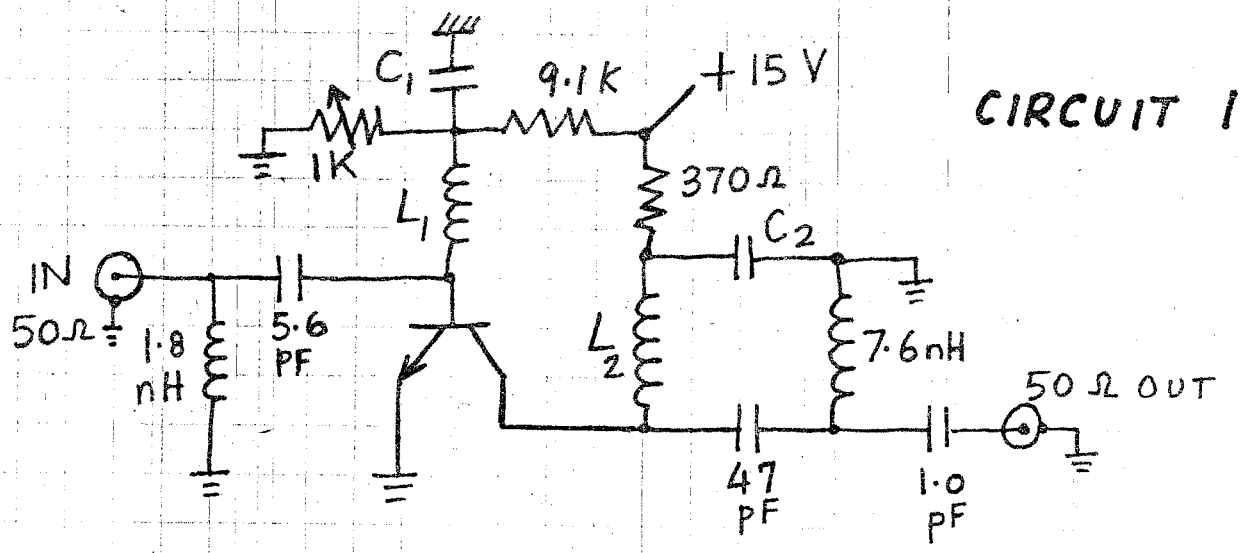
In the neighbourhood of 1.4 GHz, the transistor gain is falling at 6 dB/octave and reaches 0 dB at a gain bandwidth f_T = 6GHz. To improve gain flatness over a broadband, the matching networks should mismatch the transistor and decrease the gain at low freqneicies while leaving it intact at higher freqnencies, ie., the matching elements should be high pass to compensate for the transistor low pass characteristic



The circuit diagram and layout are shown in CIRCUIT-1. Dual copperclad Teflon-glass fibre dielectric is used for the circuit board, with ε_r = 2.5. The bias circuit is on the reverse of the same card and must be properly bypassed, and grounding carefully done to prevent high frequency resonant lengths and consequent oscillation. All elements except the input/output microstrip lines are lumped.

Capacitors : fixed values : ceramic chip capacitors
variables : screw tunable, polyester dielectric

Inductances : Short lengths or few turns of tinned copper wire, .6mm dia. At these frequencies, inductance goes as the length of the wire, 10 nH/cm, rather than the number of turns. (Wires are coiled to save space) lengths of about $\lambda/4$ ($\approx$ 5cm) act as parallel resonant chokes for biassing.



CIRCUIT 1

Circuit fabricated on double-Cu clad low loss teflon-glass fibre dielectric ($\epsilon_r = 2.5$)

INPUT/OUTPUT : SMA connectors feeding 50Ω (4.5 mm Width) microstrip line.

5.6 pF, 1.0 pF Johansen Variable capacitors

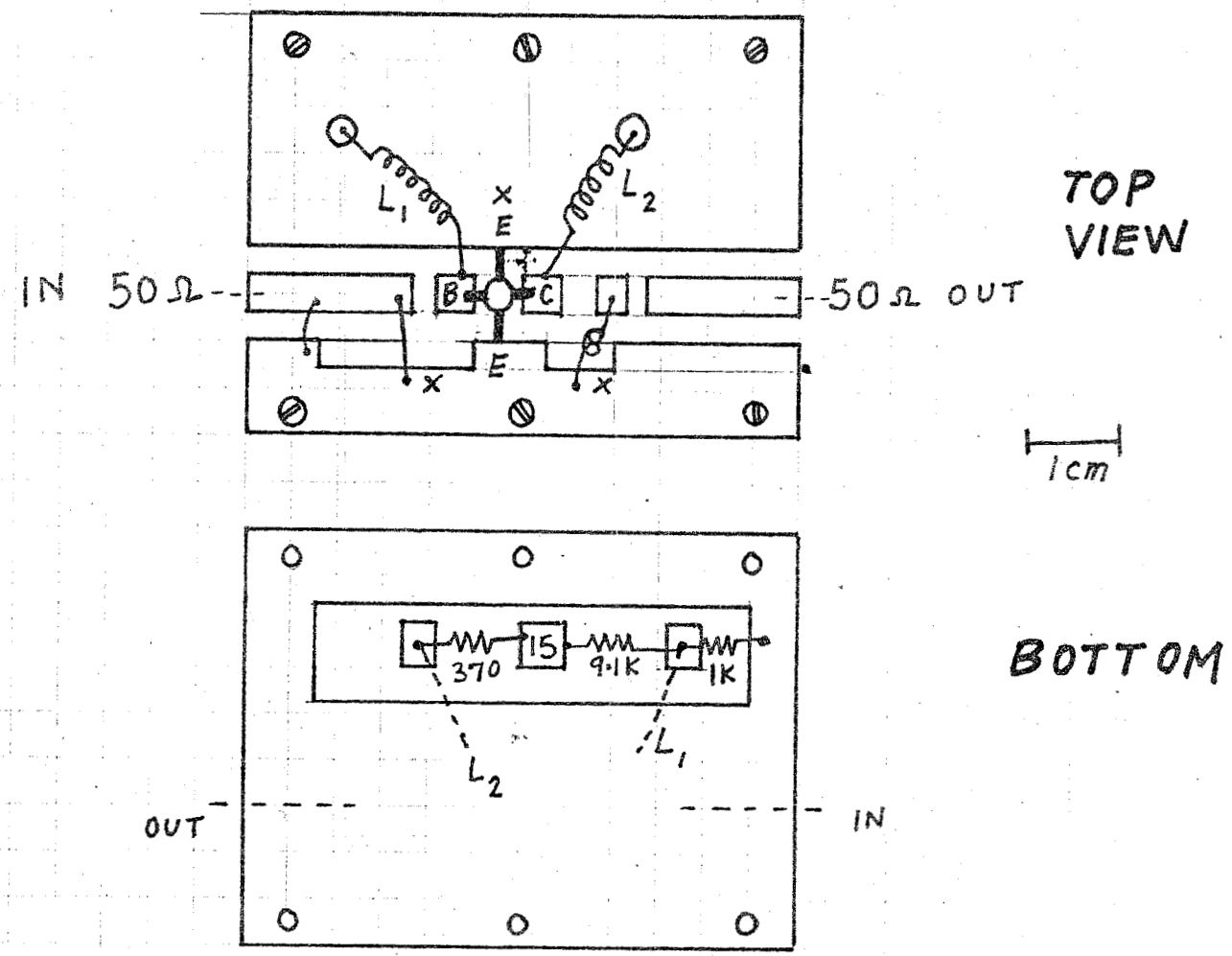
C_1, C_2 = 1000 pF R.F. bypass
47 pF d.c. block
} American Technical Ceramics chip capacitors

L_1, L_2 $\lambda/4$ length at 1.4 ghz, pass only dc

1.8 nH
7.6 nH
} tinned Cu wire, 0.6 mm dia.
≈ 10 nH/cm ; 2mm & 8mm length.

Bias : V_{CE} = 12 Volts, I_c = 8 mA

CIRCUIT BOARD LAYOUT – 1



E – emitter ; B – base ; C – Collector

X – through wire to ground plane

⊘ – grounding/mounting screws

gaps in 50Ω line are for capacitors;
left to right: 5.6 pF, 47 pF, 1.0 pF

), 𝄞 = inductors

Some amount of tuning is needed to achieve the desired centre frequency, matching and bandwidth, which can be simultaneously displayed on a swept frequency analyzer. The noise figure is measured and the input matching and bias conditions optimized for lowest noise. The noise figure is then determined and invariant to output match, which is retuned to give best stable gain. Depending on the relative priorities, design may be carried out for (i) optimum noise figure. (ii) maximum gain at a spot frequency. (iii) best gain flatness over a wide band. (iv) maximum linear output power.

3.2 Results:

Centre frequency : 1.4 GHz

Gain : 11 dB

noise figure : 3.7 dB

output match (Return loss) : 8 dB

input match : 30 dB at 1.4 GHz.

3dB gain bandwidth : 200 MHz.

Increasing the output power causes the gain to fall at the onset of non-linearity. This is measured by the 1-dB gain compression power output = -5dBm.

3.3. FET low noise amplifier:

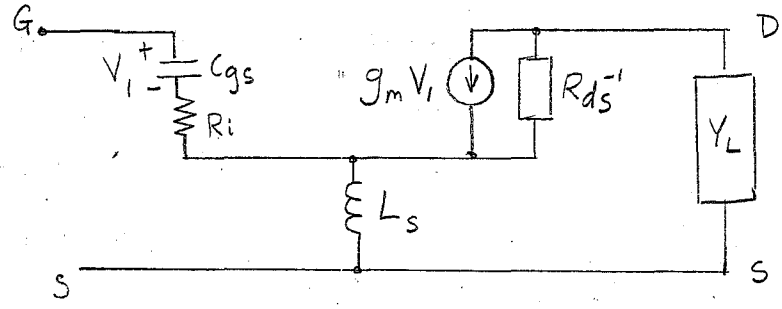
As already outlined, low noise amplifier design usually involves (i) selection of the bias point and the input matching network for mimimum noise, (ii) matching of output for maximum gain or broad bandwidth. With Ga-As fets, especially at lower frequencies (below 4 GHz) this procedure encounters the following drawbacks:

(i) The device is potentially unstable both in and out of band, and remains capable of activity upto very high frequencies (eg maximum frequency of oscillation f_{max} = 50 GHz) There is thus the possibility of unwanted oscillation if impedances are not carefully chosen.

(ii) The source impedance for optimum noise differs considerably from that for conjugate input match, leading to high VSWR for the low noise amplifier.

(iii) The high-Q reactive input makes the achievement of broadband operation difficult.

Effect of a feedback inductance in the source lead:



If R_{DS} and y_L^{-1} are large compared to ωL_s, the expression for input impedance is

$$Z_{in} \simeq R_i + \frac{1}{j\omega C_{gs}} + j\omega L_s + L_s g_m / C_{gs}\left(1 + \frac{1}{y_L R_{DS}}\right) + \omega^2 L_s^2 / R_{DS}\left(1 + \frac{1}{y_L R_{DS}}\right)$$

The last two terms increase the real part of the Z in (Rin) and if ωL_s is small, its contribution to the imaginary part (X in) is small. Rin can be pushed towards the source impedance for minimum noise, (R_{opt} + j. X opt) by suitable choice of L_s. Increasing Rin also results in an improved

bandwidth.

Noise measure M_{min} is defined as the noise figure of an infinite chain of identical amplifiers, $M_{min} = \frac{T_{min}}{T_o(1-G^{-1})}$ [T_o = ambient

Adding lossless feedback elements to any network may decrease T_{min} and G, but leaves M_{min} unaltered. For the FET (ref 5,6) the effect is to reduce X_{opt} by w.L_s (ie L_s appears effectively in series with the gate).

Thus the addition of a source inductance leads to lower VSWR, broader bandwidth and (as seen later) greater stability. The design procedure uses the S-parameter concepts of sec. 3.1 and goes as follows:

(i) From the performance data of the transistor, the bias point for minimum noise is selected. As expected, the drain voltage V_{DS} is low, corresponding to little noise from the velocity saturated electrons under the gate, and I_{DS} is about 15 % of I_{DSS}, the zero gate voltage drain current. (see section on FET noise). Common source S-parameters under these conditions are used in subsequent calculations.

The bare fet has a stability factor K = .25, highly unstable, and input reflection coeff. $\Gamma_{in} = .94 \angle -60°$, highly reactive.

(ii) The effect of L_s is included as follows:
Recognizing that the composite structure may be split into two 2-ports in series, their individual Z parameters may be summed to give the overall Z parameters, which are then converted back to equivalent S-parameters.

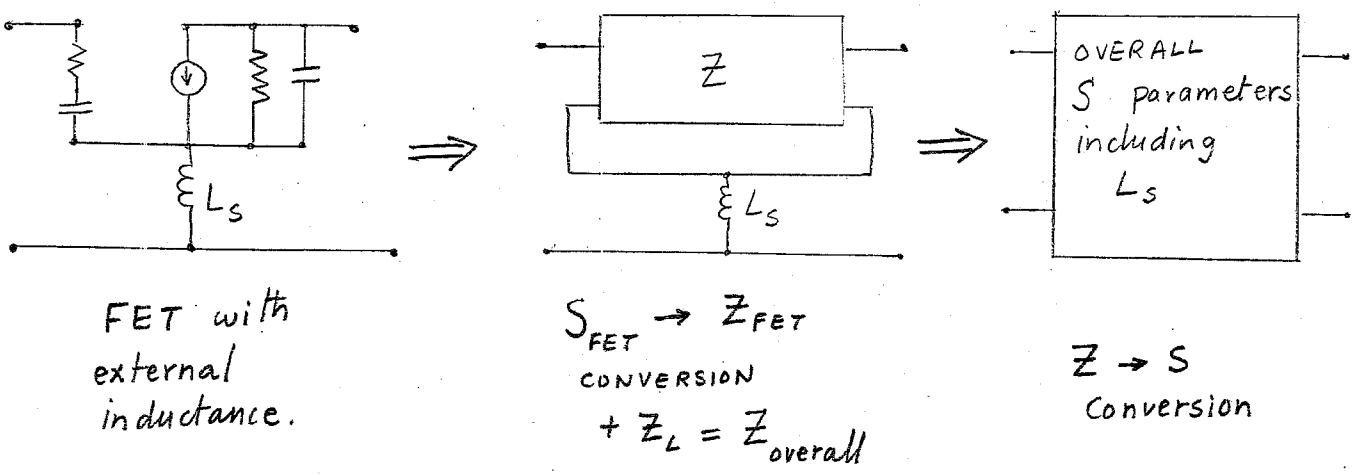


FIG 3.4 INCLUSION OF SOURCE INDUCTANCE

The modified parameters are found for several trial inductances over a range of frequencies. The final value of L_s is chosen as 4 nH, and sample parameters are shown at 1.4 GHz

$$[S]_{\text{original, 1.4 GHz}} = \begin{bmatrix} .97 \angle -19^\circ & .02 \angle 72^\circ \\ 2.06 \angle 152^\circ & .93 \angle -8^\circ \end{bmatrix}$$

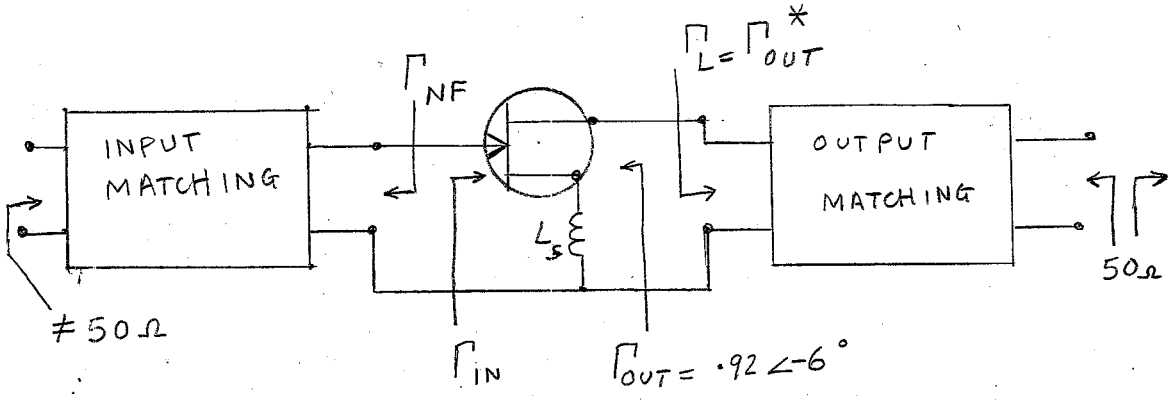
$$[S]_{\substack{\text{modified, 1.4 GHz} \\ \text{4nH}}} = \begin{bmatrix} .86 \angle -12^\circ & .02 \angle 96^\circ \\ 1.5 \angle 122^\circ & .93 \angle -3^\circ \end{bmatrix}$$

When K is calculated for the modified set, K = 1.1 and G_{max} = 17 dB, showing the stabilizing effect of the source inductance. The modified source impedance (as already indicated) is found:

$$Z'_{NF} = Z_{NF} - j\omega L_s$$

The 50 Ω source is transformed by a matching network to present this Z'_{NF} to the transistor input, and the corresponding output impedande determined from equations (A4). The output is then conjugately matched to 50 Ω and the resultant input impedance found from equations (A 4) ie: fix the source, match

the resultant output to load and find the new input impedance. (The transistor is non unilateral, hence the back and forth procedure).



This exercise yields a Γ^*_{in} ($.83 \angle 24^\circ$) closer to the modified Γ_{NF} ($.65 \angle 22^\circ$) than was obtained without the source inductance, giving a better input match. The expected gain at 1.4 GHz is about 17 dB, as seen from the location of Γ_L on the constant gain circles of the Smith chart. Stability circles are plotted for both input and output, Using the modified parameters at increasing frequencies. The high pass load and source impedances, Γ_s and Γ_L, migrate with frequency along the loci shown, and remain in the stable region upto about 5 GHz. However, beyond this frequency, the transistor's changing characteristics cause the impedances to be no longer suitable to it and instability results. The source inductance is now found to aid in the de-stabilization at high frequency by feeding back more output to the input, since its impedance increases with frequency. Analysis of high frequency oscillation is difficult since distributed effects cause capacitors to behave as inductors and coiled wire inductors to be more capacitive than inductive. Two possible solutions(neither of which was found necessary) are:

(i) inserting a metal partition isolating input and output sides of the amplifier. (ii) a microwave absorber such as carbon impregnated foam placed at the input and output introduces a loss at higher frequencies leaving the low frequency characteristics intact i.e. the amplifier cavity is no longer an effective resonant cavity at high frequency.

3.4 Results:

The constructed amplifier was found to have the following characteristics:

gain: 17 dB at 1360 MHz

3 dB bandwidth : 120 MHz

input return loss : 10 dB

The stability was found to depend upon the bias condition, specifically V_{DS} larger than about 3.5 volts caused oscillation to set in. However, minimum noise conditions were at $V_{GS} = -1.7V$ and $V_{DS} = 2$ to 2.5 volts, at which point there was no stability problem. Noise figure measurement yielded a noise temperature of around 100°K (1.29 dB N.F.) at 1400 MHz and 90°K at 1350 MHz, both at 300°K ambient.

The circuit diagram and frequency response plots in the minimum noise condition are shown in the acompanying diagrams.

CONCLUSIONS and comments on further development.

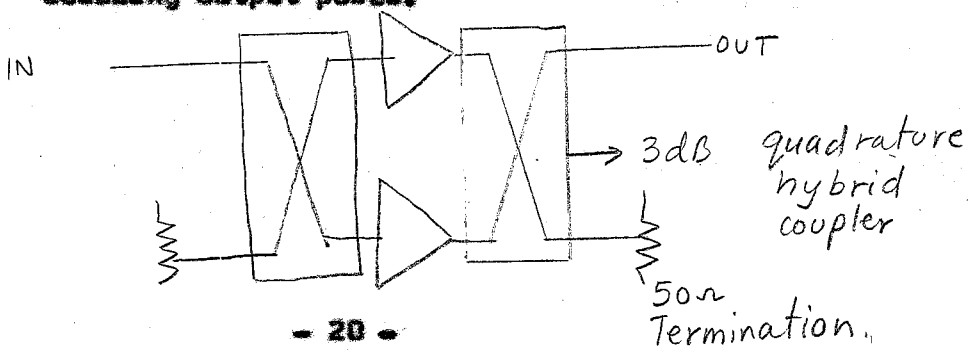
The amplifier constructed could find possible use as a communications receiver front end, without cooling or further refinement. To meet the more stringent requirements of a radio telescope front end however, improved performance is desired. Some of these improvements and the problems involved are listed:

(i) Cooling to liquid nitrogen temperature (77°K) or below reduces thermal scattering in the channel. Device gain and noise parameters change, requiring a reoptimisation of bias and matching networks in the cooled condition. Stressing of bonds due to contraction may make the circuit unreliable or unworkable.

(ii) It may be possible to increase the bandwidth to a comfortable amount by
   (a) computer synthesis of higher order matching networks,
   (b) optimizing feedback via noiseless elements (reactive in order to preserve the noise figure).

(iii) With variable impedance matching elements, the noise behaviour of the device can be explored over a range of source conditions, leading to a full characterization in terms of the 4 noise parameters of appendix C.

(iv) Together with power splitters and combiners, a 2 transistor balanced circuit instead of a single ended amplifier can give low SWR while maintaining optimum noise match and doubling output power.



HANDLING AND PRACTICAL DETAILS

While it is not as sensitive to mishandling as the bare chip, the packaged fet must still be handled cautiously:

1. Ungrounded personnel should not touch the leads, since transients easily damage the gate.
2. Soldering iron must be properly grounded and any source of transients eliminated.
3. A FET should never be inserted into a pre-biased circuit.

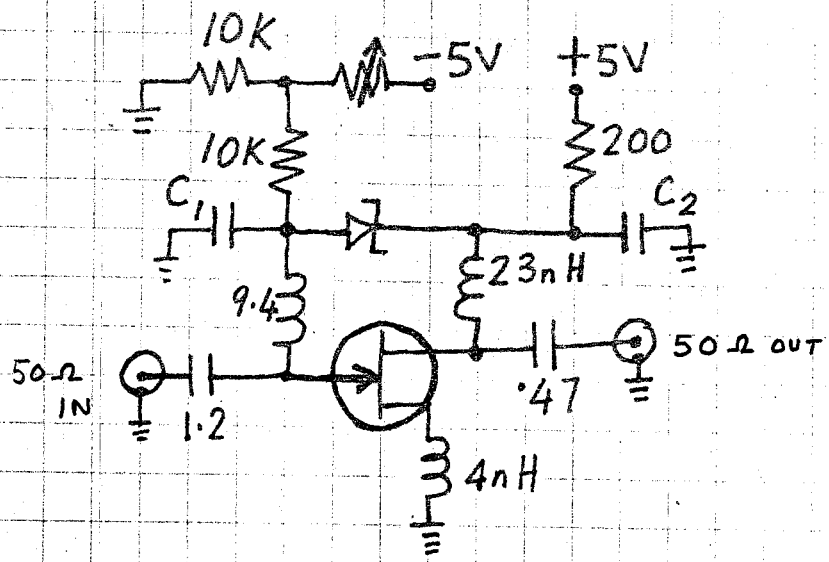
Even in the soldered-in circuit, switch-on should be done gradually: First the gate is set to -2 V, then drain voltage is applied slowly and finally gate is readjusted to get desired drain current.

4. Use of a digital multimeter to check resistances of the device should be avoided since the voltage supply within the meter may destroy the gate.
5. Soldering time should not exceed 20 secs. at 260° C.

Indium alloy solder, with melting point 180° C was used for soldering the transistor and all ceramic chip capacitors. This contains 2% silver, which is necessary to keep the silver in the chip capacitor bonding pads from leaching out while soldering.

6. The 50 Ω microstrip lines for input output were formed by applying 4.5 mm masking tape to the PCB and etching. All bonding islands etc., on the board are kept to minimum area to avoid the introduction of unpredictable distributed elements into the circuit. (Capacitance to ground plane is 0.1 Pf/cm^2).

CIRCUIT 2



C_1, C_2 = 100.0 pF chips. capacitors

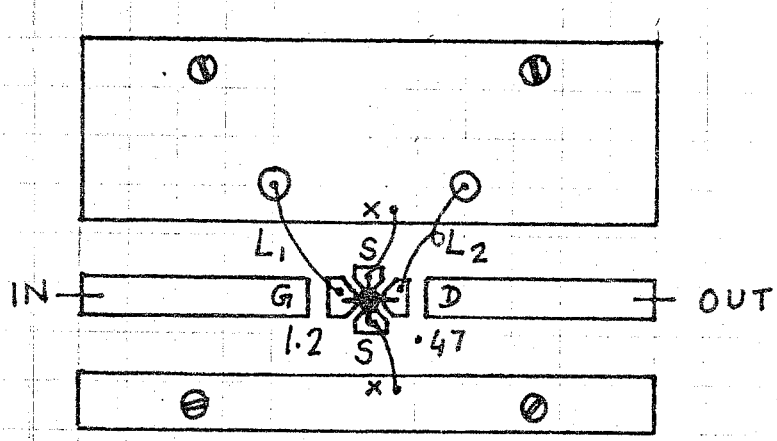
1.2, .47 pF : Variables.

All other details as in CIRCUIT 1

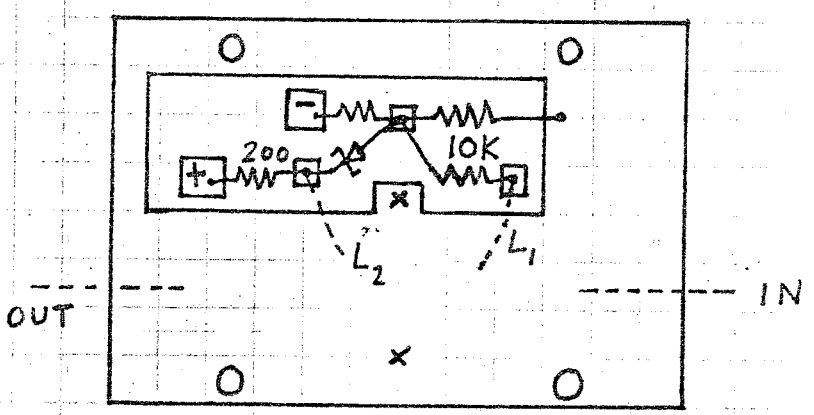
Bias: V_{DS} = 2.5 Volts I_{DS} = 8mA

V_{GS} = − 1.7 Volts

CIRCUIT BOARD LAYOUT - 2



TOP



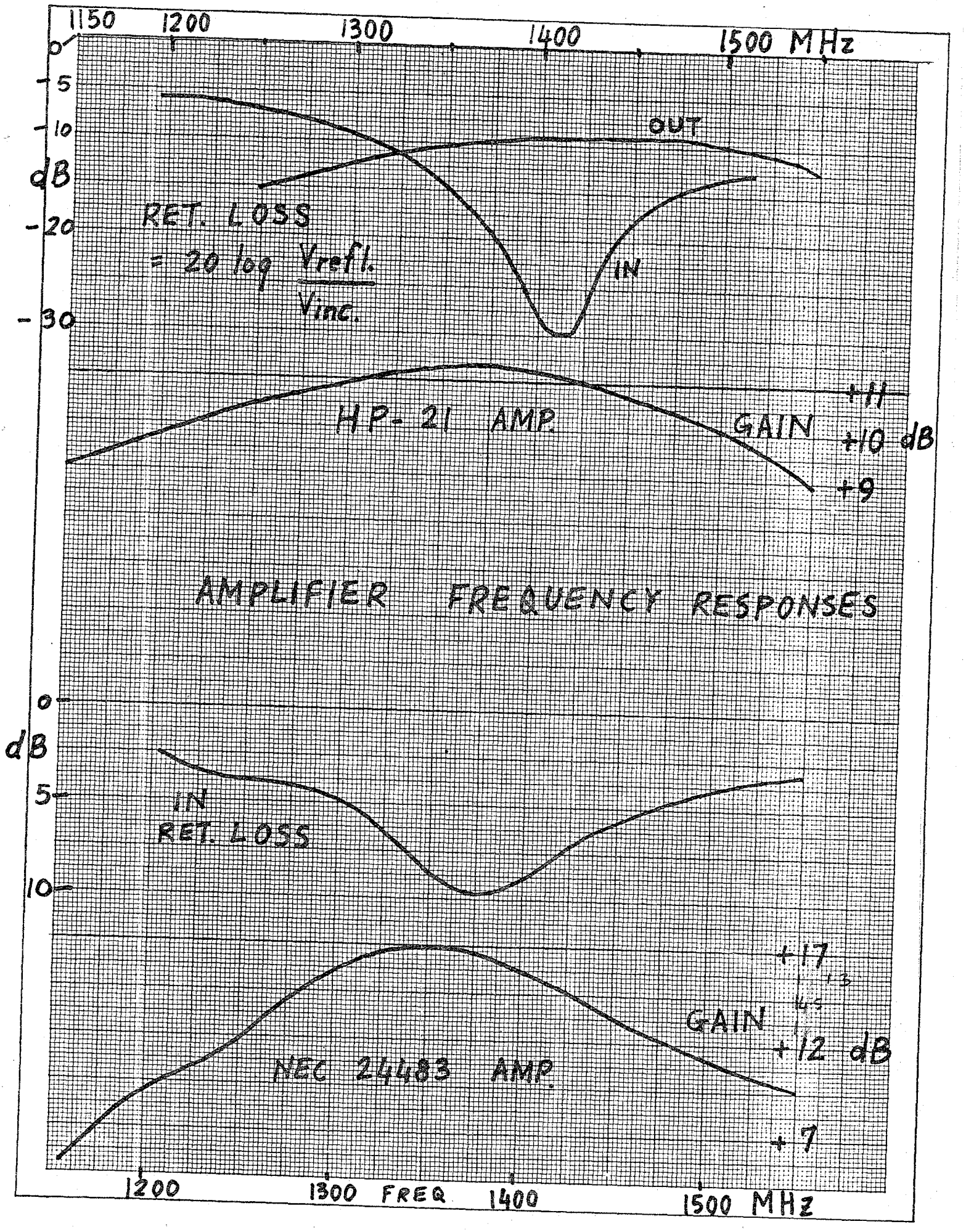
BOTTOM

S - Source ; G - gate ; D - drain

$L_1 = 9.4$ nH ; $L_2 = 23$ nH

1.2 PF, .47 pF Variables

: 5 Volts, supply reversal protection and limiting V_{GD}


1150
1200
1300
1400
1500 MHz
0
5
10
dB
20
30
OUT
IN
RET. LOSS
= 20 log Vrefl. / Vinc.
HP-21 AMP.
GAIN
+11
+10 dB
+9
AMPLIFIER FREQUENCY RESPONSES
0
dB
5
10
IN
RET. LOSS
+17
+13
+12 dB
+7
GAIN
NEC 24483 AMP.
1200
1300 FREQ
1400
1500 MHz

NEC MICROWAVE TRANSISTOR SERIES

NE244

Low-Noise X-Band GaAs MESFET

FEATURES

- VERY HIGH f_{MAX}
  55 GHz
- HIGH MAXIMUM AVAILABLE GAIN
  17 dB at 4 GHz
  12 dB at 8 GHz
  10 dB at 12 GHz
- LOW NOISE FIGURE
  1.4 dB at 4 GHz
  2.5 dB at 8 GHz
  3.5 dB at 12 GHz
- HIGH ASSOCIATED GAIN
  13.5 dB at 4 GHz
  10.5 dB at 8 GHz
  7.0 dB at 12 GHz
- PROVEN RELIABILITY AND STABILITY
- 1.0 MICRON GATE
- SPACE QUALIFIED

DESCRIPTION

The NE244 is a gallium arsenide (GaAs) n-channel field effect transistor (FET) employing a 1.0μ long Schottky-barrier gate. The device is available as a chip (NE24400) and in two rugged hermetically sealed metal-ceramic stripline packages. The chip offers exceptionally low noise figures and high associated gains, making it ideal for microwave integrated circuits operating up to 12 GHz. The chip's gate and channel are glassivated with a thin layer of SiO_2 for mechanical protection only. The NE24483 is a low cost packaged device for industrial, military, and space applications. The NE24406 is in a low-loss, hi-rel package designed for space applications. NEC uses the highest grade materials and the latest design and production techniques to manufacture the best devices available. Reliability is assured by quality control and test procedures patterned after MIL-S-19500 and MIL-STD-750. Long term performance stability is assured by NEC proprietary wafer selection and processing. The exceptionally high gain, associated with a very low noise figure, has made the NE244 the industry's standard. The NE244 offers the engineer the best in performance, reliability and quality.

PERFORMANCE SPECIFICATIONS (T_a=25°C)

NE PART NUMBER EIAJ[1] REGISTERED NUMBER PACKAGE CODE			NE24400 Chip			NE24406 2SK85 06			NE24483 83		
SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
f_{MAX}	Maximum Frequency of Oscillation at V_{DS}=3V, I_{DS}=30mA	GHz		55			55			55	
MAG	Maximum Available Power Gain[2] at V_{DS}=3V, I_{DS}=30mA (Typ. I_{DS}=50% I_{DSS})										
	f = 4 GHz	dB		17			17			17	
	f = 8 GHz	dB		12			11			11	
	f = 12 GHz	dB		10			9			9	
NF_{MIN}	Minimum Noise Figure[3] at V_{DS}=3V, I_{DS}=10mA (Typ. I_{DS}=15% I_{DSS})										
	f = 4 GHz	dB		1.4			1.5			1.5	
	f = 8 GHz	dB		2.5	3.5[4]		2.7	3.5		2.7	3.5
	f = 12 GHz	dB		3.5			3.9			3.9	
GNF	Associated Gain at NF at V_{DS}=3V, I_{DS}=10mA (Typ. I_{DS}=15% I_{DSS})										
	f = 4 GHz	dB		13.5			13.0			13.0	
	f = 8 GHz	dB	8.5[4]	10.5		8.5	10.0		8.5	10.0	
	f = 12 GHz	dB		7.0			6.5			6.5	
P_{OUT}	Output Power at 1 dB Compression Point at V_{DS}=3V, I_{DS}=30mA (Typ. I_{DS}=50% I_{DSS})										
	f = 4 GHz	mW		10.0			10.0			10.0	
	f = 8 GHz	mW		7.1			7.1			7.1	

SEE NOTES ON BACK PAGE

ELECTRICAL CHARACTERISTICS (T_a=25°C)

NE PART NUMBER EIAJ[1] REGISTERED NUMBER PACKAGE CODE			NE24400 Chip			NE24406 2SK85 06			NE24483 83		
SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
I_{DSS}	Drain Current at V_{DS}=3V, V_{GS}=0	mA	30	60	100	30	60	100	30	60	100
V_p	Pinch-off Voltage at V_{DS}=3V, I_{DS}=0.1mA	V	-1.5	-4.0		-1.5	-4.0		-1.5	-4.0	
g_m	Transconductance at V_{DS}=3V, I_{DS}=10mA	mΩ	15	20	100	15	20	100	15	20	100
I_{GS}	Gate to Source Leakage Current at V_{GS}=-5V	μA		0.1	1.0		0.1	1.0		0.1	1.0
R_{th}	Thermal Resistance (C-A)	°C/W			170[5]			260			400
P_T	Total Power Dissipation	mW			500			500			300

SEE NOTES ON BACK PAGE

All DC tests performed per MIL-STD-750

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

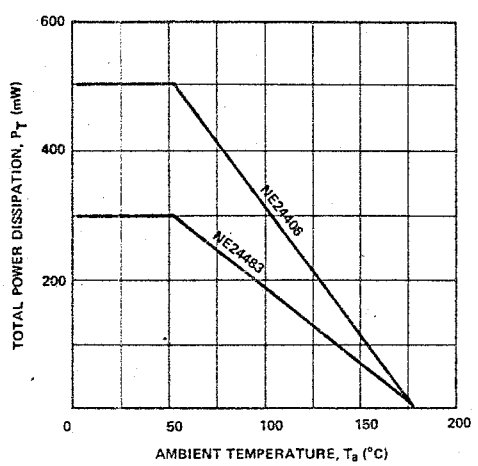
PARAMETER	SYMBOL	RATINGS	UNITS
Drain to Source Voltage	V_{DS}	5.0	V
Gate to Source Voltage	V_{GS}	-10.0	V
Drain Current	I_{DS}	100	mA
Channel Temperature	T_{ch}	175	°C
Storage Temperature	T_{stg}	-65 ~ +175	°C

RELIABILITY SCREENING (HES-32325-02, MIL-STD-750)

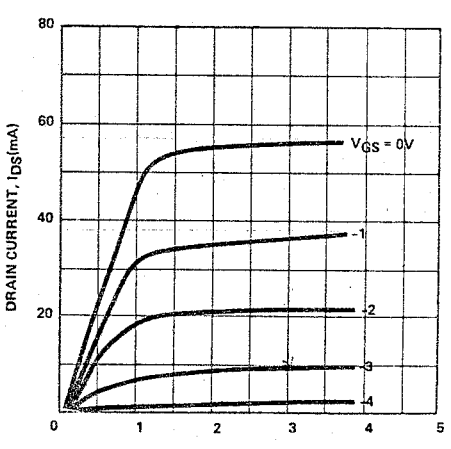
GRADE D (Industrial) 200-1200 Failures in 10^9 Device Hours (FIT)	GRADE C (Military) 50-300 Failures in 10^9 Device Hours (FIT)
100% DC Wafer Probe Pre-Cap Inspection (Sample basis) 100% Gross Leak Test 100% Mechanical Shock Test 100% Group A Tests (Tests may vary depending upon package style.)	100% DC Wafer Probe 100% Pre-Cap Inspection 100% Vacuum Bake (150°C - 1 hr) 100% Gross Leak Test 100% High Temperature Storage (125°C - 24 hrs) 100% Environmental Tests (Heat Cycle, Shock, Vibration, Centrifuge) 100% Power Burn-in at $P_c$max (T_{ch}=125°C, T_a =100°C - 168 hrs) 100% Group A Tests

DEVICE CHARACTERISTICS

POWER DERATING CURVES

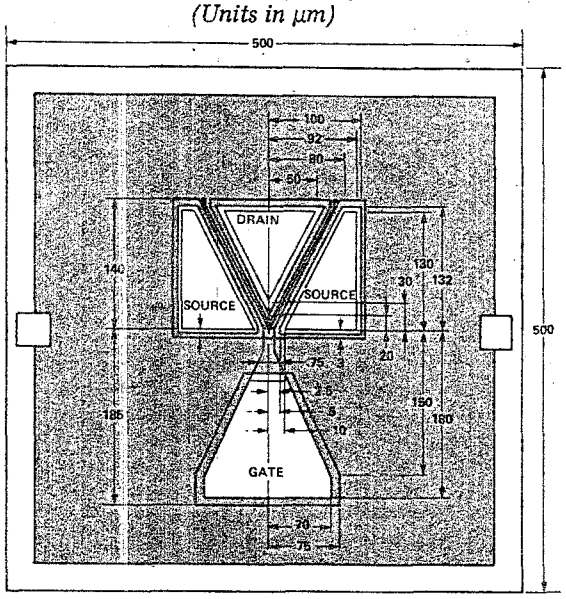


DC PERFORMANCE



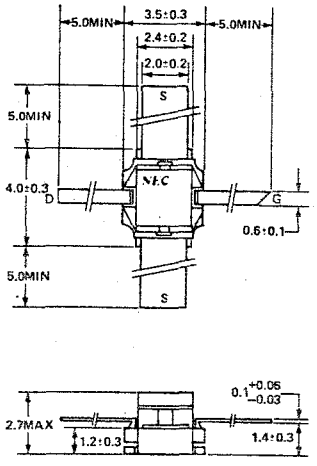
PHYSICAL DIMENSIONS

NE24400 (CHIP)
(Units in μm)

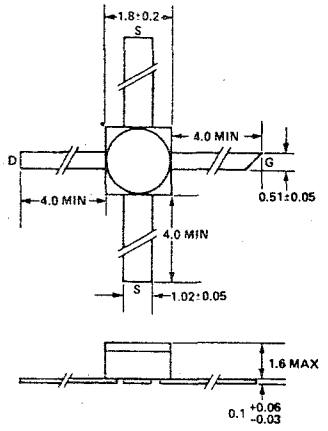


SiO_2 GLASSIVATED REGION
All bonding pads are Ti-Pt-Au

NE24406
(Units in mm)

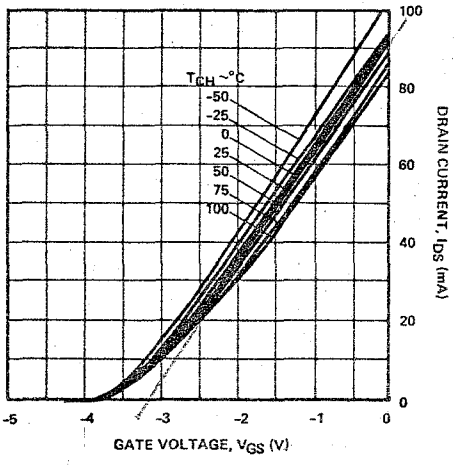


NE24483
(Units in mm)

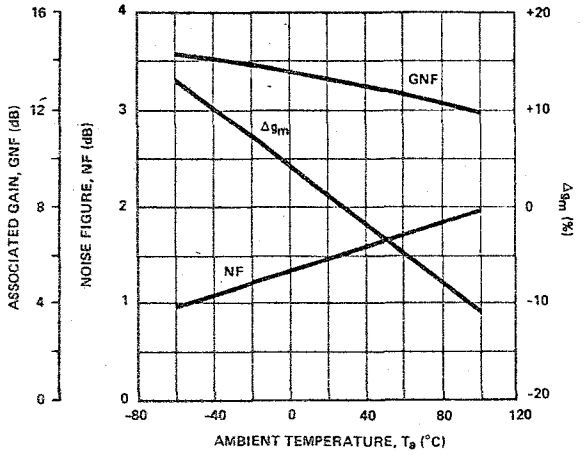


PERFORMANCE CHARACTERISTICS

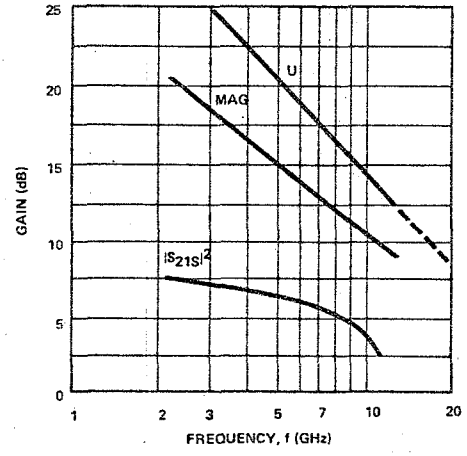
DRAIN CURRENT VS. GATE VOLTAGE AT VARIOUS CHANNEL TEMPERATURES



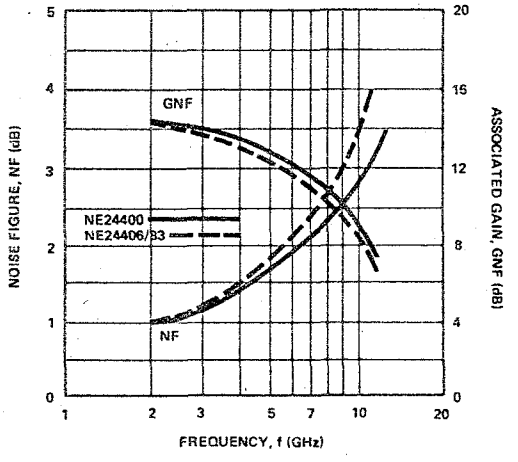
TYPICAL PERFORMANCE VS. AMBIENT TEMPERATURES FOR THE NE24406 AND NE24483 AT 4.0 GHz WITH I_{DS} = 10mA AND V_{DS} = 3V



TYPICAL GAIN VS. FREQUENCY FOR THE NE24406 AND NE24483 AT V_{DS}=3V AND I_{DS}=30mA

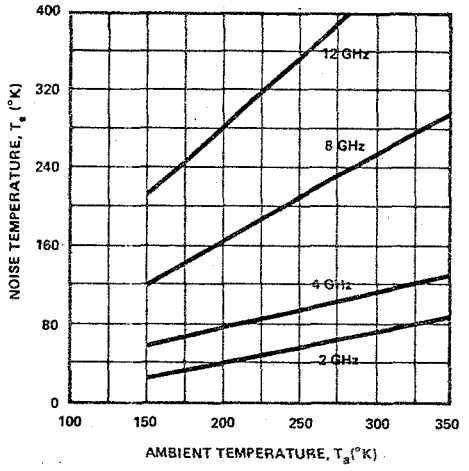


TYPICAL NOISE FIGURE AND ASSOCIATED GAIN VS. FREQUENCY AT V_{DS}=3V AND I_{DS}=10mA

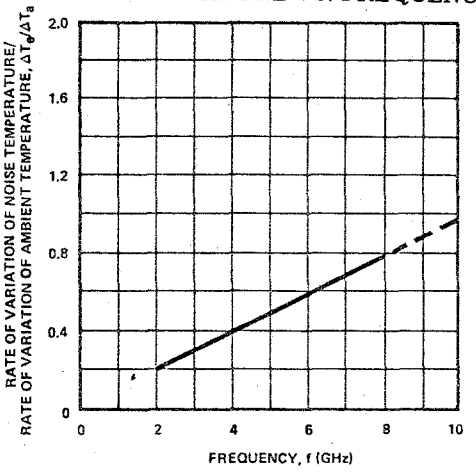


PERFORMANCE CHARACTERISTICS (Cont'd)

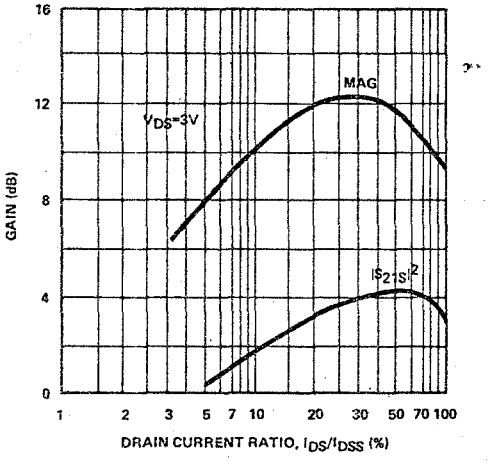
TYPICAL NOISE TEMPERATURE VS. AMBIENT TEMPERATURE FOR THE NE24406 AND NE24483 AT VARIOUS FREQUENCIES



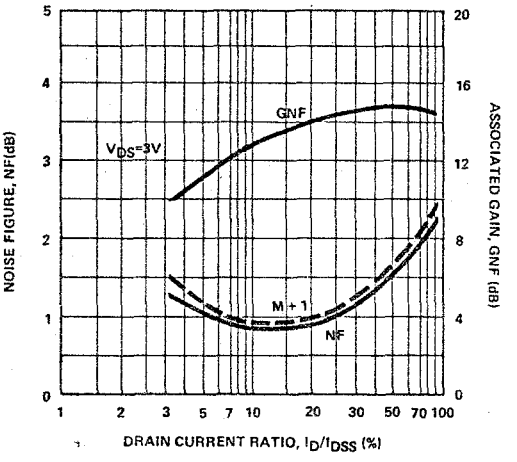
RELATIONSHIP BETWEEN THE RATE OF VARIATION OF NOISE TEMPERATURE/ RATE OF VARIATION OF AMBIENT TEMPERATURE VS. FREQUENCY



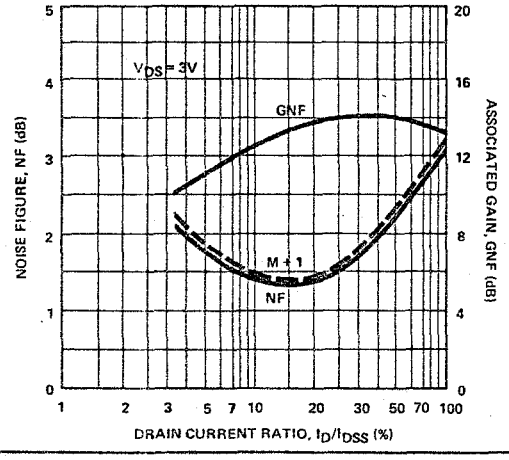
TYPICAL GAIN VS. DRAIN CURRENT RATIO FOR THE NE24406 AND NE24483 AT 8.0 GHz



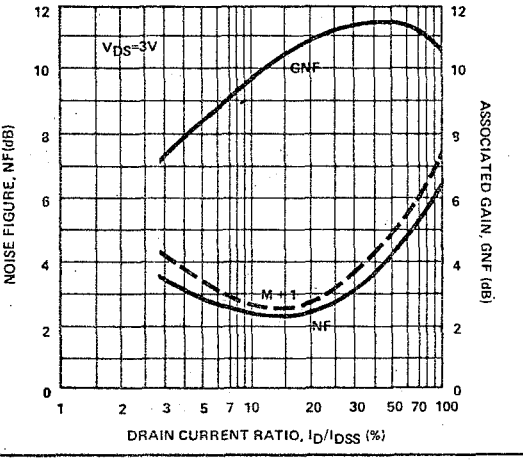
TYPICAL NOISE FIGURE AND ASSOCIATED GAIN VS. DRAIN CURRENT RATIO FOR THE NE24406 AND NE24483 AT 1.9 GHz



TYPICAL NOISE FIGURE AND ASSOCIATED GAIN VS. DRAIN CURRENT RATIO FOR THE NE24406 AND NE24483 AT 4.0 GHz

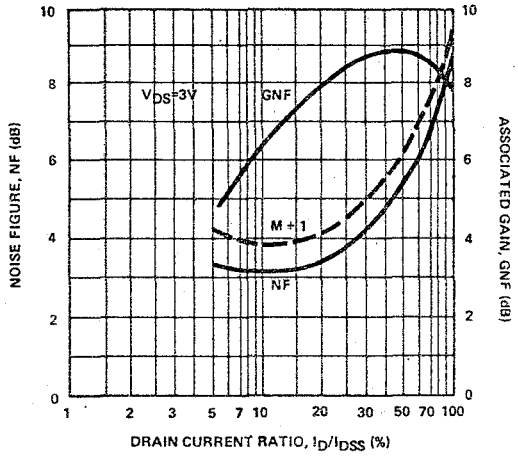


TYPICAL NOISE FIGURE AND ASSOCIATED GAIN VS. DRAIN CURRENT RATIO FOR THE NE24406 AND NE24483 AT 8.0 GHz

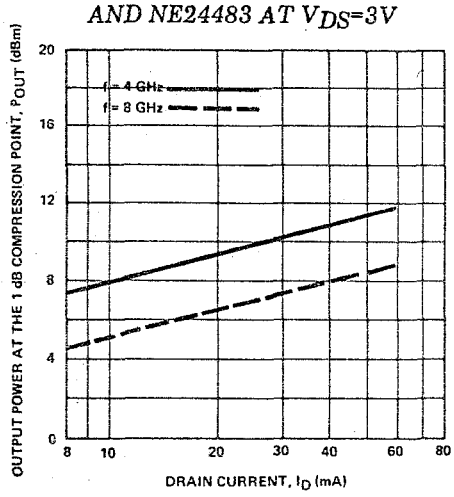


PERFORMANCE CHARACTERISTICS (Cont'd)

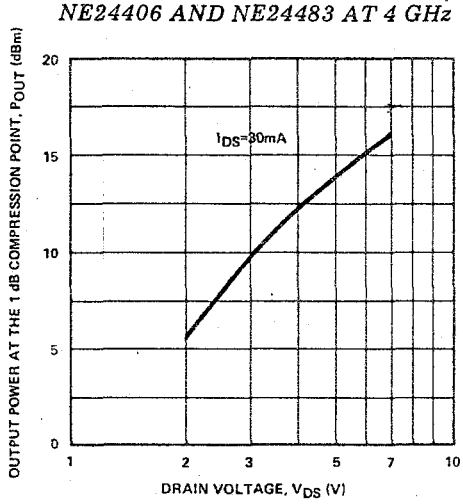
TYPICAL NOISE FIGURE AND ASSOCIATED GAIN VS. DRAIN CURRENT RATIO FOR THE NE24406 AND NE24483 AT 10.6 GHz



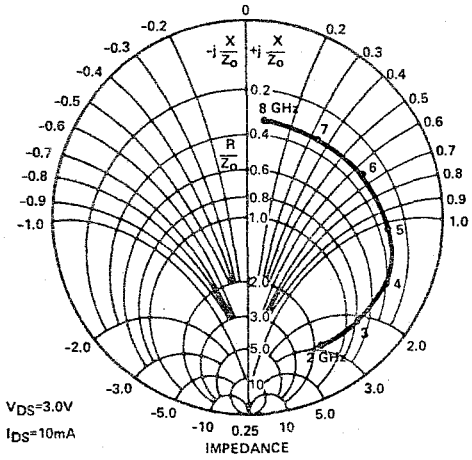
TYPICAL OUTPUT POWER AT THE 1 dB COMPRESSION POINT VS. DRAIN CURRENT FOR THE NE24406 AND NE24483 AT V_{DS}=3V



TYPICAL OUTPUT POWER AT THE 1 dB COMPRESSION POINT FOR THE NE24406 AND NE24483 AT 4 GHz

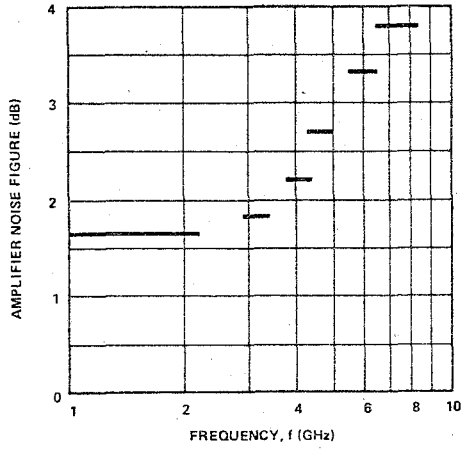


TYPICAL SOURCE IMPEDANCE DATA FOR OPTIMUM NOISE FIGURES FOR THE NE24406 AND NE24483

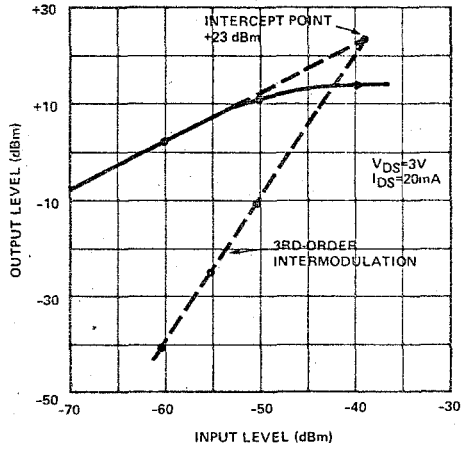


AMPLIFIER CHARACTERISTICS

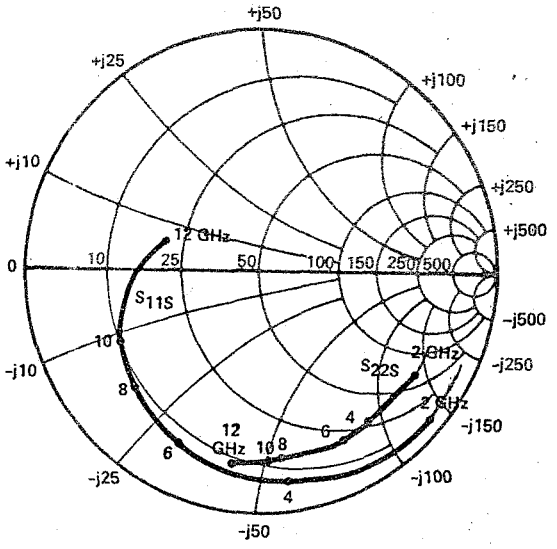
TYPICAL LOW NOISE AMPLIFIER NOISE FIGURE VS. FREQUENCY USING THE NE24406

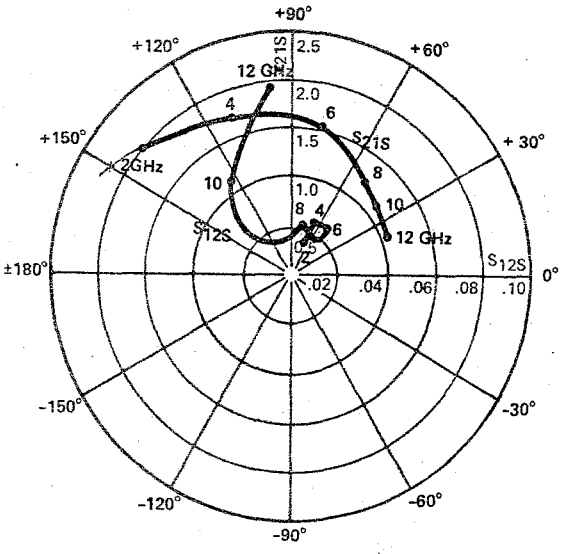


INPUT/OUTPUT LINEARITY CHARACTERISTICS FOR A 4 GHz 125°K LOW NOISE AMPLIFIER USING THE NE24406



NE24483 COMMON SOURCE SCATTERING PARAMETERS





Coordinates in Ohms
Frequency in GHz
(V_{DS}=3V, I_{DS}=30mA, Z_{OUT}=50Ω)

S–MAGN AND ANGLES

V_{DS}=3V, I_{DS}=10mA

FREQUENCY (MHz)	S11		S21		S12		S22	
2000	.950	–39	1.795	143	.024	63	.812	–23
3000	.872	–58	1.684	128	.032	56	.768	–34
4000	.891	–78	1.628	110	.039	45	.796	–49
5000	.888	–93	1.547	95	.041	41	.831	–59
6000	.805	–108	1.404	78	.050	32	.805	–69
7000	.757	–121	1.200	66	.043	23	.776	–80
8000	.747	–131	1.048	57	.039	20	.808	–88
9000	.693	–139	0.977	48	.026	–10	.792	–91
10000	.644	–143	0.963	49	.027	62	.831	–91
11000	.533	–158	1.041	38	.038	60	.837	–92
12000	.470	171	1.195	19	.045	52	.811	–100

V_{DS}=3V, I_{DS}=30mA

2000	.947	–41	2.028	142	.015	66	.799	–23
3000	.866	–61	1.892	128	.018	64	.760	–33
4000	.888	–82	1.824	110	.021	69	.791	–46
5000	.870	–98	1.711	94	.028	52	.832	–57
6000	.797	–114	1.552	78	.024	52	.808	–66
7000	.748	–126	1.316	65	.021	62	.776	–78
8000	.734	–137	1.154	56	.020	73	.805	–86
9000	.662	–145	1.055	48	.014	96	.806	–89
10000	.608	–150	1.054	47	.046	125	.840	–88
11000	.482	–169	1.121	37	.063	113	.859	–89
12000	.438	158	1.286	18	.078	100	.858	–97

APPENDIX A

S-PARAMETERS DESIGN EQUATIONS

1. **Definition:** With reference to Fig. A1.

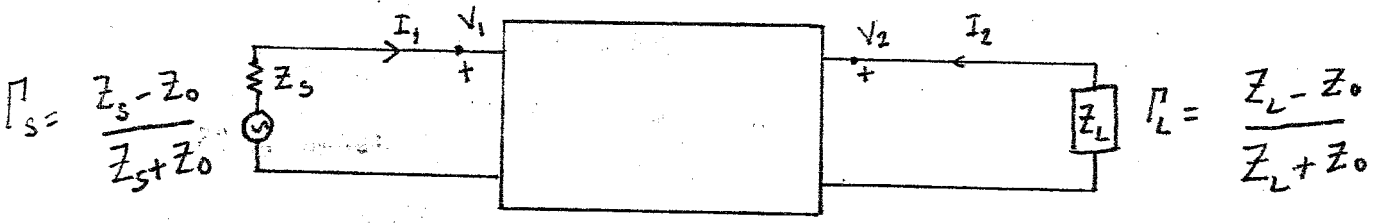


FIG.A1: 2-Port Embedded in a line of impedance Z_0

Total Voltage and Current Related to Travelling waves:

$$V_1 = \vec{E}_{i1} + \overleftarrow{E}_{x1}$$
$$V_2 = \overleftarrow{E}_{i2} + \vec{E}_{x2}$$
$$I_1 = (\vec{E}_{i1} - \overleftarrow{E}_{x1}) / Z_0$$
$$I_2 = (\overleftarrow{E}_{i2} - \vec{E}_{x2}) / Z_0$$

Power Related to Travelling waves:

$$a_1 = \vec{E}_{i1} / \sqrt{Z_0}$$
$$a_2 = \overleftarrow{E}_{i2} / \sqrt{Z_0}$$
$$b_1 = \overleftarrow{E}_{x1} / \sqrt{Z_0}$$
$$b_2 = \vec{E}_{x2} / \sqrt{Z_0}$$

a^2 represents incident power,
b^2 represents reflected power,

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \quad \text{- Eqn.A1.}$$

2. **Measurements:**

$S_{11} = \dfrac{b_1}{a_1} \Big|_{a_2 = 0}$ is ratio of reflected to incident Voltage with output matched to Z_0.

$S_{12} = \dfrac{b_1}{a_2} \Big|_{a_1 = 0}$ = reverse transmission with input matched.

$S_{21} = \dfrac{b_2}{a_1} \Big|_{a_2 = 0}$; $S_{22} = \dfrac{b_2}{a_2} \Big|_{a_1 = 0}$.

The measurement is easily performed on an instrument (such as the H-P vector voltmeter) which measures both amplitude and phase of a signal withrespect to a reference.

3. Signal flow graphs: The 2-port in equation A1 is represented in Fig. A2a.

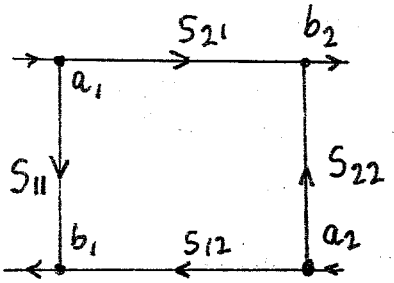


Fig.A2a - 2-port

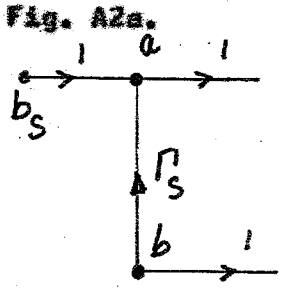


Fig.2b-Generator

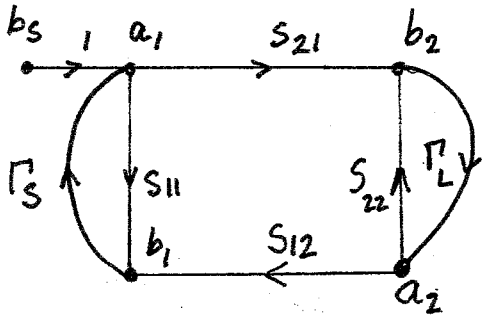


Fig.2c-2-port with Generator and load.

For the Generator: Power delivered into Z_o from a generator of impedance Z_s is $\frac{V_s^2}{(Z_o+Z_s)^2}$ $\qquad Z \equiv b_s^2$

Flow chart (2b) indicates $a = b_s + b\,\Gamma_s$; where $\Gamma_s = (Z_s-Z_o)/(Z_s+Z_o)$ is the voltage reflection coefficient of the source.

4. Mason's Rule:

L (1) = First order Loop = Product of paths encountered starting from a node and returning to it.

L (2) = Second order Loop = Product of any two non-touching first order loops.

L (3) = Third order Loop = Product of any three non-touching L (1)'s.

T = ratio of a dependant (Eg. b_2) to an independant (Eg. b_s) variable.

$$T = \frac{P_1}{\Delta}\left[1 - \Sigma L_1(1) + \Sigma L_1(2) - \Sigma L_1(3) \ldots\ldots\right] + \frac{P_2}{\Delta}\left[1 - \Sigma L_2(1) + \cdots\right] - \text{Eqn. A2.}$$

$$+ P_i/\Delta\left[1 - \Sigma L_i(1) \cdots\right]$$

Where P_i = Path 'i' from dependant to independant variable.

$\Sigma L_i\ (j)$ = Sum of jth order loops not touching. P_i.

$\Delta = [1 - L(1) + L(2) - \ldots]$

$\Sigma L(j)$ = Sum of all jth order loops.

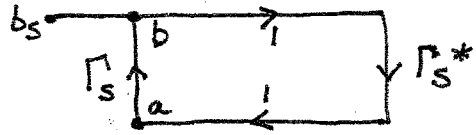


Fig. A4 Matched Generator.

P_{avs} = Power available from source = Power delivered under matched conditions.

$$= |b_1|^2 - |a_1|^2 = \frac{|b_s|^2}{1-|\Gamma_s|^2}$$ since

$$\frac{b}{b_s} = \frac{1}{1-\Gamma_s\Gamma_s^*} \quad \text{and} \quad \frac{a}{b_s} = \frac{\Gamma_s^*}{1-\Gamma_s\Gamma_s^*}$$ by Mason's rule applied to Fig. A4.

Power delivered to load = $P_{del} = |a_2|^2 - |b_2|^2$

G_T = Transducer power gain = $P_{del}/P_{avs} = \dfrac{b_2^2\,(1-|\Gamma_L|^2)}{|b_s|^2/(1-|\Gamma_s|^2)}$

Mason's rule applied to Fig. 2c now gives:

$$\frac{b_2}{B_s} = \frac{S_{21}}{1 - S_{11}\Gamma_s - S_{22}\Gamma_L - S_{21}S_{12}\Gamma_s\Gamma_1 + S_{11}S_{22}\Gamma_s\Gamma_L}$$

hence $$G_T = \frac{|S_{21}|^2\,(1-|\Gamma_s|^2)\,(1-|\Gamma_L|^2)}{|(1-S_{11}\Gamma_s)(1-S_{22}\Gamma_1) - S_{21}S_{12}\Gamma_s\Gamma_1|^2}$$ - Eqn.A3.

Stability: A network having positive real (p.r.) Z_{in} and Z_{out} for all p.r. sources and loads, is absolutely stable. Otherwise it is conditionally stable. (Both definitions are for a specific frequency.).

The Smith chart interior represents p.r. impedances, with $|\Gamma_S|$ and $|\Gamma_L| \leq 1$. Thus absolute stability implies $|\Gamma_{IN}|, |\Gamma_{OUT}| \leq 1$ for sources and loads in the chart interior.

From Fig. A2c and Eqn. A2,

$$\Gamma_{in} = \frac{b_1}{a_1} = S_{11} + \frac{S_{21} S_{12} \Gamma_L}{1 - S_{22} \Gamma_L} \qquad (a)$$

$$\Gamma_{out} = \frac{b_2}{a_2} = S_{22} + \frac{S_{21} S_{12} \Gamma_s}{1 - S_{11} \Gamma_s}$$

The boundary $|\Gamma_{in}| = 1$ has $|\Gamma_{IN}| > 1$ on one side, < 1 on the other ; ie. it partitions the output impedance plane into stable and unstable regions (ie. values of Γ_L in the unstable region cause $\Gamma_{IN} > 1$).
Putting $\left| S_{11} + \frac{S_{21} S_{12} \Gamma_L}{1 - S_{22} \Gamma_L} \right| = 1$ in Eqn. A4a gives a circle of centre $C_o = S_{22} - d S_{11}^*$; radius $\rho_o = \frac{|S_{12} S_{21}|}{|S_{22}|^2 - d^2}$

where $d = (S_{11} S_{22} - S_{21} S_{12})$; Subscript 'o' for output. i for input
Eqn. A4b gives expressions with Γ_L replaced by Γ_s and S_{22} by S_{11} . for the input stability circle, C_i and ρ_i.

To find which side of the boundary is stable say, for the input plane; put $\Gamma_S = 0$, which corresponds to the Smith chart centre, and causes $\Gamma_{OUT} = S_{22}$ (Eqn. A4b). The region in which the centre lies is then stable if $S_{22} < 1$ and unstable if $S_{22} > 1$.

$$\underline{\text{Stability Factor K}} = \frac{1 + d^2 - |S_{11}|^2 - |S_{22}|^2}{2 |S_{12} S_{21}|}$$

Where $d = (S_{11} S_{22} - S_{21} S_{12})$

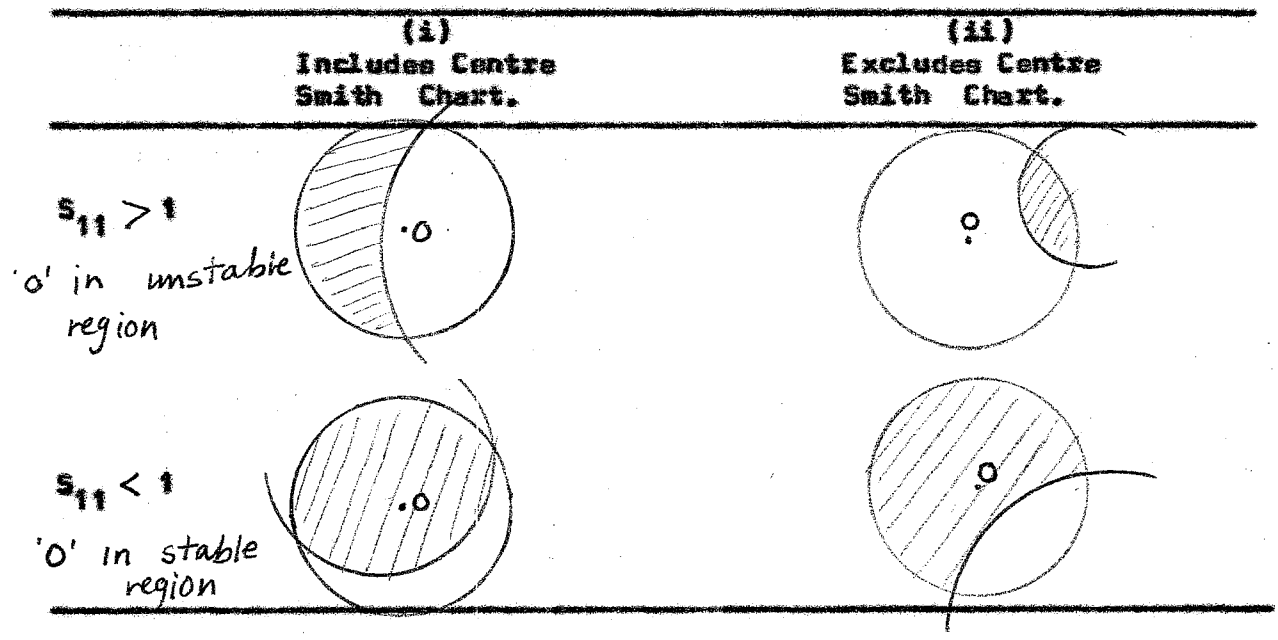
(i) for a unilateral device, $K = \infty$

(ii) for an absolutely stable device, $K > 1$, and the stability circle lies entirely outside the p.r. part of the Smith chart. Conjugate matching for maximum transducer gain is possible.

(iii) $K < 1$ means that there are p.r. impedances which can cause the device to oscillate. (Conjugate matching is undefined as the input impedance depends critically on the output load and vice versa). A stabilizing mismatch is necessary.

Graphically, stability is summarised in the following diagrams:

Stability Circle in Output Plane



In each case, stable p.r. impedance regions are shaded. Similar conditions hold in the input plane with S_{22} replacing S_{11}.

Constant gain circles are loci of impedances resulting in constant transducer gain, from equation A3.

C_g = Centre of gain circle = $\frac{G}{1 + DG}\ C^*$

radius $\rho_g = \left[1 - 2K\left|S_{21}\,S_{12}\right| G + \left|S_{12}\,S_{21}\right| G^2\right]^{1/2} (1 + DG)^{-1}$

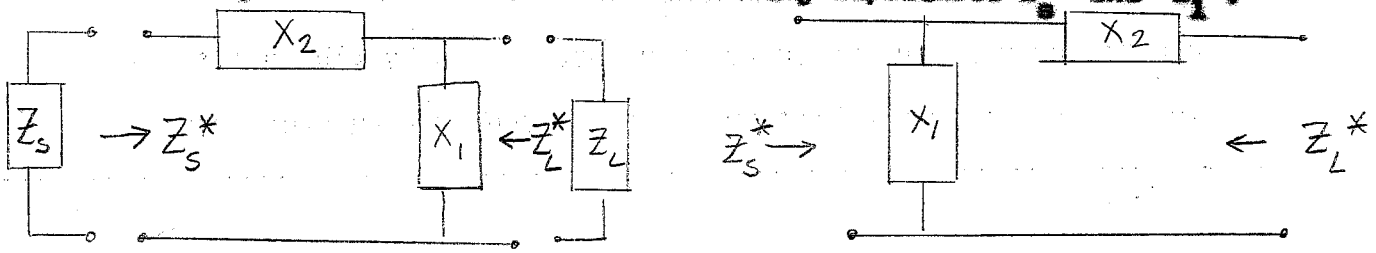
Where $G = \frac{\text{desired gain}}{S_{21}}$; $d = \left(- S_{12}\,S_{21} + S_{11}\,S_{22}\right)$

$D = \left|S_{22}\right|^2 - |d|^2$

$C = S_{22} - dS_{11}^*$

2 - element reactive matching:

With X_1 and X_2 purely reactive, there are 2 configurations that match the arbitrary impedances Z_s and Z_L.



In general for each configuration, there are 2 sets of reactances, but for some special cases only one distinct set exists

$$X_1 = \frac{X_L R_s}{R_s - R_L} \pm \left[\left(\frac{R_s X_L}{R_s - R_L}\right)^2 - R_s \left(\frac{X_L^2 + R_L^2}{R_s - R_L}\right)\right]^{1/2}$$

$$X_2 = R_s \left(\frac{X_1 + X_L}{R_L}\right) - \left(X_1 + X_s\right)$$; for the first configuration.

Reversing subscripts s and L gives the 2 sets of reactances for the second configuration.

These reactances are identical to those found by graphical means (Eg. on the Smith Chart).

APPENDIX B

Measurements:

1. Gain and Return loss (echo)

   Referring to Fig. B1 (overleaf)

   Detector R is the reference channel, 3dB- coupled to the forward main line; A is 3 dB - coupled to the input reflected wave, B is directly taken at the device output. The detector outputs are fed to Y-axis dc log amplifiers and displayed as A/R, B/R in dB against frequency.

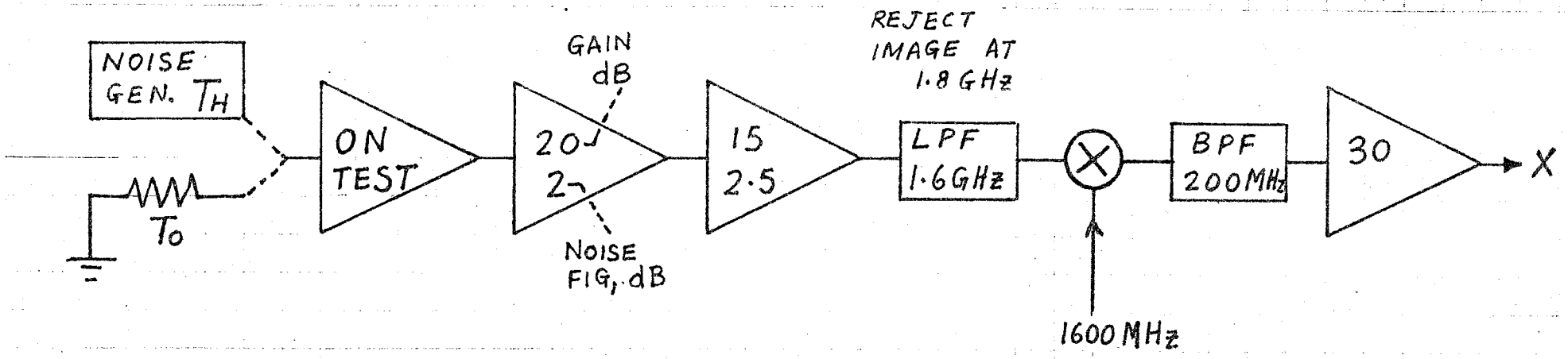
2. Noise:

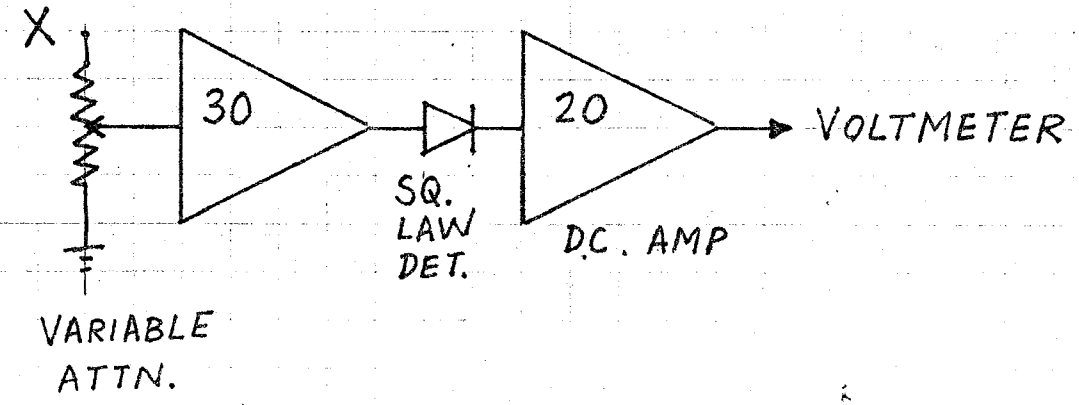
   Referring to Fig. B2, the top part of the diagram upto X, is used for automatic measurement by Noise, figure meter. The NF meter provides an output switched at 1 KHz between a gas tube noise source at equivalent temperature T_H and a resistor at standard temperature T_o corresponding outputs at X are $\propto (T_H + T_D)$ and $(T_o + T_D)$ where T_D = device equivalent noise temperature These are fed back to the meter, compared, and the N-F read of a calibrated scale. For more accurate manual measurements, T_H is injected from a calibrated noise diode, the output from X is further amplified, square law detected to yield a voltage proportional to power, and measured on a 4 digit DVM. The variable attenuation keeps the power in the square law region of the detector.

Noise diode has 5.76 dB excess noise, ie. T_H = 3.77 (300°K) = 1131°K.

	Voltage (mV)		Equivalent device Temp.	
	Source off	Source on	T_D	NF (dB).
Freq.	155 mV	475 mV	102.5	1.29
	150 "	468 "	98.5	1.24
1400 MHz.	180.7	555	101.2	1.27
	118.8	366	99.5	1.25

	Voltage (mV)		Equivalent device Temp.	
	Source off	Source on	T_D	NF (dB)
Freq.	174 mV	548	87.6	1.11
	139 "	435	91.2	1.15
1380 MHz	100 "	314	89.3	1.13
	51.6 mV	162	89.4	1.13





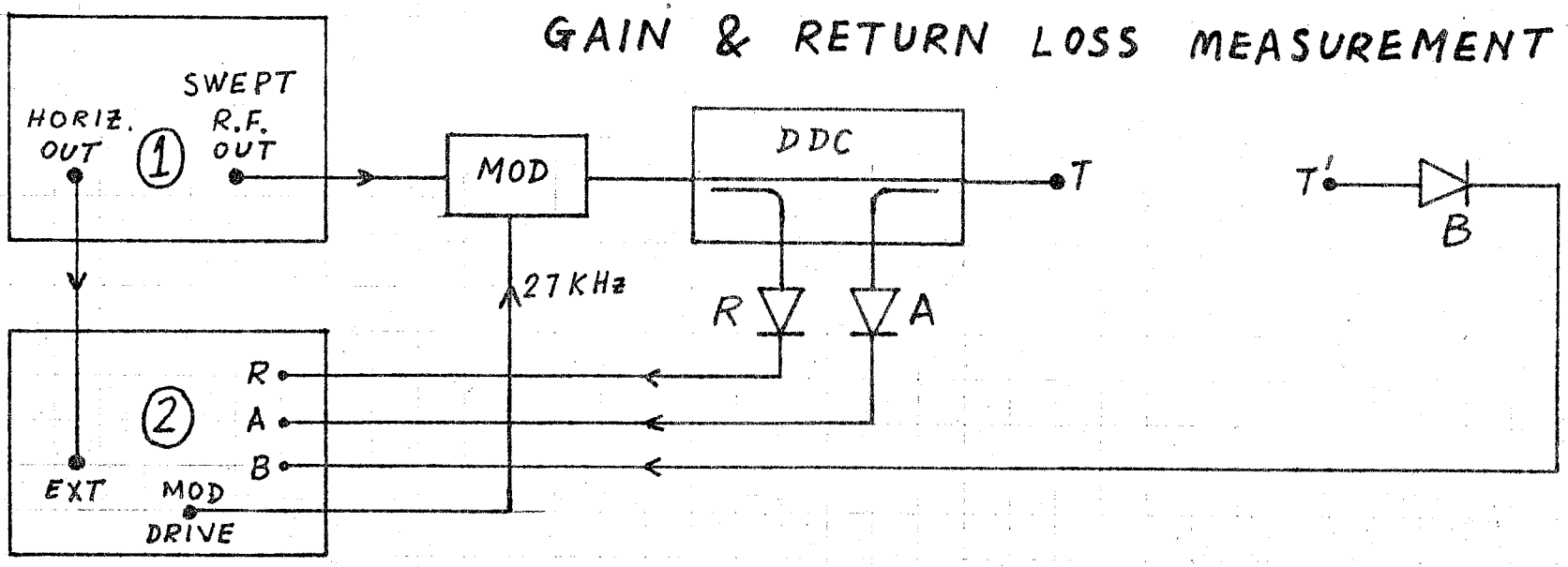
NOISE MEASUREMENT

T_D = DEVICE NOISE TEMPERATURE

$V_o \sim T_o + T_D$; $V_H \sim T_H + T_D$

$T_o = 300°K$ T_H KNOWN (1131°K FOR DIODE NOISE GEN. USED)

GAIN & RETURN LOSS MEASUREMENT



1 : Sweep oscillator — 4 Band, 0-2500 MHz

2 : Display-A/R, B/R vs. frequency

MOD = MODULATOR

→▷ = Square law detector

DDC = Dual Directional coupler.

R — Reference channel

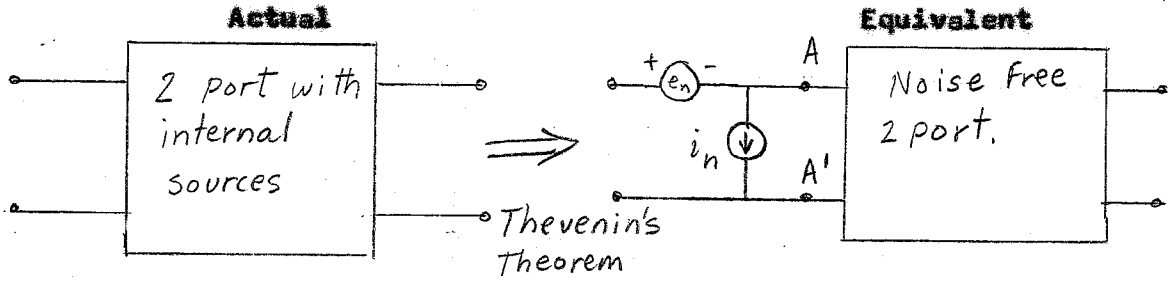
A — Reflected power, Calibrated by placing short at T

B — Transmitted power " by direct connection of T to T'

Device under test connected at T T'

APPENDIX - C

Noise Representation in 2-Ports:

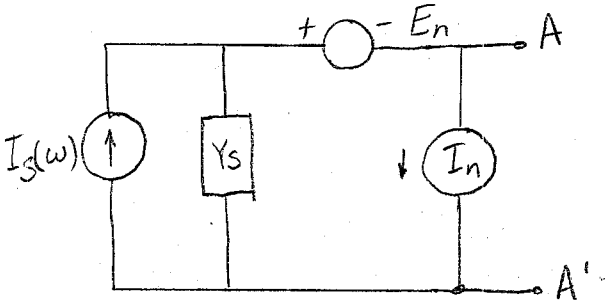


Using the Nyquist relation for rms quantities,

$\bar{e}_n^2 = 4 R_n k T_o \Delta f$; where R_n is an equivalentnoi noise resistance at standard temperature T_o, Δf is the band of interest.

and $\bar{i}_n^2 = 4 G_n k T_o \Delta f$; G_n = eq, noise conductance.

When the equivalent network is fed with a random noise current source $I_s(w)$ with internal impedance Y_s at temperature T_o , then noise output at A A' is found as follows:



E_n, I_n are Fourier Transforms of e_n , i_n; $Y_s = G_s + j B_s$

total short circuit output current = $I_s + I_n + Y_s E$, assuming the internal 2-port noise and the external I_s are uncorrected, squaring the fourier magnitudes, taking averages and using Parseval's theorem;

total mean square fluctuation $= \left|\overline{i_s^2}\right| + \left|\overline{i_n + Y_s e_n}\right|^2$

where bar denotes time average.

$$= \left|\overline{i_s^2}\right| + \left|\overline{i_n^2}\right| + \left|Y_s\right|^2 \cdot \overline{e_n^2} + Y_s^* \overline{i_n e_n^*} + Y_s \overline{i_n^* e_n}$$

Noise figure $= F = \dfrac{\text{Total output noise}}{\text{Contribution due to } Y_s \text{ alone.}}$

$$F = \frac{\left|\overline{i_s^2}\right| + \left|\overline{i_n + Y_s e_n}\right|^2}{\left|\overline{i_s^2}\right|} = 1 + \frac{\left|\overline{i_n + Y_s e_n}\right|^2}{\left|\overline{i_s^2}\right|} \quad \text{- Eqn. 1.}$$

Eqn. (1) can be simplified if i_n is split into a component perfectly correlated with e_n and an uncorrelated component, i_u.

Then $\overline{(i_n - i_u) \cdot i_u^*} = 0$ and $\overline{e_n \cdot i_u^*} = 0$ } at all frequencies.

The correlated component, $(i_n - i_u)$ may be expressed as $Y_r \cdot e_n$

where $Y_r = (G_r + jB_r)$ has the dimensions of admittance. $e_n i_n^*$

then $is = e_n (i_n - i_u)^* = Y_r^* \left|\overline{e_n^2}\right|$

Putting $\left|\overline{e_n^2}\right| = 4R_n kT_o \Delta f$; $\left|\overline{i_u^2}\right| = 4 G_u kT_o \Delta f$,

$$F = 1 + \frac{1}{4kT_o G_s \Delta f} \left[\overline{i_u^2} + \left|Y_s + Y_r\right|^2 \overline{e_n^2}\right]$$

$$= 1 + \frac{G_u}{G_s} + \frac{R_n}{G_s}\left[(G_s + G_r)^2 + (B_s + B_r)^2\right]$$

F has a minimum F_o at $G_o = \dfrac{G_u + R_n G_r^2}{R_n}$; $B_o = -B_r$

and

F for any arbitrary $Y_s = (G_s + jB_s)$ is then

$$F = F_o + \frac{R_n}{G_s}\left[(G_s - G_o)^2 + (B_s - B_o)^2\right]$$ in terms of the 4 parameters R_n, F_o G_o and B_o OR equivalently in terms of

$\overline{e}_n^2$ $\quad$ $\overline{i}_n^2$ $\quad$ $e_n i_n^*$

(complex, so 2 parameters)

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Vivek Dhawan.

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