

PROJECT REPORT ON

**TWO AXES MICRO POSITIONING CONTROLLER**

CARRIED OUT AT

**RADIO ASTRONOMY LAB  
RAMAN RESEARCH INSTITUTE  
BANGALORE**

UNDER THE ESTEEMED GUIDANCE OF  
**Mr. ANANTHASUBRAMANIAN  
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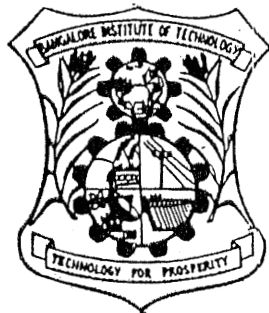
BY

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SUBMITTED TO BANGALORE UNIVERSITY IN PARTIAL FULFILLMENT  
FOR THE AWARD OF DEGREE OF

**BACHELOR OF ENGINEERING IN  
ELECTRONICS AND COMMUNICATION.**

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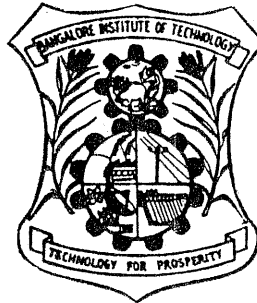


1996-97

**DEPARTMENT OF ELECTRONICS AND COMMUNICATION  
BANGALORE INSTITUTE OF TECHNOLOGY  
K.R.ROAD, BANGALORE-560004  
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION


# BANGALORE INSTITUTE OF TECHNOLOGY




## Certificate


*This is to certify that the project titled*  
**Two Axes Micro-positioning Controller**  
*has been successfully completed by the following students of final year*  
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*in partial fulfillment of requirements for the award of Bachelor Of Engineering*  
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*during the academic year 1996-97.*

*The project work was carried out at*  
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15 July 1997.

## Certificate

This is to certify that the project work entitled "*Two axes Micro-positioning Controller*" was carried out by **Pradeep S., M.R.Naveen** and **Navin Rajendran P.C.** in the Radio Astronomy Laboratory of the *Raman Research Institute*, Bangalore under my guidance for the partial fulfilment of the requirements for the award of *Bachelor of Engineering degree in Electronics and Communication* of the Bangalore University, Bangalore.

  
( **P.G. ANANTHASUBRAMANIAN** )  
ENGINEER.

*TWO AXES MICRO-POSITIONING  
CONTROLLER*

## **ACKNOWLEDGEMENTS**

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Our stay at the R.R.I. was a very enlightening one. We gained insight into the practical aspects of designing electronic circuits of a varied nature, and learnt a lot from the mistakes we had committed inadvertently. We spent so much time at the R.R.I. that it almost became our second home.

**PRADEEP S.**  
**NAVEEN M.R.**  
**NAVIN RAJENDRAN P.C.**

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# *Introduction*

## **INTRODUCTION**

### **1.1 Existing system :**

The mm. wave receiver used with the **10.4m mm-wave Telescope** in the R.R.I. uses a mechanically tunable **Wide-Band Gunn Oscillator** for the 1st down conversion of the R.F. signals in the frequency range 80 - 115 GHz.

The present system of setting the o/p frequency and power of the Gunn oscillator involves manual adjustment of the two micro-meters as per special charts that give the required readings of the  $\mu$ -meters for specific values of frequency and the corresponding values for peak power. A person who wishes to set a particular frequency of the Gunn oscillator has to manually turn the tuning the respective  $\mu$ -meter to the values in the chart.

### **1.2 Requirements:**

In general, each frequency setting on the Gunn oscillator has a corresponding position for peak power o/p . Eight such L.O.frequencies are commonly employed for the mm. wave observations using the radio telescope.

A control panel has to be provided such that an operator can

→ choose any of the 8 frequency and corresponding power settings.

→ start/stop the  $\mu$ -meters as and when required.

→ select any of the  $\mu$ -meters, change its direction and move it in discrete steps for minor adjustments.

When changing from one frequency setting to another in the pre-decided eight settings, the  $\mu$ -meters should automatically be set to the desired value of the frequency & power.



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A facility should be provided such that a P.C. can control the frequency & power settings from a remote location.

The power supply will be external to the modules made. The modules will be provided with the required on-board regulators.

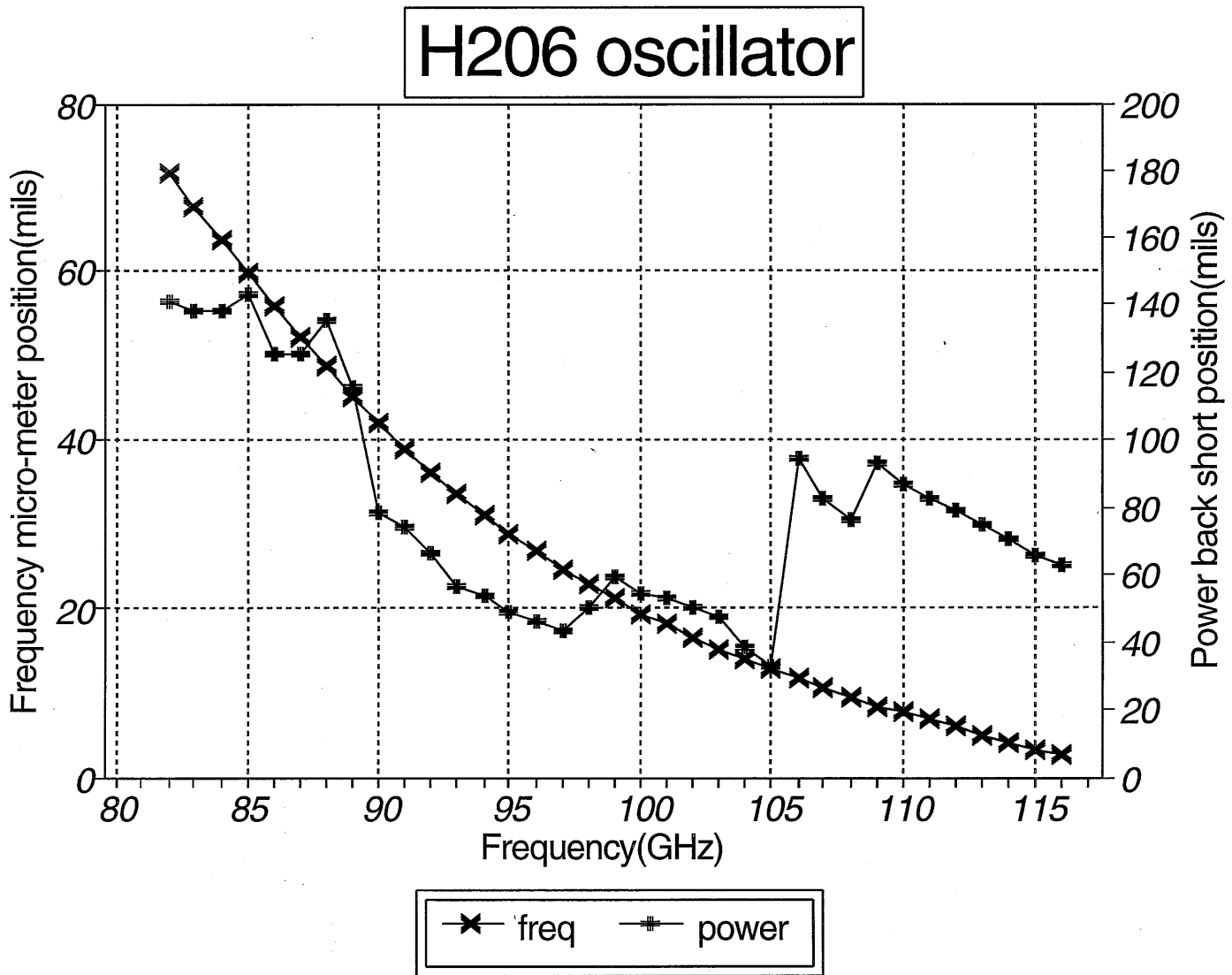
The design aim is to build a prototype module with minimum hardware and a micro-controller as the heart of the system.

### ***1.3 Brief Description of the project:***

A brief description of the project is provided with the help of four simple block diagrams.

The **micro-controller 8031** is the main control unit in this closed loop system which controls the position of the motors. The  $\mu$ -meters of the Gunn oscillator are coupled to the shaft of stepper motors which move in a direction determined by the micro-controller. Feedback potentiometers are also coupled to the shaft of the motor. The basic set up of the project is as shown in **Block Diagram 1**. For a position of the  $\mu$ -meter there exists a unique voltage on the feedback potentiometer. Therefore there will be eight different voltages corresponding to eight commonly used frequencies. These voltages are set on the reference potentiometers which when compared with the feedback potentiometer determines the direction of rotation required.

For example, from the plot of H206 oscillator, it can be seen that variation of the  $\mu$ - meter position is monotonous with regard to frequency but not with power. Hence, it is deduced that reference voltage settings represented by the codes are monotonic for frequency but not for power. So the codes themselves can determine the direction for the frequency motor but not for the power motor. The frequency  $\mu$ -meter(operated between 80 and 115GHz) has lesser number of turns than the power  $\mu$ -meter.



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The set up consists of two modules. The first module with a front panel has the facility to set reference voltages for frequency and power. The second has the following controls on the front panel.

- A switch labeled  $\overline{\text{LOCAL}}$  /REMOTE indicates the mode of operation. When the switch is in the position LOCAL, settings can be done from the front panel. If REMOTE mode is selected, all settings are done from a remote location, and the front panel has no effect on the movement of the  $\mu$ -meters.
- Three switches labeled  $S_2$ ,  $S_1$  and  $S_0$  are used to set the frequency to one of eight commonly used values. The required code may be set referring to a chart which specifies the code for the chosen frequency. The indication of the code is given by three LEDs placed above the switches.
- The START / STOP switch is to start or stop the motor.
- The  $\overline{\text{F/P}}$  switch which decides the motor to be used in case of fine movement.
- The DIR switch which specifies the direction of rotation, again used only for fine movement.
- Two independent switches to turn the motors ON/OFF.

The information regarding the switches is read into the controller. The controller checks the code and decides to perform either fine or coarse movement. In the case of coarse movement, i.e., when the code has changed, both  $\mu$ -meters are moved to the desired position. The fine movement is done if the code is the same, and decisions are made on the basis of the control switches.

Basically, a stepper motor is operated in full steps by providing digital signals to the windings, but by providing a sinusoidal signal to one phase and a 90 degree phase shifted signal to the other phase, *micro-stepping* is achieved. This increases the number of steps per revolution i.e., the resolution of the motor. In this application a 200 full step per revolution stepper motor is used in *micro-stepping* mode to provide a minimum of 3600 steps/revolution.

The sinusoidal signals are stored in look up tables and given sequentially to Digital-to-Analog Converters (DAC), the output of which is given to digitally controllable

## *Introduction*

drivers through Pulse Width Modulators. A set of control signals from the controller also decides the phase and direction of currents.

The two modules as described above are briefly described.

The three block diagrams shows the basic elements of the two modules.

**Block diagram 2** shows the various devices connected to the controller. The memory ( EPROM 27C64 ) is enabled using a decode logic based on the o/p of pins A13 and  $\overline{\text{PSEN}}$  of the controller. The same pins are used to enable a buffer which reads the control data as shown. The control data includes the following :

→ Information regarding Front panel switches

STA / STO ( start /stop the motor )

DIR ( change direction of rotation of the motor )

$\overline{\text{L}}$  / R ( Local or Remote mode of operation )

→ Status of Limit Switches

L1 (indicates if the freq.  $\mu$ meter has reached an extreme)

L2 (indicates if the power  $\mu$ meter has reached an extreme)

→ Status of Comparators.

CMP1 (status of freq. f/b pot compared with chosen reference)

CMP2 (status of power f/b pot compared with chosen reference)

→L0,L1 and L2 which are the code levels given to MUX to choose one of the eight reference voltages.

→Tx and Rx for serial transmission and reception through ICL 232.

→D0 - D4 are digital signals given to the DAC

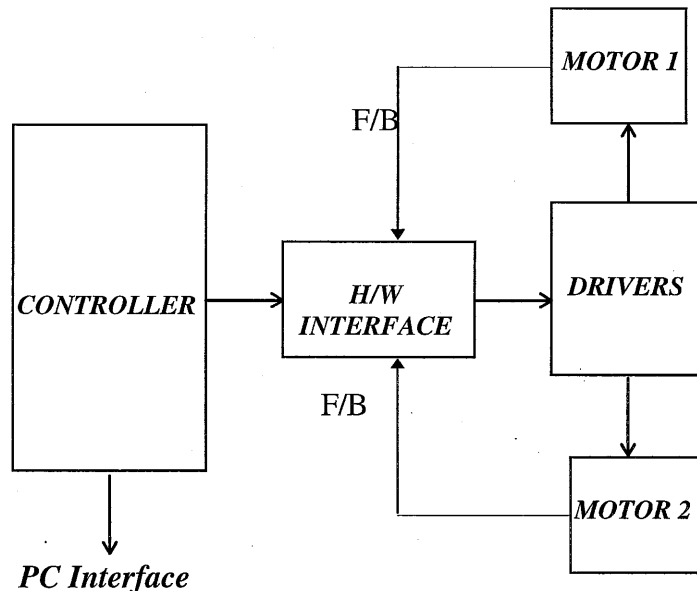
→SQ,LA,MO are signals to decide the motor, phase and direction of current.

→ENM1 and ENM2 are separate controls to enable/disable the two drivers.

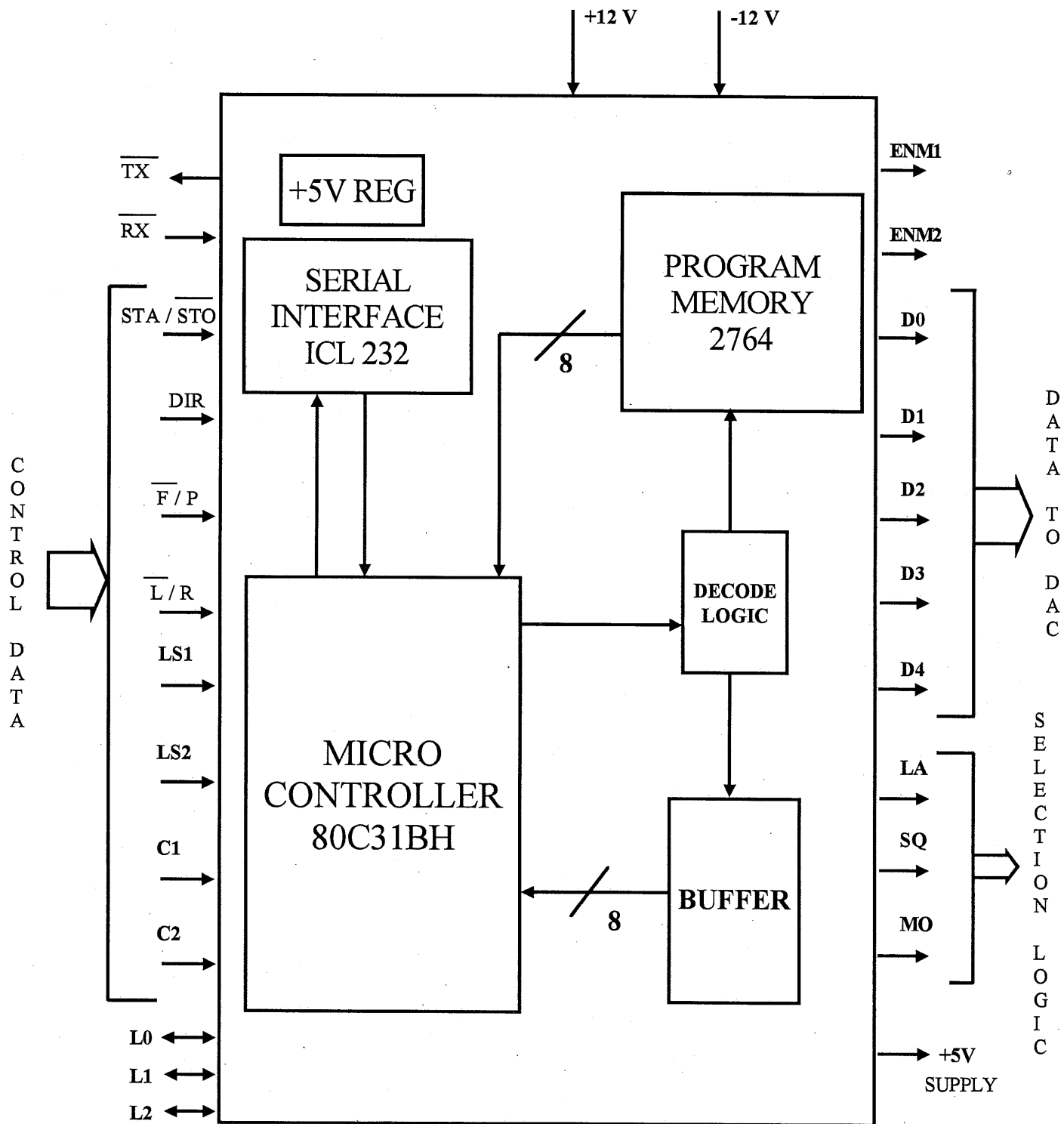
**Block diagram 3** shows a decode logic which decides the DAC based on SQ,LA and MO. The DAC output voltage is fed to a Pulse Width Modulator ( PWM ) which provides stable currents through the windings. The PWM o/p is fed to the stepper motor driver which consequently sends appropriate currents (M1A,M1B,M2A and M2B) to the motor windings to make the motor move in the proper direction. A **precision rectification** is used for **feedback** from the driver to the PWM ensures that the currents are stable.

**Block diagram 4** shows regulators, the reference pots(explained earlier), comparator and multiplexer. The supply to feedback pots are provided from here. The compared outputs CMP1 and CMP2 are given to the controller. A level shifter is provided to convert TTL logic to CMOS logic for the multiplexer.

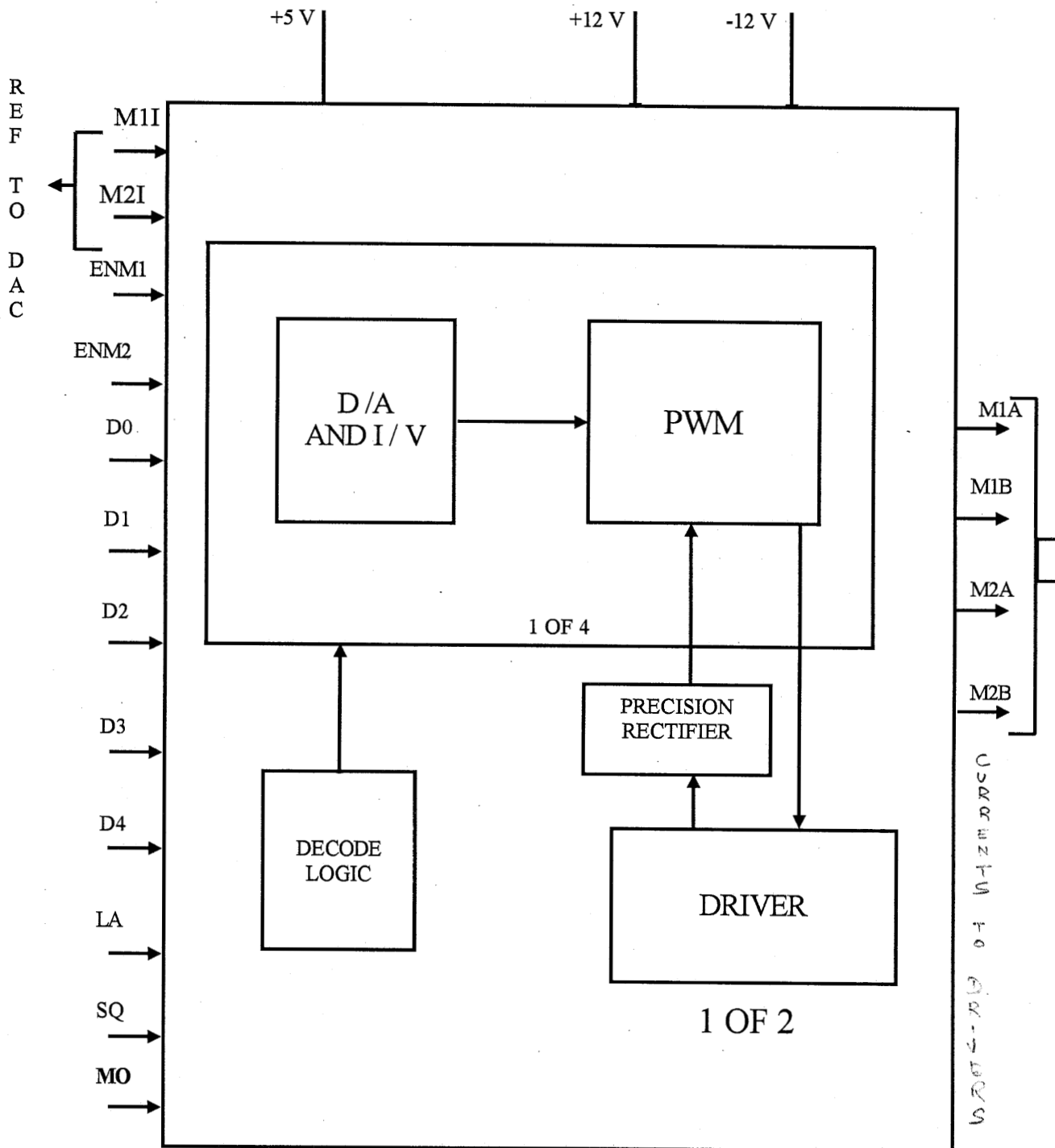
A detailed description of the hardware and their design and the software are provided in subsequent chapters.(The schematics are provided in the appendix)



Block diagram 1

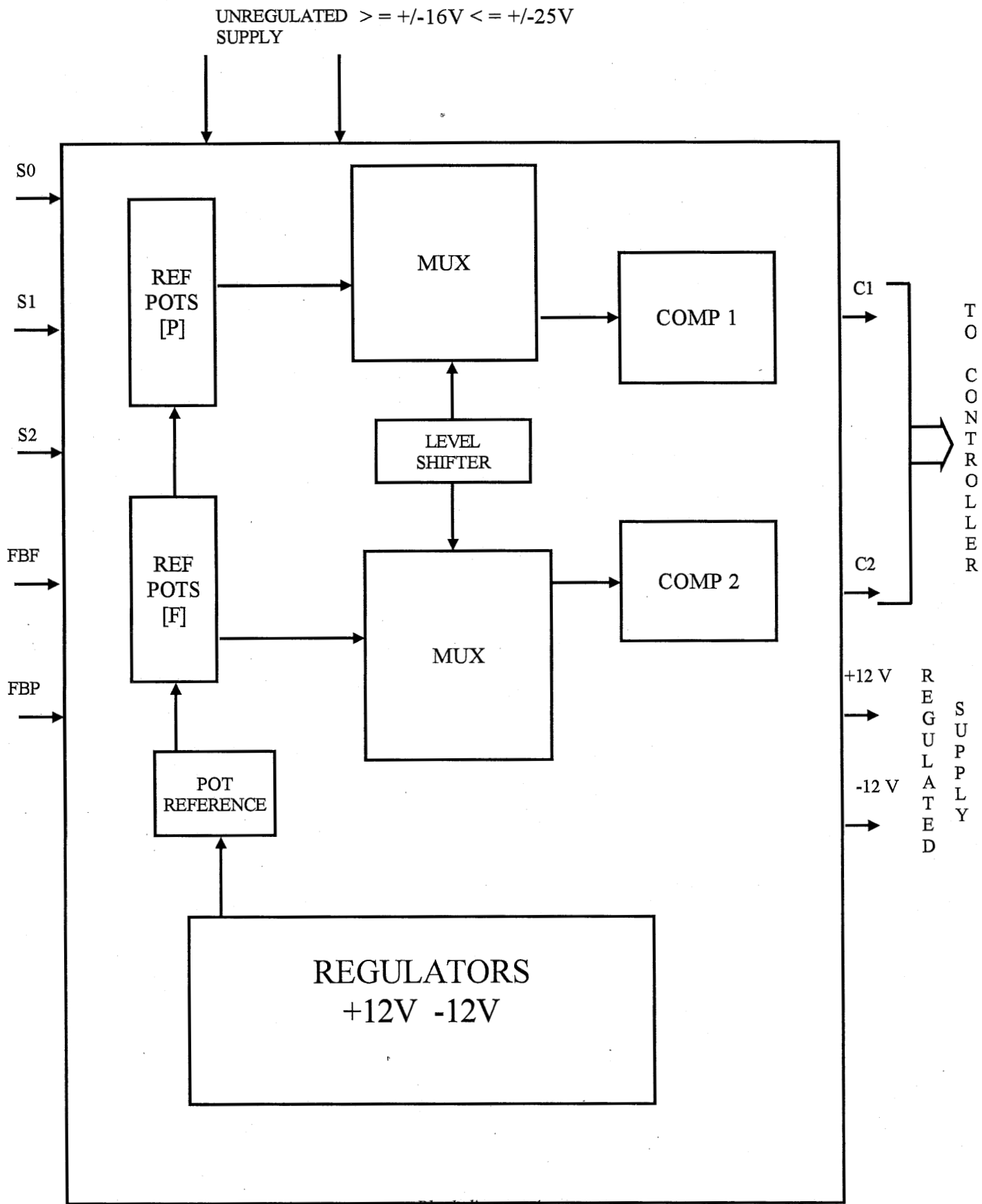


Block diagram 2



Block diagram 3

Introduction



Block diagram 4



*Hardware*

## **HARDWARE**

### **2.1 MICROCONTROLLER 80C31BH**

The **INTEL 80C31BH** is a stand-alone high-performance single-chip computer fabricated with INTEL's highly reliable +5V, depletion mode N-channel silicon gate **HMOS** technology and packaged in a 40-pin DIP. It provides the hardware features, architectural enhancements and new instructions that make it a powerful and cost-effective controller for applications requiring upto 64K bytes of program memory and up to 64K bytes of data storage. The controller also has direct bit-programmable features.

#### **Features:**

- 128x8 RAM
- Four 8-bit ports, 32 I/O lines
- Two 16-bit timer/event counters
- High performance full-duplex serial channel with unique addressing modes.
- External memory expandable to 128K
- Five source-two priority level nested interrupt structure
- On chip oscillator and clock circuits.

Internal memory address space is further divided into 256 byte internal data RAM and 128 byte Special Function Register(SFR) address spaces, 4 register banks, 128 addressable bits and stack residing in the internal data RAM. All registers except the program counter and the four 8-register banks reside in the Special Function Register space.

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These memory-mapped registers include the arithmetic register, pointers, I/O ports, interrupt system register, timers and serial port and special function registers. 128 bit locations in the SFR address space are bit-addressable.

### **I/O facilities:**

Each of the 32 pins are treated as 32 individually addressable bits and also as four parallel 8-bit ports addressable as **ports 0,1,2 and 3**.

**Port 0** : It is an 8 bit open drain bi-directional I/O port. It is also the multiplexed low order address and data bus when using external memory.

**Port 1** : It is an 8 bit quasi bi-directional I/O port. It is used for low order address byte during programming and verification.

**Port 2** : It is an 8 bit quasi bi-directional I/O port. It also emits the high order 8 bit address when accessing external memory. It is used for the high order address and control signals during programming and verification.

**Port 3** : It is an 8 bit quasi bi-directional I/O port. It also contains the interrupt, timer, serial port and  $\overline{RD}$  and  $\overline{WR}$ . The secondary functions assigned to the pins of port 3.

Ports 1 , 2 and 3 can be configured as i/p by writing a 1 into the corresponding bit latch in the port SFR . The bit latch clocks in a value from the internal bus in response to a **write to** latch signal from the CPU.

The level of the port pin itself is placed on the internal bus in response to a **read pin** signal.

Ports 1,2,3 when configured as i/p they pull high and will source current when pulled low.

The following table gives the secondary functions of the pins of port 3 and the assigned configuration as per our application.

PIN	SECONDARY FUNCTION	ASSIGNED CONFIGURATION
P3.1	Txd/clock	Txd-Serial port's transmitter data output(asynchronous)
P3.2	$\overline{\text{Int0}}$	Used as interrupt
P3.3	Int1	Bi-directional I/O pin for selection bit S0
P3.4	T0	Enabling of driver 1 ENA
P3.5	T1	Enabling of driver 2 ENB
P3.6	$\overline{\text{WR}}$	Bi-directional I/O pin for selection bit S2
P3.7	$\overline{\text{RD}}$	Bi-directional I/O pin for selection bit S1

Table-1

A 12MHz crystal is connected across XTAL1 and XTAL2 which are the input and output of the oscillator high-gain amplifier respectively. The crystal circuit is given as per the micro-controller specifications. On power-ON, a **RESET** of 10msec is provided.

### 2.1.a CONTROL WORD:

CONTROL WORD is the data byte which gives certain information to the controller(shown in the table).This is the main data byte based on which the controller performs various operations. The CONTROL WORD is accessed as a external program memory via a buffer(74HCT244) by setting pin A13. In order to differentiate between memory and buffer a decode logic is provided. The instruction to access external Program memory(MOVC) is used here.

A13	$\overline{\text{PSEN}}$	Control provided
0	1	Memory is enabled
1	1	Control word buffer is enabled

Table-2

**Control Word Description :**

CW.0	<b>START/STOP</b>	To start/stop the motor
CW.1	$\overline{\text{F/P}}$	To select frequency/power motor
CW.2	<b>DIR</b>	To select direction of motor movement in FINE mode
CW.3	$\overline{\text{L/R}}$	To select LOCAL/REMOTE mode of operation
CW.4	<b>LS1</b>	Status of limit switch of motor1
CW.5	<b>LS2</b>	Status of limit switch of motor2
CW.6	<b>CMP1</b>	Output of comparator 1 ( Frequency )
CW.7	<b>CMP2</b>	Output of comparator 2 ( Power )

Table-3

**2.1.b FRONT PANEL**

The front panel is as shown in the picture(Appendix). It consists of the three codes  $S_0$ ,  $S_1$  and  $S_2$  which are configured as shown from table 1, and the four bits of the Control word(START/STOP,  $\overline{\text{F/P}}$ , DIR and  $\overline{\text{L/R}}$ ) as shown in table 2. The wiring of the switches is as shown in the **schematic diagram 2 of 5**. The code switches are read only in the LOCAL mode and the controller sets the codes in the REMOTE mode. The switches are hence enabled only in the LOCAL position of  $\overline{\text{L/R}}$  switch. These switches should not affect the input to the level shifter and should not interfere with the each other when switched to REMOTE. In order to prevent any such interference, diodes are used for isolation between themselves , i.e., they are disabled when the  $\overline{\text{L/R}}$  is in REMOTE position.

## **2.2 MEMORY**

### **EPROM 27C64:**

**27C64** is a single 5V, 64K ultra-violet erasable and electrically programmable memory[EPR0M]. It has an access time of 250ns which is compatible to high performance microprocessor and micro-controller applications. HMOS-E technology is used, which is a high speed **N-channel MOS** Silicon Gate technology.

An important feature is that it has a separate output control  $\overline{OE}$  and chip enable  $\overline{CE}$ . The output enable eliminates bus contention in multiple bus micro processor systems. It has a stand-by mode which reduces power dissipation without increasing access time. This is done by applying a **TTL** high signal to the  $\overline{CE}$  input.

The five modes of operation of the memory are Read, Standby, Program, Program Verify and Program Inhibit.

**Read mode:** It has two control functions both of which must be logically satisfied to obtain data at the outputs.  $\overline{CE}$  is the power control and should be used for device selection Data is available at the outputs after the falling edge of  $\overline{OE}$ .

It is accessed using address pin13(**A13**) which is connected to  $\overline{OE}$  and  $\overline{PSEN}$  which enables the chip( $\overline{CE}$ ).

The lower address byte is latched by **74HCT573**, enabled by **ALE** from the micro-controller.

The total memory space utilized by the program is around **2KB**. Since it is less than 4Kbytes, a controller of the same family with in-built memory **87C51** (with a 4K internal program memory ) may be used. But the advantage here is that the memory may be removed when it is required to re-program repeatedly, rather than removing the controller itself. It also provides an expansion facility.

### 2.3 DIGITAL TO ANALOG CONVERTER

Digital to Analog Conversion is done by **DAC-0800** which is a monolithic 8-bit high speed current-output DAC with a settling time of 100ns. Power dissipation is very low(33mW) with +/- 12V supplies and is independent of the logic states. An important feature of the DAC0800 is that it can be interfaced directly with TTL, CMOS, PMOS and others. Complementary current outputs are available.

#### DATA BYTE:

The control & data signals from micro-controller is a byte where 3 bits are for selection of the latches for the respective motors and the other 5-bit digital data represents the Reference current to be converted to analog signals with a **digital to analog converter** ( DAC ). Since 5 bits are used, 32 levels (  $2^5$  ) may be obtained. For micro-stepping, the currents in the windings are *sinusoidal*, i.e., as current increases sinusoidally in one winding, it decreases sinusoidally in the other. The sine waveform ( 0-90 deg ) is converted to 5-bit digital data using the relationship given below.

given below

$$\sin\left[\frac{k \times 90}{31}\right] \times 31 = \text{CODE}$$

where k varies from 0 to 31 and CODE is the nearest Hexadecimal value of the decimal value obtained from the L.H.S. Since there are 32 levels it corresponds to 6400 steps/revolution which is greater than the requirement of 3600 steps/rev. These values are then **ORed** with the 3 bits SQ, LA, MO and stored in different look-up tables. There will be 64 bytes each for A, (2 for sine w/f and 2 for cosine w/f )resulting in a total of 512 bytes of data in the look-up tables for the two motors. The motor can thus be moved by just giving out these data to the DAC at a predetermined rate. For coarse movement, a speed of 40Hz is employed.

## **Hardware**

Here, the motor stops depending on the code or using the stop switch. It is also operated in fine mode at 1Hz where manual stopping is required.

### **Description:**

DB.5 SQ Determines direction of current flow in the motor winding.

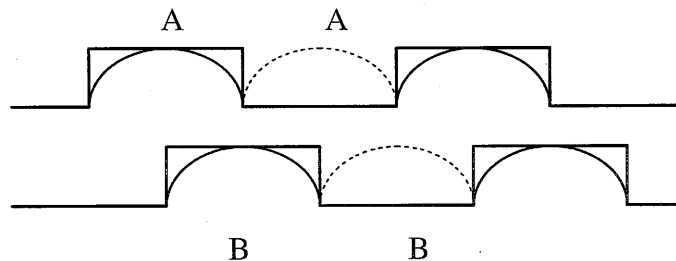
DB.6 LA Chooses the latch (phase A / B)

DB.7 MO Selects the motor (freq. / power)

Five bit Data is latched by decoding these 3 bits to hold the motor in position till next data is given.

### **LOGIC FOR SELECTION OF LATCHES AND SEQUENCE:**

The sequence in which the various latches are to be selected is determined by the 3 most significant bits in the data byte. The MSB (**MO**) signifies the motor to be enabled. The next bit (**LA**) in combination with MO determines the latch to be selected by the decoder **74HCT238**. The combination of bits for selecting latch and sequence is as shown in Table 4. The data is sent to the two latches (one corresponding to sine w/f other corresponding to cosine w/f as shown in diagram below) one after the other. Since the latch holds the data which was at its i/p at the time of it being disabled, the data for one latch may go into the other resulting in glitches of about 1  $\mu$ sec duration. To overcome this, a delay is introduced at the o/p of the controller by using a **RC FILTER**. Further this problem is also taken care in software by disabling the 1st latch before the 2nd latch is enabled.



*Figure 2.31*



## Hardware

Direction of flow of current through the windings of the motors is determined by the sequence bit ( **SQ** ) (as shown by the thick line)

MO	LA	SQ	LATCH ENABLED	MOTOR	SEQUENCE
0	0	0	LATCH 1	1	A
0	0	1	LATCH 1	1	$\overline{A}$
0	1	0	LATCH 2	1	B
0	1	1	LATCH 2	1	$\overline{B}$
1	0	0	LATCH 3	2	A
1	0	1	LATCH 3	2	$\overline{A}$
1	1	0	LATCH 4	2	B
1	1	1	LATCH 4	2	$\overline{B}$

Table 4

### Design:

The reference voltage for the DAC is +10V.

The supply voltages are +/-12V.

The full-scale analog o/p voltage for 5 bits is 1V(which is the maximum reference voltage to the PWM).

### Design equations

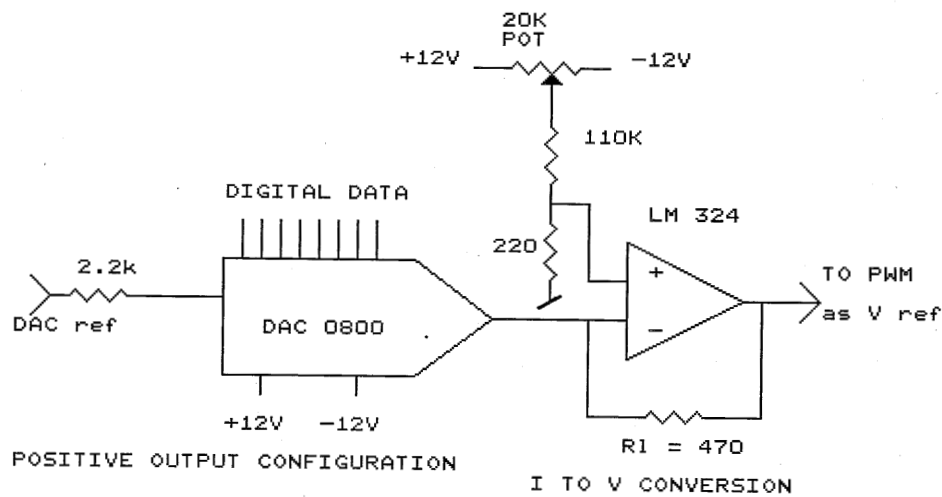
$$I = I_0 + \overline{I_0}$$

$$I = \frac{V_{ref}}{R_{ref}} \times \frac{31}{256} = \frac{1V}{R_L} \quad \text{where } R_L = 4.13K\Omega \text{ and } R_{ref} = 5K\Omega$$

The o/p current is converted to a proportional voltage using LM324(as current-to-voltage converter).

An offset-correction circuit is provided to the +ve terminal of the LM324 as shown in the **schematic diagram 3 of 5**. LM324 has a maximum offset of +/- 7mV(max).

The correction is provided by varying the 20KΩ pot which provides adjustment up to 24mV. The correction is made by maintaining the data to the DAC as 0 and varying the pot to obtain a zero output at the PWM. This can be easily done by operating the motor in **fine movement** mode. The gain of the PWM also affects this, as a very high gain provides a non-zero output due to extremely small changes at the input.



## **2.4 PULSE WIDTH MODULATOR**

The IC **TL494** is used to control the current through motor windings.

### **Features:**

- fixed frequency PWM control circuit designed for switch mode power supply control
- on chip oscillator
- on chip error amplifier
- output transistors rated at 500mA source or sink

The TL494 is used to provide a stable current in the windings of the motor as small changes in the current changes the position of the motor. The current stability is better in a linear regulator, but in a chopper, the power efficiency is better, with a good current stability. The output of the PWM is compatible to the TTL logic levels, making it easy to control the driver. Four such modulators are used, one for each winding of the two motors.

The output of the DAC is given as the reference voltage to the error amplifier. The current in the driver is sensed (by a sense resistor) and fed to the error amplifier to generate the PWM o/p in the proper sense.

When the f/b voltage from the sense resistor is greater than the reference voltage (from DAC) to the error amplifier of the PWM duty cycle of the PWM decreases. Similarly when the f/b voltage is lesser, duty cycle increases. When the motor has been latched to a particular position, the PWM helps in maintaining a constant average output voltage by correcting errors and varying the duty cycle at the output depending on the feedback.

The response of the PWM also depends on the gain of the error amplifiers. Very high gain makes it to respond to small changes at the reference of the feedback making the output unstable. So an optimum gain is to be designed. Further a suitable series RC element is added to the F/B of the error amplifier to reduce the noise in the motor.

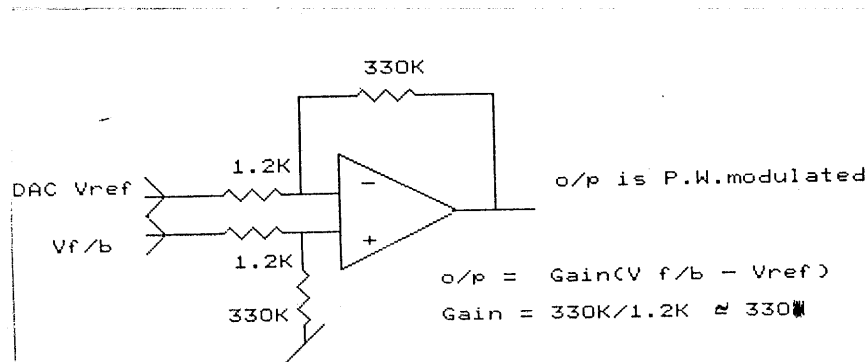
**Design:**

- One of the error amplifiers is disabled.
- The output transistors of TL494 are used in parallel to provide current to the driver.
- Dead time control and output control pins are disabled.
- The modulator is operated at 25KHz .The  $R_T$  and  $C_T$  are suitably selected by using the formula -

$$F_{osc} \approx \frac{1.1}{R_T \cdot C_T}$$

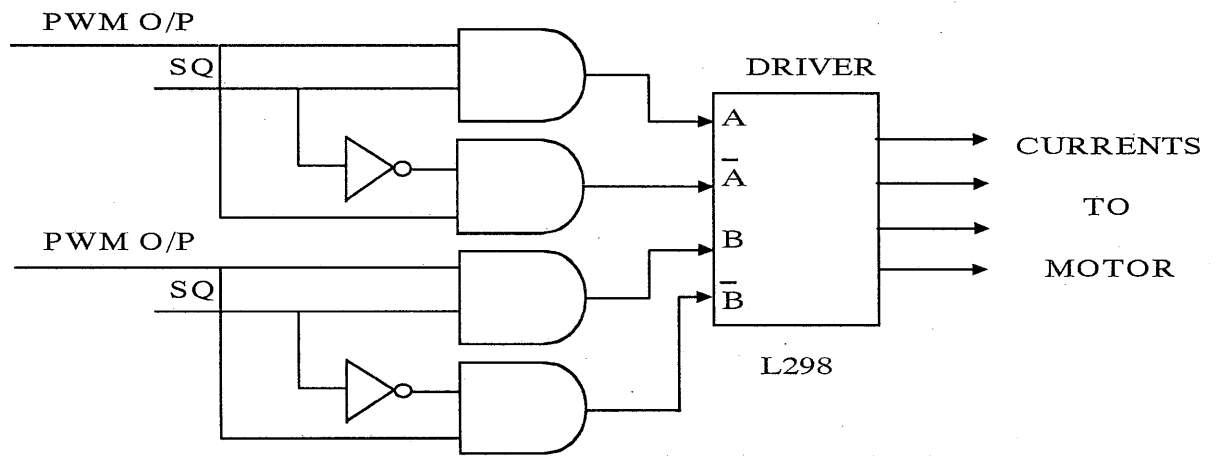
Assuming  $C_T=10$  KpF, we get  $R_T= 4.7K\Omega$

**Error Amplifier Design:**



*Figure 2.4.1*

The output along with SQ(as shown below) is fed to the driver through a digital circuit which decides the direction of current.



## **2.5 DRIVER**

A digitally controllable driver is used to control the direction and the magnitude of the current in the windings. The driver used in this application is the Dual Full-Bridge Driver **L298**. It is a power integrated circuit usable for driving resistive and inductive loads. This device has four push-pull drivers with separate logic inputs and two enable inputs. Each driver is capable of driving loads up to 2A continuously. The maximum operating voltage for the driver is 50V.

The emitters of the low-side power drivers are separately available for current sensing. Feedback from the emitters can be used to control load current in a switching mode or to detect load faults.

Separate logic and load supply lines are provided to reduce total IC power consumption. It is further reduced when enable inputs are low.

Two such drivers are employed, one for each motor. Each full bridge has one phase winding(inductive load) of the motor as the load i.e., A or B. The drivers are enabled by ENA and ENB for frequency and power motors respectively.

### **Design:**

Power supply given = 20V

As mentioned earlier the full scale voltage to a winding is 1V. If a full scale current of 330mA is desired in each winding, high wattage sensing resistors of  $3.3\Omega$  each is used.

A single heat sink is provided for both the drivers.

The current is passed through the windings by turning on a pair of diagonally opposite transistors. As mentioned before, the PWM o/p along with SQ signal is used to turn ON the appropriate pair of transistors(Q1,Q4 or Q2,Q3) to change the direction of the current, as shown in the **fig. 2.5.1**(shows the circuit for one of the 2 windings). Flywheel diodes provided across the transistors are required to maintain the direction of the current in the inductive load when the transistors are switched at a high speed by the control from the PWM.

The voltage across the sensing resistance connected to the drivers changes polarity. It has to be rectified before feeding it to the PWM error amplifier. Since the amplitude of

the sensed voltages are very low, high precision rectification is required. LF347, a quad high-speed JFET operational amplifier.

This is done by the rectifier as shown in fig.2.5.2

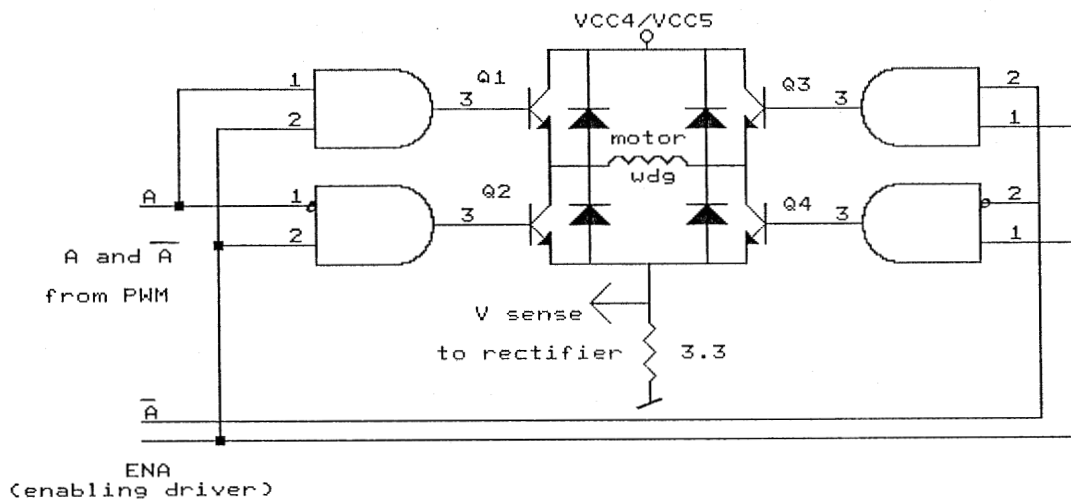


Figure 2.5.1 Internal structure of L298(1 of 2)

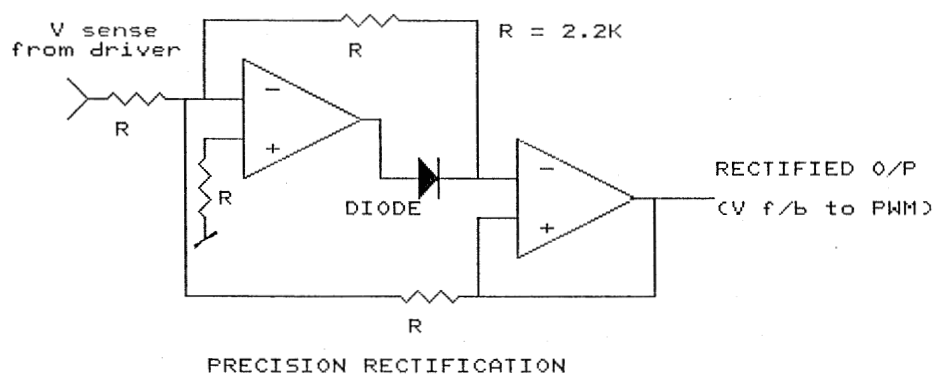


Figure 2.5.2

## 2.6 STEPPER MOTOR:

Stepper motors are used to vary the position of the  $\mu$ -meters. This is done by coupling the motor shaft to the  $\mu$ -meter. The available stepper motor is **HY200-1713-033BC** from **SGST** which is a 2-phase motor with 200 full steps.

This particular motor will require a driver with voltage and current rating of about 15V and 330 mA per phase. Also to be noted is the fact that 200 steps/rev stepper motors are *commonly available* in the market.

From the frequency and power position charts for three Gunn oscillators, we find that for a 1GHz change in frequency, a minimum rotation of 0.7 mils is required at the highest frequency. In our application, a resolution of 10MHz is required, which corresponds to a rotation of 0.007 mils.

1 rotation corresponds to 25 mils  $\rightarrow$  200 full steps

0.007 mils  $\rightarrow$  1/18 of a full step

Therefore the stepper motor has to be used in  $\mu$ -stepping mode resulting in a minimum of 3600 steps per revolution. Five bits are used provide signals to the driver. So a total of 32 microsteps may be obtained in one full step. A total of 6400 micro steps per revolution is obtained which is greater than the requirement.

This motor has six leads and two phases(as shown in data sheet). Each phase has two windings in series. Either of the windings may be used with the common lead, or both the windings in series. In this application only one winding has been used in order to reduce the current drawn. If both were to be used, the supply voltage has to be increased from 16V to a greater value.

A DC motor with gears would have served the purpose but since it had to be imported, a stepper motor is suitably used.

## **2.7 ANALOG MULTIPLEXER**

**MC 14051 BCP** is a 8-to-1 analog multiplexer (MUX) and works on a supply between 3V to 18V, with I/P voltage any where between -0.5V to  $V_{DD}+0.5V$ .

14051 has better isolation between switches (typically 80 dB), with a quiescent current of 5nA and O/P voltage ratio (high on/off) of 65dB (typical).

It is used to select the appropriate voltage settings corresponding to different frequency/power positions. Two MUXs are used with a common control i.e., one of the eight analog voltages are selected using S0, S1 and S2. The MUXs are kept permanently enabled (the inhibit pin is permanently disabled by grounding it).

The input to the MUX should be less than the supply voltages. Since inputs from the potentiometers range up to 10V, a +12V supply is provided. S0, S1 and S2 are level-shifted from TTL to CMOS using transistors to make it compatible with the supply voltage of the MUX. (A CMOS HIGH  $> 2/3 V_{CC}$  and CMOS LOW  $< 1/3 V_{CC}$ ).

### **2.7.a LEVEL SHIFTER**

Transistor **2N 2222** is used to shift the level of the code provided to the MUX from the switches as well as from the micro-controller. Supply to the transistor is +12V. The MUX requires a minimum voltage of 8V to recognize a logic HIGH. The LED used to denote the position of the code switch requires a current of 5mA to turn on, and hence the resistor used at the collector of the transistor is 1.5K $\Omega$  i.e.

$R = \frac{12V - 8V}{5mA} \cong 1.5K\Omega$ . The transistor used has a  $h_{fe}$  of 100 to provide a current of

5mA at the collector. For the LED to turn on, the base current should be 50 $\mu$ A.



The base of the transistor is connected to the micro-controller , the minimum logic HIGH voltage from the controller is 2.5V. Hence, for the base current to be 50 $\mu$ A, a 33K $\Omega$  resistor is used, taking into account the 0.7V drop at the transistor, i.e.

$$R = \frac{2.5V - 0.7V}{50\mu A} = 33K\Omega$$

The code switches are connected to the controller through a 3K $\Omega$  resistor. This is to provide appropriate voltages ( logic HIGH ( min ) =2.5V, logic LOW (max) = 0.7V ) at the controller pins and also to provide appropriate current ( 50  $\mu$ A ) to the base of the transistor to turn on the LED at the collector when the switch is in the ON position (logic HIGH). A HIGH at the i/p of the level shifter appears as a LOW at the o/p, and vice-versa, because the transistor acts as an inverter. Due to this, the order of selection of the reference pots is inter-changed.

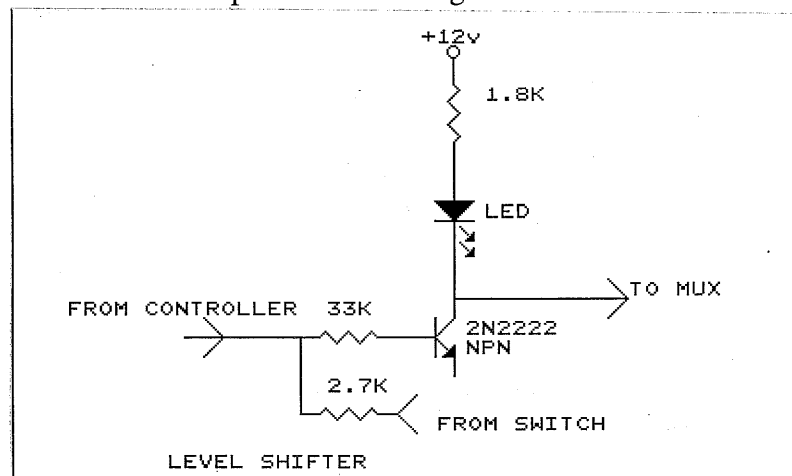


Figure 2.7.1

The output of the MUX is given to the comparator(inverting terminal). **LM339** is the comparator used. These are high-precision comparators which eliminates the need for dual supplies and are compatible with all logics. The selected voltage is compared with the voltage from the feedback potentiometers coupled to the motors. This voltage represents the instantaneous position of the motor. The comparator output (to be more precise, the transition from one logic level to another) is given to the micro-controller(CW.6 and CW.7) through pull-up resistors.

There are eight reference pots for motor 1. The voltage on each pot corresponds to one of eight frequently used values of frequency in the Gunn oscillator.

A similar set of voltage levels are adjusted for the eight pots corresponding to motor 2. Each voltage selects a particular power for the oscillator. The signals of each frequency have to have a pre-determined power, and so the frequency and power of the signals have to be simultaneously set to the desired value.

The values of  $S_0$ ,  $S_1$  and  $S_2$  determine the reference pot selected as the output of the MUX. This o/p is continuously compared with the varying voltage from the feedback potentiometer, and when the feedback voltage equals the reference voltage, there is a transition of logic level (  $H \rightarrow L$  or  $L \rightarrow H$  ) at the comparator o/p which is being monitored by the micro-controller. When such a transition is detected, the controller freezes all data to the DACs and as a result, the motor currents are stabilized (remains constant) . The motor is then fixed at the present position , setting the oscillator to the required frequency / power.

### **2.7.b INDICATORS :**

There are five LEDs on the main board. Three of them indicate the status of the code pins  $S_2$ ,  $S_1$  and  $S_0$ . The other two indicate whether the two motors are on or off. A special feature included in the software is to indicate when the motor has stopped moving, either after being set to the desired position ( after doing coarse movement ) or after the motor has been manually stopped ( while doing fine movement, and the **START/STOP** bit is made LOW ). The indication is given by making the code **LEDs** blink for a short duration ( 10 seconds ).

**NOTE:** Since the blinking is generated by toggling the inputs to the transistors used for level-shifting, if the code happens to be (0,0,0) , the i/ps are permanently LOW as seen from *figure 2.7.1* and hence the LEDs do not blink.

## **2.8 POWER SUPPLY REQUIREMENTS:**

The unregulated supply given is +/- 16V. These voltages are regulated by ICs **7812** and **7912** to provide +/- 12V. A 5V regulated supply is obtained in the second PCB using IC 7805. On the 1<sup>st</sup> PCB, a reference voltage generator **AD581** is used, to get a stable reference voltage of 10V .

The current drawn by the PCBs from the +12V supply is around 175mA, and from the -12V supply it is around 50mA

The current drawn by the +5V regulator (7805) alone, on the 2<sup>nd</sup> PCB is around 75mA. The power dissipation in the regulator is reduced by connecting a resistor in series, the value of which is chosen to be 82  $\Omega$  ( 1W )such that 8V appears at the i/p of the regulator. Suitable heat sinks are provided for all the regulators.

Since the entire system is powered ON always, to reduce the power consumption, **HCT** ICs are used.

## **2.9 REFERENCE DESIGN:**

The maximum current that can be drawn from the reference AD581 is 10mA. This current is not sufficient for the various references required. Suitable buffers (LM324) limit the current to 5mA and also provide appropriate voltages to various devices as mentioned below.

**DAC** : 4 DACs are used . These require a current of 2mA and a voltage between 0 and 10V. Hence a 5K $\Omega$  pot is used at the i/p of the LM324 .

**2 F/B POTS (FREQ/POWER):** The f/b POTS require supply of 10V and current of 1mA each , to provide good resolution to sense the voltage change with each micro-step . Hence, 10K $\Omega$  pots are used.

**16 REFERENCE VOLTAGE POTS (8 -FREQ, 8-POWER):** Each of the POTS used for setting reference voltages for selecting different frequencies require a current of 1.6mA and a voltage between 0-10V. Hence, a pot of 5K $\Omega$  is used at the i/p of the LM324 .

The pots used for setting voltages for selecting different power values corresponding to each frequency setting require a current of 1.6mA and a voltage of 10V each.

The power  $\mu$ -meter has more number of turns than the frequency  $\mu$ -meter. So the range of reference voltages is greater. Hence higher value potentiometers of 50K $\Omega$  are used.

## 2.10 INTERRUPT CONTROL :

Limit switches are provided to indicate if the  $\mu$ -meters have reached their extreme position. The configuration for this is as shown in the **schematic diagram**. Here, when the  $\mu$ -meter reaches its limit, the **limit switch** will be hit. The controller will be interrupted when the limit switch is hit, OR when the fuse blows after an excess current flow due to a fault. This in turn results in an interrupt subroutine being executed to disable the drivers. The status of the two limit switches ( freq. motor / power motor ) is also available to the controller through the control word , based on which appropriate action can be taken i.e., two bits are assigned to indicate the status of each  $\mu$ -meter. These bits are cleared when the corresponding motor has reached its limit .

### Interrupt circuit design:

To provide a voltage of 3V at the i/p of the NAND gate, a voltage divider circuit is provided, as shown by the figure. To provide a current of 5mA to the LED, a resistor of value  $2.7K\Omega$  is connected in series with the LED.

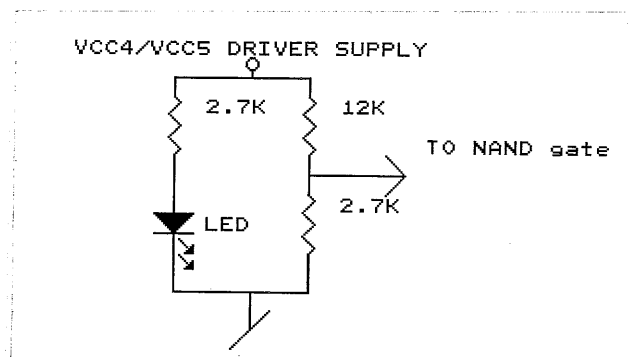


Figure 2.10.1

## **2.11 SERIAL COMMUNICATION:**

When the two motors are to be operated from a distant location, say from a P.C. , the L/R pin is maintained at HIGH. A separate program is run from the P.C. side to do the following:

- a) Set up the required baud rate
- b) Send data serially to the  $\mu$ -controller to set frequency or power
- c) Send or receive acknowledgement to/from the controller

Similarly, at the controller side, when the L/R pin is HIGH, a routine monitors the data at the serial pin **Rx** of the controller, and suitably processes it to make the necessary changes, i.e. set frequency/ power as desired, or send an acknowledgement signal back to the P.C.

The baud rate to be used for transmission is to be specified by setting up a counter (timer 1) in auto-reload mode with a specific count corresponding to the baud rate required. The baud rate used in our application is 9600 baud (bits per sec ) . For this purpose, all timer interrupts have to be disabled.

If the control system is running in the LOCAL mode, with  $\bar{L}/R$  pin at LOW, and if a remote P.C. tries to access the  $\mu$ -controller, *the serial interrupt* of the 8031 is activated, and the controller then performs an interrupt service routine which sends a message to the P.C. that the controller is currently being used in the LOCAL mode and cannot be accessed by the P.C.

### **2.11.a SERIAL INTERFACE:**

Serial communication with a PC for remote mode of operation is performed using the **in-built UART**. Rxd and Txd levels are shifted to RS-232 interface standard with the help of a chip **ICL 232**.

#### **Chip details:**

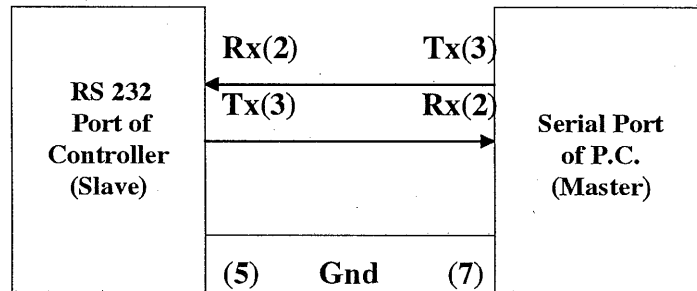
**ICL 232** is a dual **RS-232** transmitter/receiver interface circuit that meets EIA RS-232 specifications with TTL / CMOS compatibility and low power consumption.

The logic levels may be shifted between

logic 1 → -12V

logic 0 → +12V

The serial interface may be schematically represented as shown.



Serial port of P.C.(COM1/COM2) may be used. This may also be implemented in **Daisy Chain** mode where the master accesses several slaves each with a different address, where the controller may be one of them. Suitable settings are made in the system **BIOS** for communication.

The **UART** in the **μ-controller** can be operated in different modes:

Mode 0: 8 data bits at fixed baud rate

Mode 1: 10 bits ( 8 data + 1 start + 1 stop) at variable baud rate

Mode 2: 11 bits( 8 data + 1 start + 1 stop + 1 programmable bit ) at fixed baud rate.

Mode 3: 11 bits ( 8 data + 1 start + 1 stop + 1 programmable bit ) at variable baud rate.

**Mode 1** and **Mode 3** is used in this application so as to use the variable baud rate. Mode 3 has a programmable 9<sup>th</sup> bit. The 9<sup>th</sup> bit may be used to indicate whether the byte is an address byte or a data byte. The 9<sup>th</sup> bit is set to '1' by setting the bit **TB8** in the **SCON** register. **RB8** corresponds to ninth received bit.

9<sup>th</sup> bit is '1' → Address byte

9<sup>th</sup> bit is '0' → Data byte

## **2.12 HARDWARE CORRECTIONS:**

1. In the PCB, the bit positions had been reversed by mistake. Since the lower 3 bits of the DAC were shorted to ground, the data byte provided to the DAC from the controller was changed ( by modifications in the software ) in such a way as to keep the byte unaltered as seen from the DAC .

The full-scale voltage at the output of the DAC had to be scaled down to the design value of 1V, for which the value of the resistor  $R_L$  was re-designed as shown below.

$$I = \frac{5V}{2.2k\Omega} \times \frac{255}{256} = \frac{1V}{470\Omega} \quad \text{Where } R_{ref} = 2.2K\Omega$$
$$R_L = 470\Omega$$

2. One of the error amplifiers of the PWM had to be disabled by giving the reference o/p ( pin 14 ) of PWM to it's inverting terminal ( pin 15). Instead, it was connected to non-inverting terminal ( pin 16 ) . This was corrected on the board as desired.

3. The path AD0 was missing on the PCB . An external link is provided .



*Software*

## **SOFTWARE:**

The software includes writing an assembly language program for the **8031** micro controller and C++ programming at the PC end for serial communication.

The *Assembly Language Program* (A.L.P.) is explained with flow charts.

### **3.1 Program Description:**

In the main program, the control word along with the code settings is read and stored in the beginning and depending on the position of the LOCAL / REMOTE switch ( LOW / HIGH ), the program jumps to **local** or **remote** routines. In the LOCAL routine, no action is taken till the START / STOP switch is set .On start, the code settings are compared with the previous value; if they are the same, control is passed on to the **fine movement** routine of the motor ( Frequency or power motor depending on the position of the FREQ / POWER switch ) . If the code settings are different, control is passed to the **coarse** routine . Here the power motor is moved after the frequency motor . In the course of movement of the frequency motor, if the START / STOP switch is cleared, control is passed back to the main program without doing the power routine. Otherwise, the motor is rotated till there is a transition in the comparator o/p ( i.e., the motor reaches the desired position ) and the control is passed to the **power** routine in which the same procedure is followed . After the power motor has reached the desired position, or the START / STOP switch is cleared, control is transferred to the main program .

In the **coarse** routine, to indicate the stopping of the motor, a **blink** routine is called, which toggles the code LEDs for a duration of 10sec.

In the **remote** mode of operation, the controller continuously polls for the data to be received. A link is established between the P.C. and the controller by sending an address to the controller. If the address from the P.C. is valid, the controller acknowledges by sending an acknowledge signal to the P.C. along which information regarding the latest code set in LOCAL, the status of  $\bar{L}/R$  and limit switches are sent. If the controller is in LOCAL mode, then no further information is sent to it from the P.C. side. Else, a second byte is transmitted. The P.C. polls for the acknowledgement only for a certain interval of time after which the address has to be re-transmitted if

required. Once the link is established, the second byte is transmitted. This carries information about the code set from REMOTE, the motor to be operated, the direction of operation (if it is fine movement another byte indicating the number of steps may be sent). The controller processes the data and moves the motor accordingly. After completion of operation, another acknowledgement is sent to the P.C.

The data transmission is mainly in polling mode at both the ends. Eleven bit operation is employed for the transmission of the address byte. Apart from the start, stop and 8 address bits, a ninth bit is set which identifies the byte as an address, to the controller. ( **mode 3** operation). The P.C. employs 11 bit operation by using 2 stop bits for transmission. One of the stop bits is interpreted as the ninth data bit by the controller. After the address is acknowledged and the link is set up, both the P.C. and controller change to 10 bit operation. (**mode 1** operation ).

### **REGISTER INITIALIZATIONS:**

The pointers for the look-up tables are stored into registers at the beginning of the program. Some special function registers have to be initialized at the beginning of the program. They are described as follows:

#### **TCON: Timer / Counter Control Register**

TCON is set to **40H** , thereby turning timer 1 on to generate the required baud rate for serial communication. Level triggering mode is used for interrupt **INT0**.

#### **TMOD: Timer / Counter Mode Control Register**

TMOD is used to enable either timer or counter operation and to set their mode of operation. Among the 8 bits, 4 bits each are used to set parameters for each timer (Timer 0, Timer 1). Timer mode is enabled, and the timer ( Timer 1) is operated in mode 2 , which is an 8-bit auto reload mode. This is done to generate the required baud rate. TMOD is set to **20H**. The 8-bit reload value to set the baud rate is stored in TH1 and TL1.

Baud rate is generated (Mode 1 and 3) using the relation

$$\frac{2^{SMOD}}{32} \times \frac{Osc. freq}{12 \times (256 - TH1)}$$

where oscillator frequency is 11.059MHz, SMOD = 0 and TH1=FDH which is the reload value. A value of **FDH** is used for a baud rate of **9600bps**.

**PCON: Power control Register:** This register is set to 00H and is redundant in this application.

**SCON: Serial Port Control and Status Register.**

This register contains not only the mode selection bits, but also the 9th data bit for transmit and receive (TB8 and RB8) and the serial port interrupt bits (TI and RI).

SCON is set to **58H** for Mode 1 and **D8H** for Mode 3 respectively. Both have variable baud rate. TI and RI are polled for transmission and reception of data.

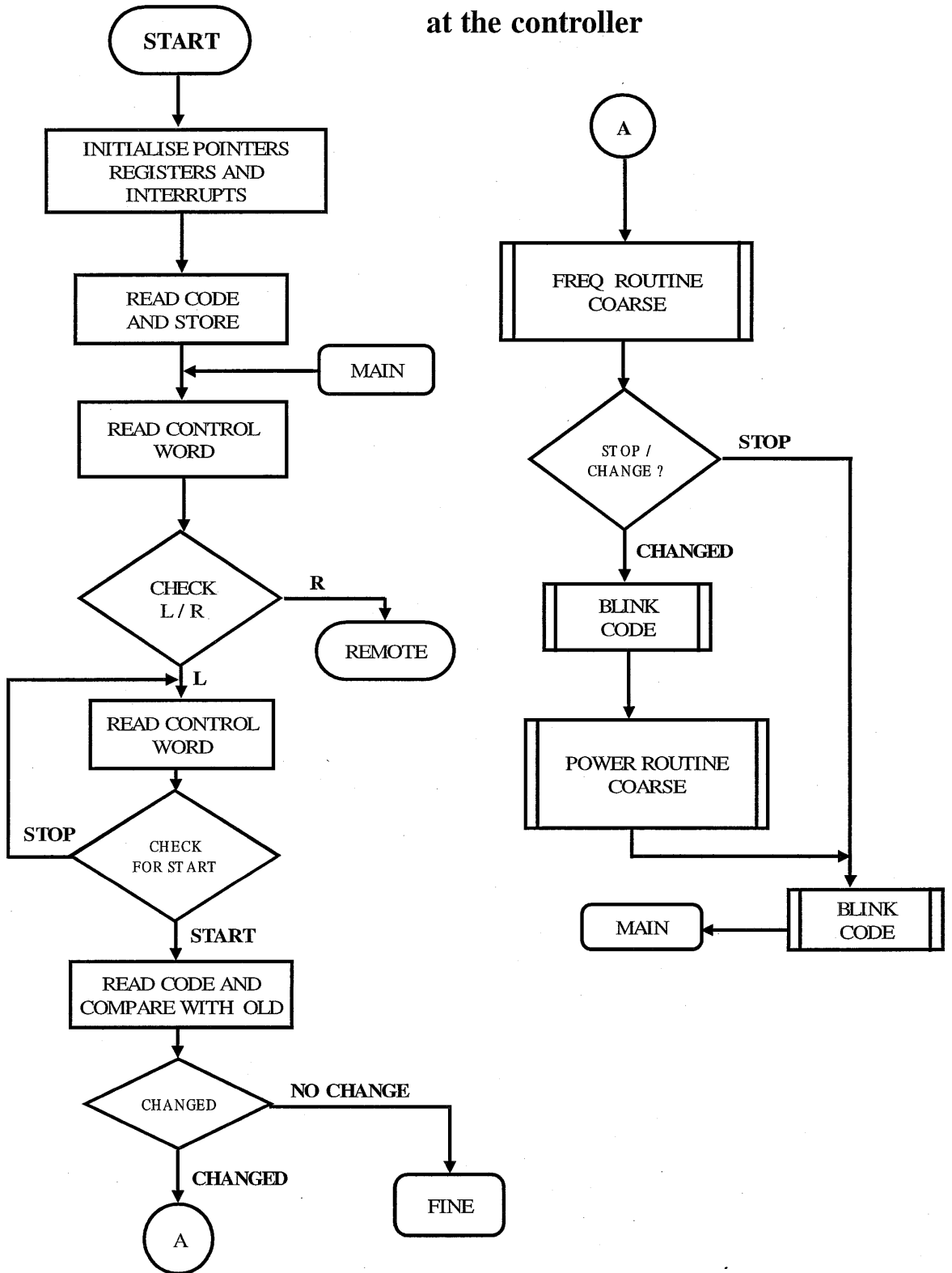
**IE (Interrupt Enable Register):**

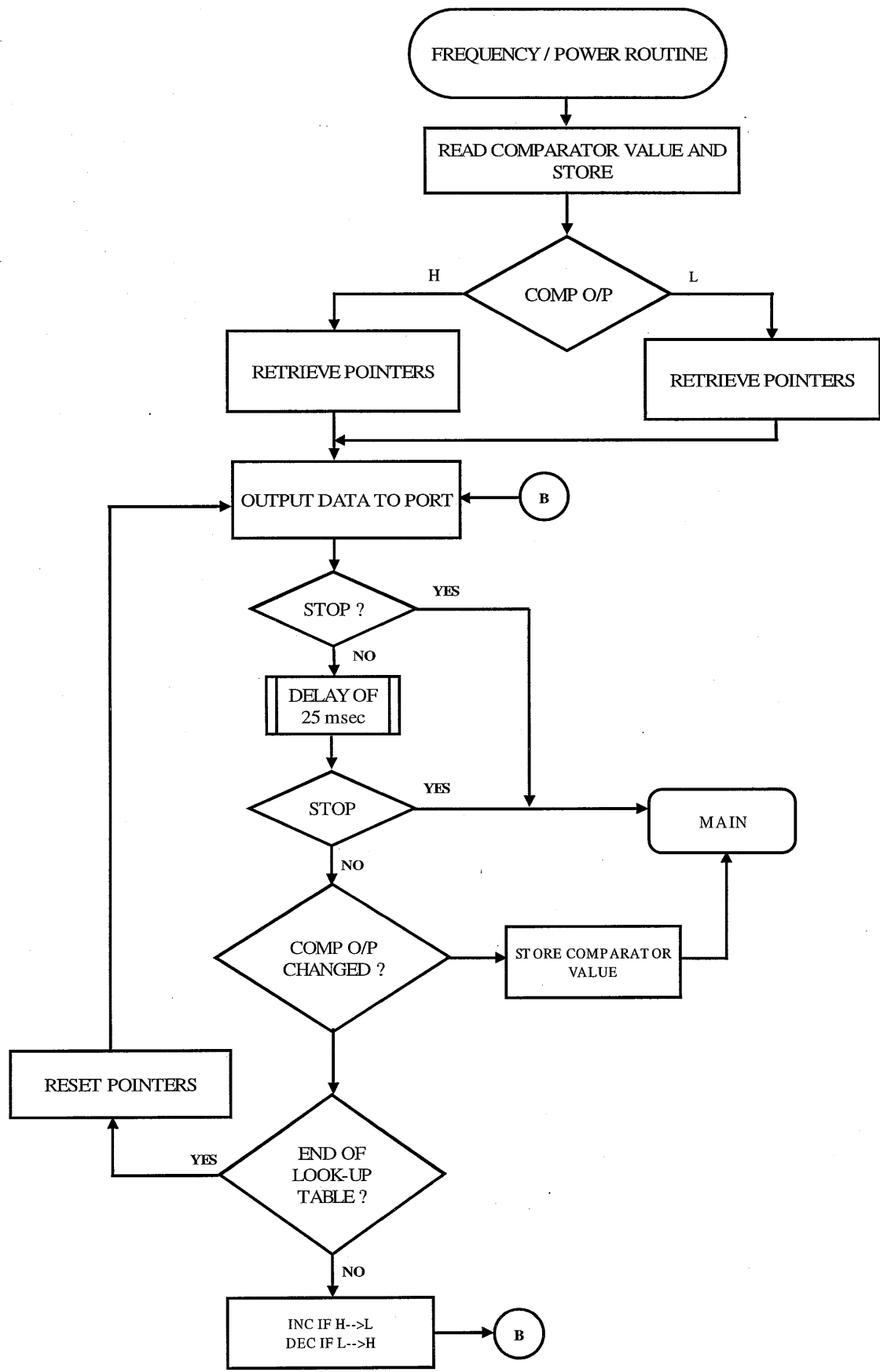
IE is set to **91H** in LOCAL mode to enable interrupt INT0 and serial interrupt and **81H** in REMOTE. Serial interrupt is used only in LOCAL mode to deny the remote access since the controller cannot poll serial reception in this mode.

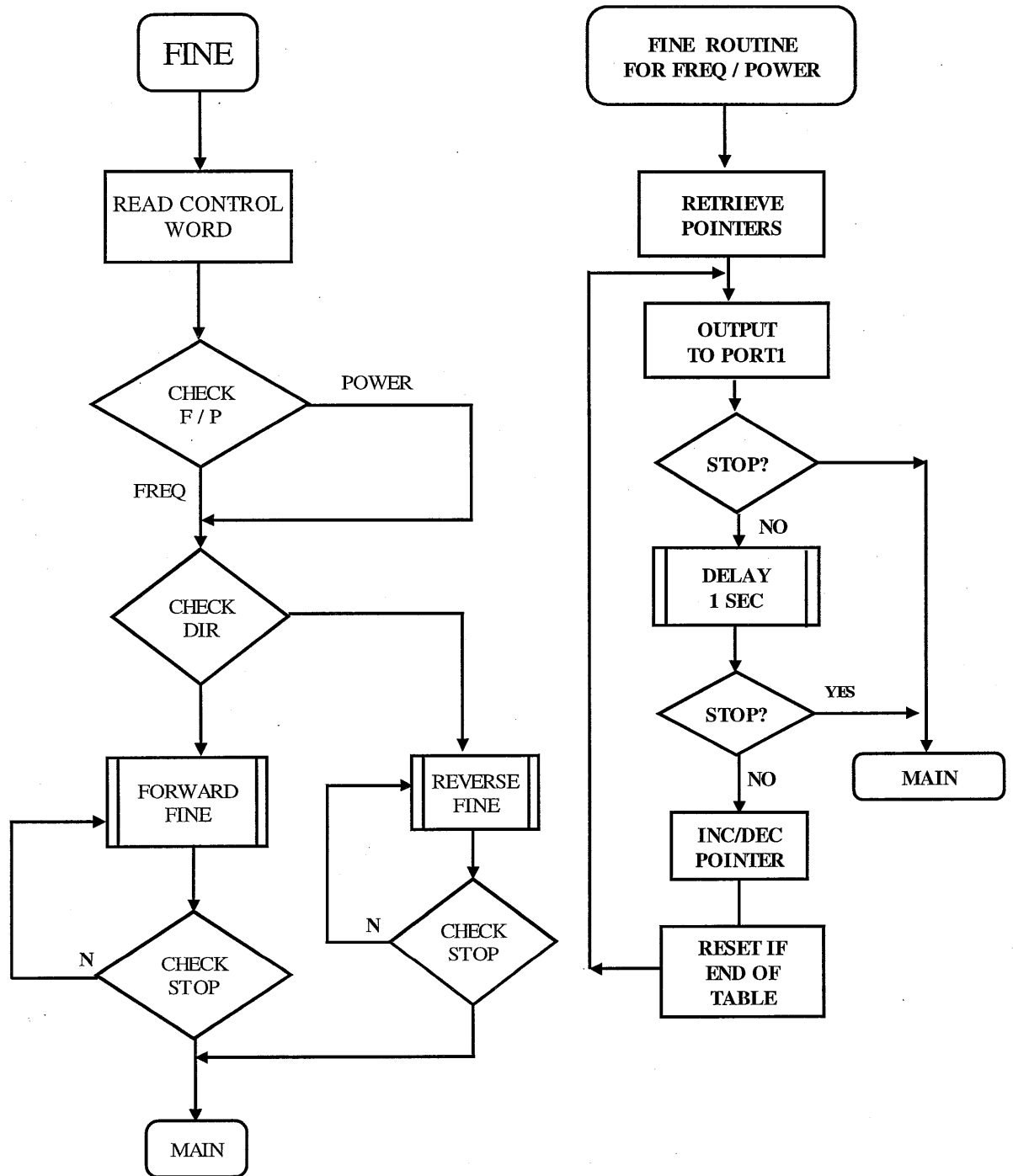
On the P.C. side, a built-in function of C++, **BIOSCOM** is used to define settings for baud rate and to read the status register after each transmission and reception. It also defines the port to be accessed (COM1/COM2). Functions **inportb** and **outportb** are used to receive and send data respectively. Details of setting serial port configuration from BIOS is given in the data sheets.

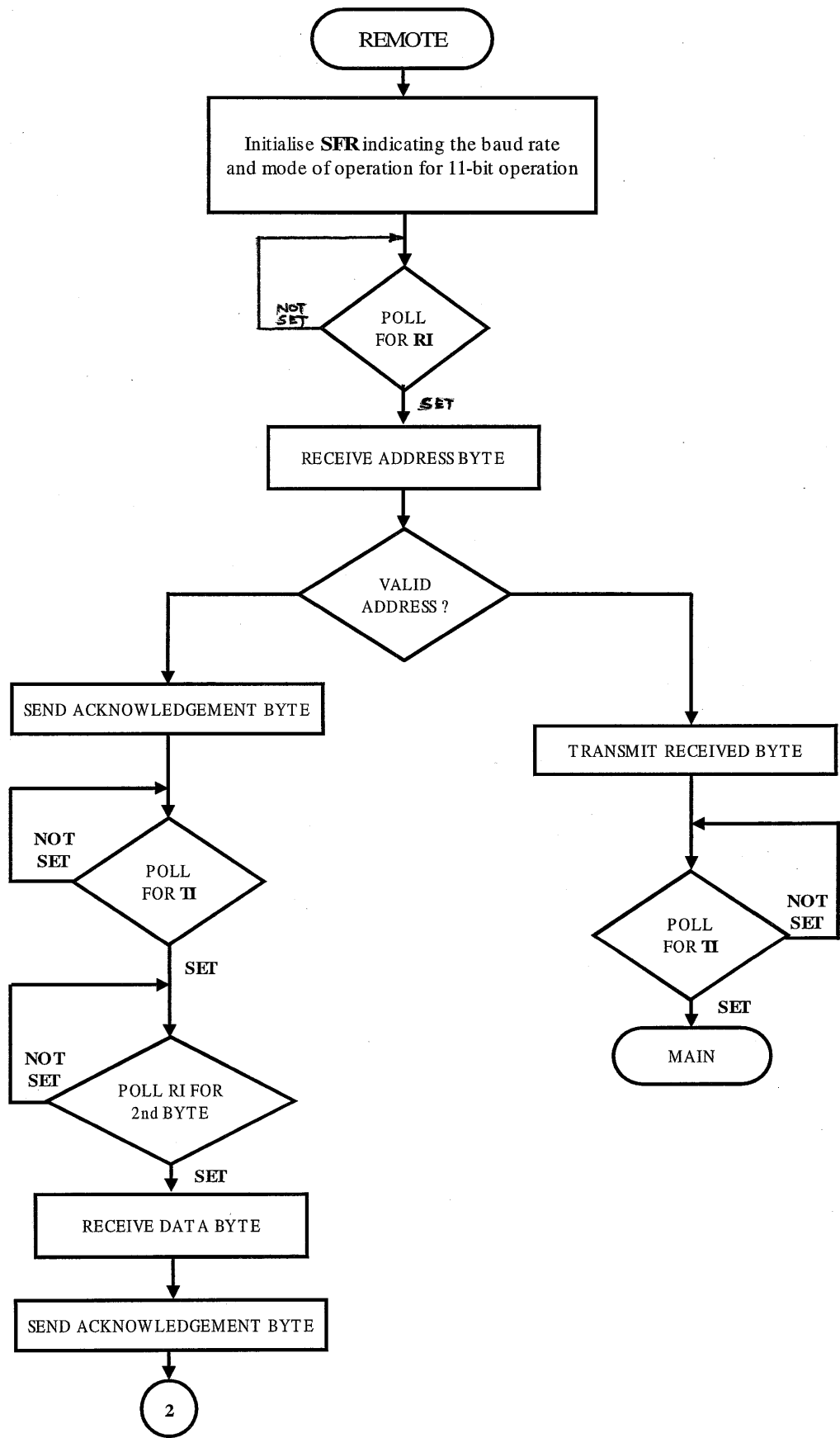
The ALP is converted to object code using assembler **X8051**. The OBJ file is converted to HEX file using **LINK51** which is further converted to a binary file by **HEXBIN** converter. This binary file is programmed on to the EPROM using **CHIPMASTER 3000**.

### Flowcharts for software at the controller

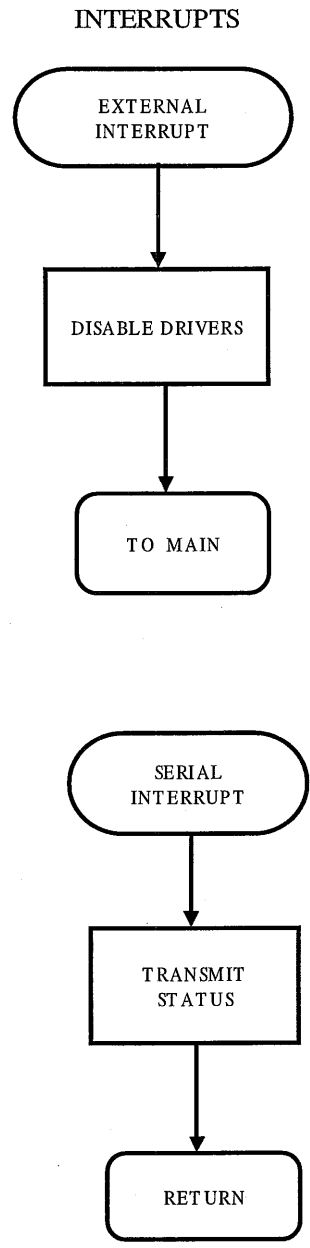
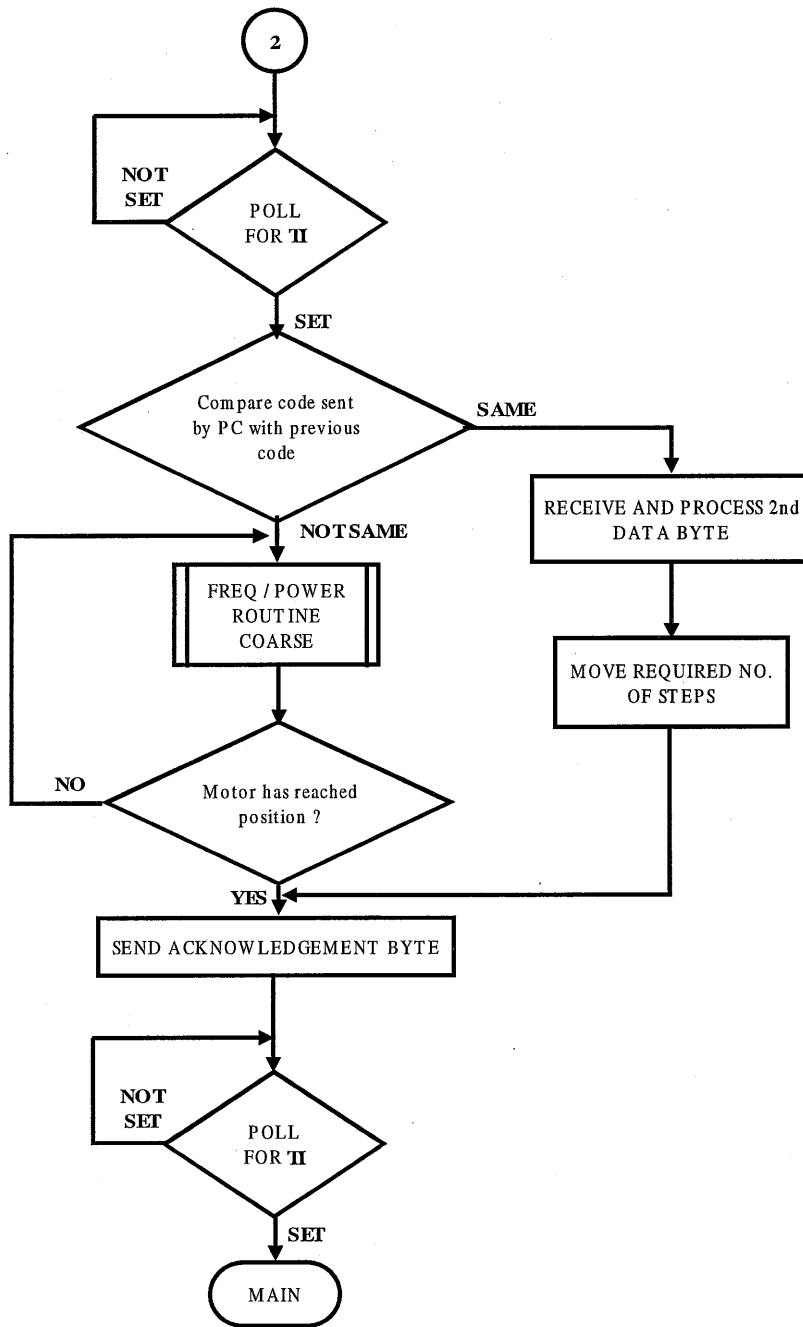


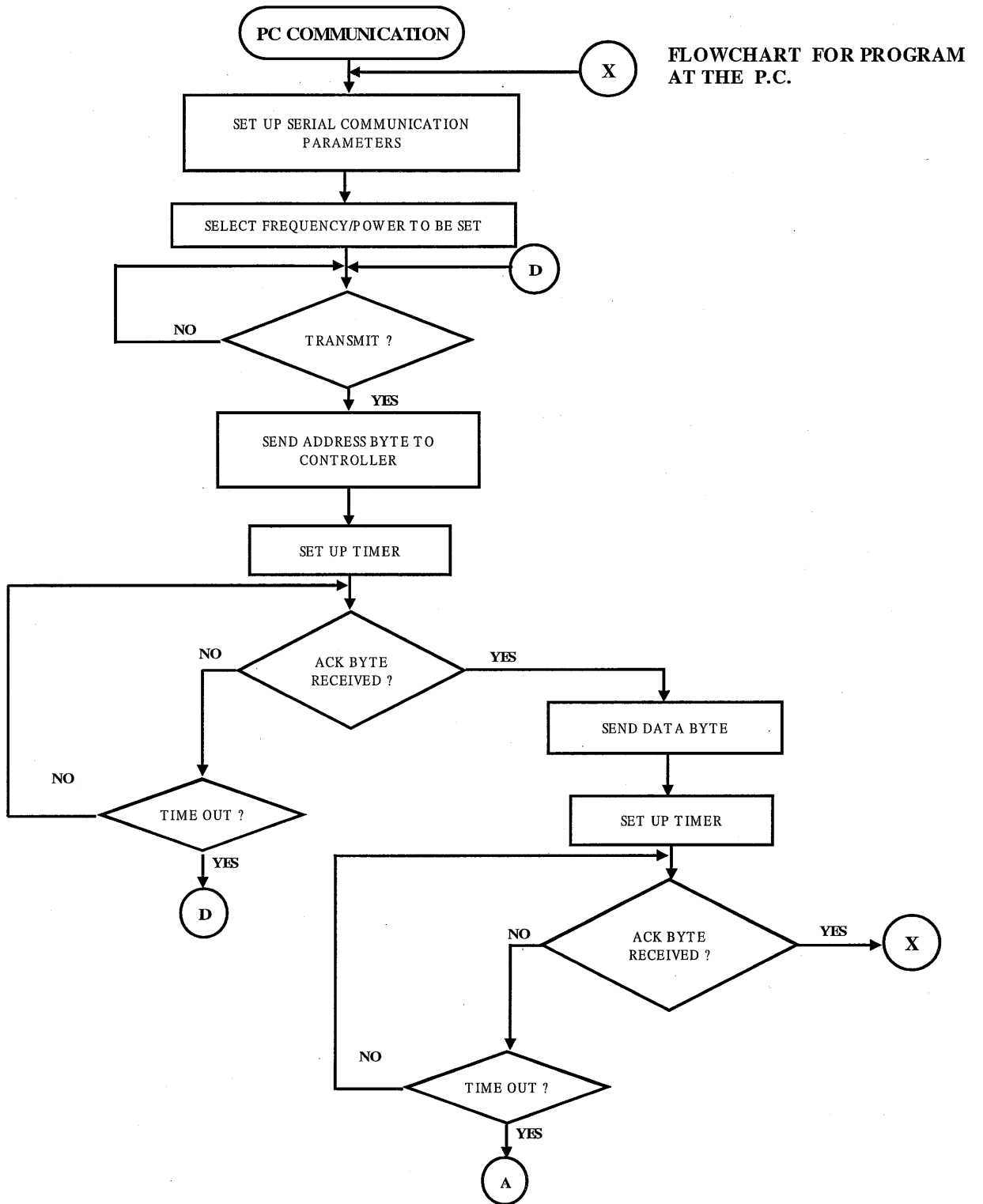












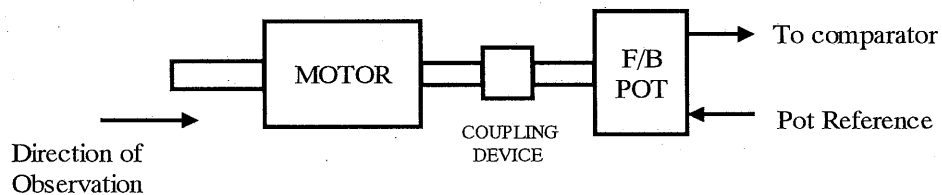
*Conclusion*

## CONCLUSION

The present work has presented a study in the electronics of a stepper motor, using a  $\mu$ -controller ( 8031 ) as the Central Processing Unit. The main aim of the project is to control a 200-step stepper motor in  $\mu$ -stepping mode to get 3600 steps per revolution, each step corresponding to a change of 0.3 mV on the coupled f/b pot.

The system operates the motor in both coarse and fine movement.

- **Coarse movement** by setting a code (  $S_2, S_1, S_0$  ) on the front panel. The motor moves only if the code sent varies from the previously stored value, and in a direction determined by the code and the comparator o/p.



H  $\rightarrow$  L transition  $\Rightarrow$  Anti-clockwise movement

L  $\rightarrow$  H transition  $\Rightarrow$  Clockwise movement

The direction of rotation may be changed by either making alterations in the software, or by reversing the polarities of the f/b pots.

- **Fine movement** by setting the direction switch on the front panel, and turning the motor ON and OFF by using the START /STOP switch on the front panel.

DIRECTION SWITCH:

L  $\rightarrow$  Clockwise movement

H  $\rightarrow$  Anti-clockwise movement

For the purpose of testing, 8 different voltages were set at the reference pots, one for each freq/power. On setting a particular code, the motor moved to the specified position wherein the f/b voltage equalled the reference i/p. All the codes were set one by one, and in each case, after the motor stopped moving, the readings corresponding to the f/b voltages and reference voltages were measured using a 5-digit multimeter ( to observe changes of the order of mV).

A plot of the code v/s f/b voltage indicated that the readings coincided for both forward and reverse direction of motor movement.

## *Conclusion*

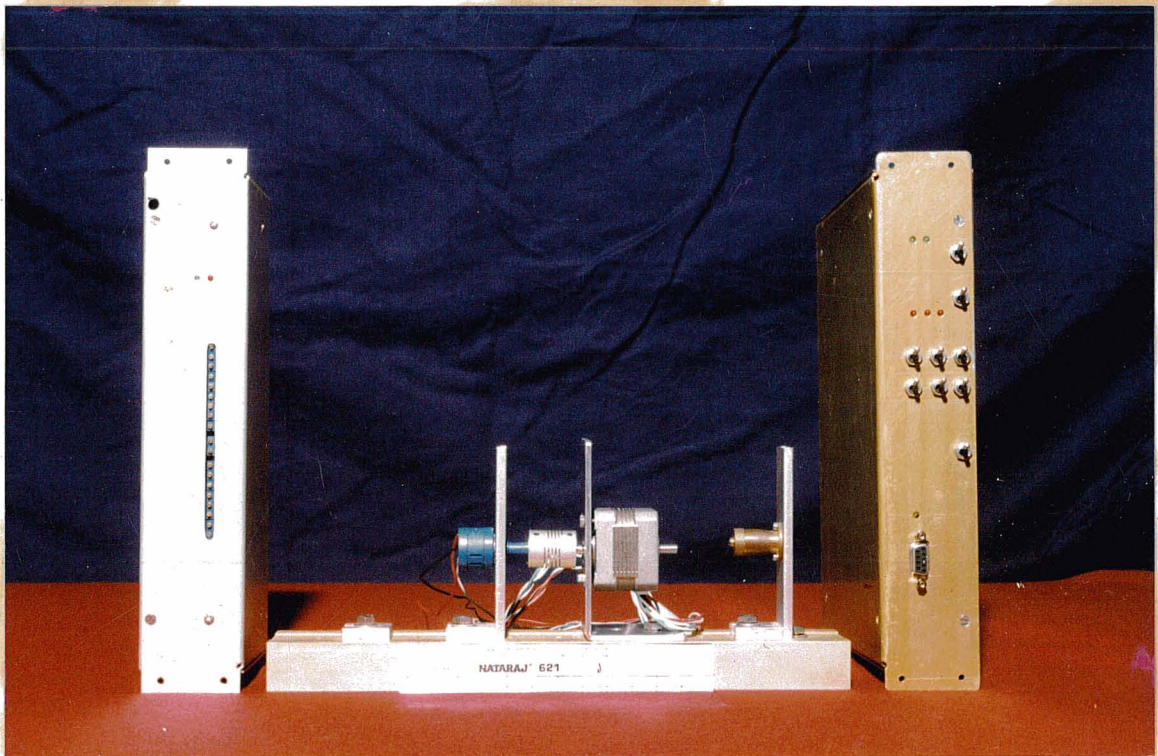
The differences b/w the reference and f/b voltages were tabulated, and a plot of the differences v/s code revealed that the deviation for all codes was fairly constant for L→H transitions, i.e., clockwise movement of the motor, at a value of 0.5mV. This corresponds to an error of 3  $\mu$ -steps. This problem can be solved by providing a suitable off-set in the reference voltages corresponding to each code, or by moving the motor in fine movement after the motor has stopped.

In **remote** operation, the motor movements can be controlled from a distant location, by a P.C.

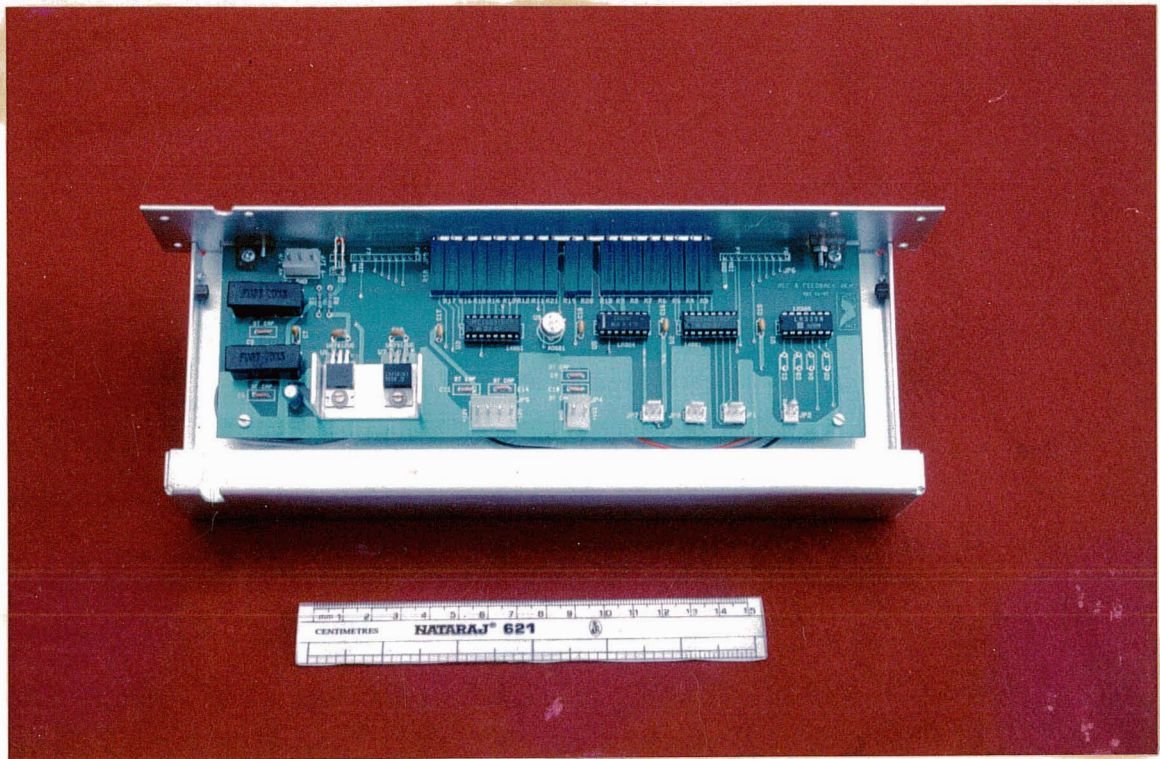
- The P.C. can set the required freq/power and transmit the code to the controller.
- The P.C. first sends an address byte to the controller, and sends the code as a data byte only on receiving an acknowledgement.
- The controller gives an indication to the P.C. when the motor has reached the desired position, and also gives information regarding the status of the controller.
- When the P.C. tries to access the system when it is operating in LOCAL mode, the controller gives an indication to it, denying permission to change settings.
- A facility can be provided to operate the motor in fine movement. For this purpose, the software at the P.C. side can be modified to send a 2<sup>nd</sup> data byte containing the no. of steps to be moved, and in what direction.
- A *hot-key* can be provided at the PC to stop motor movements immediately, if the key is pressed.

# *Appendix*

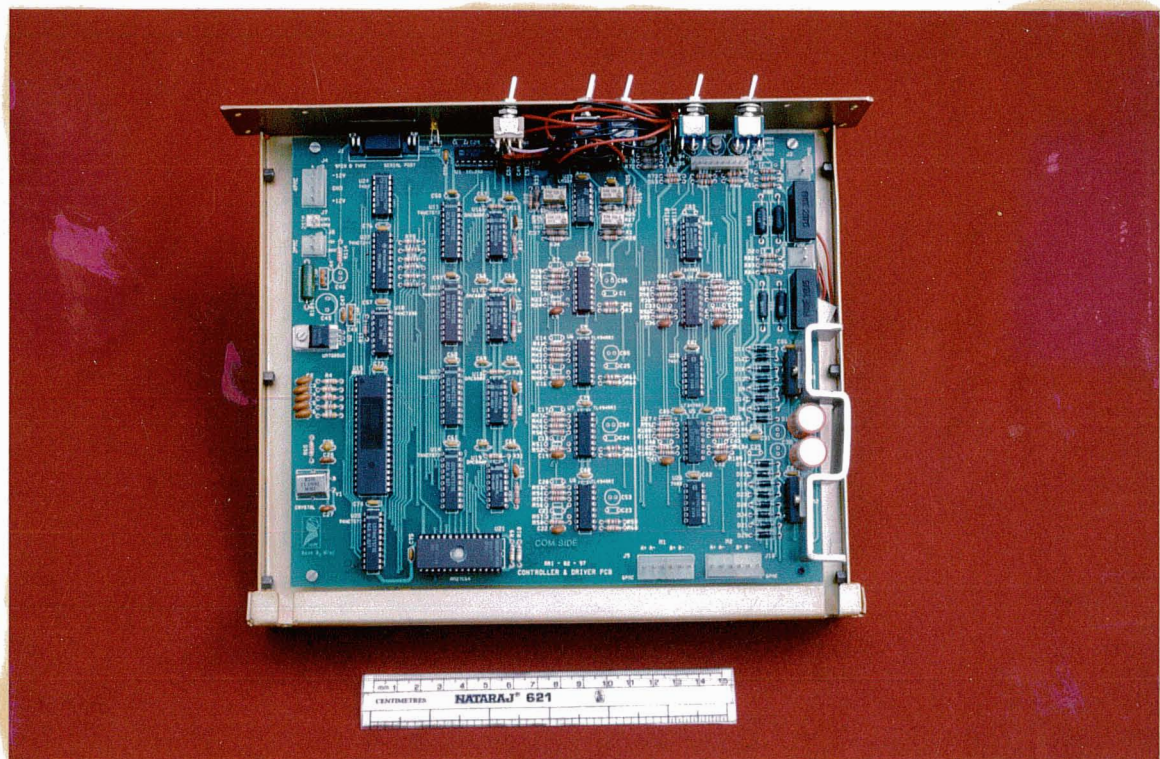
**PHOTOGRAPHS:**



**FRONT VIEW OF THE MODULES**

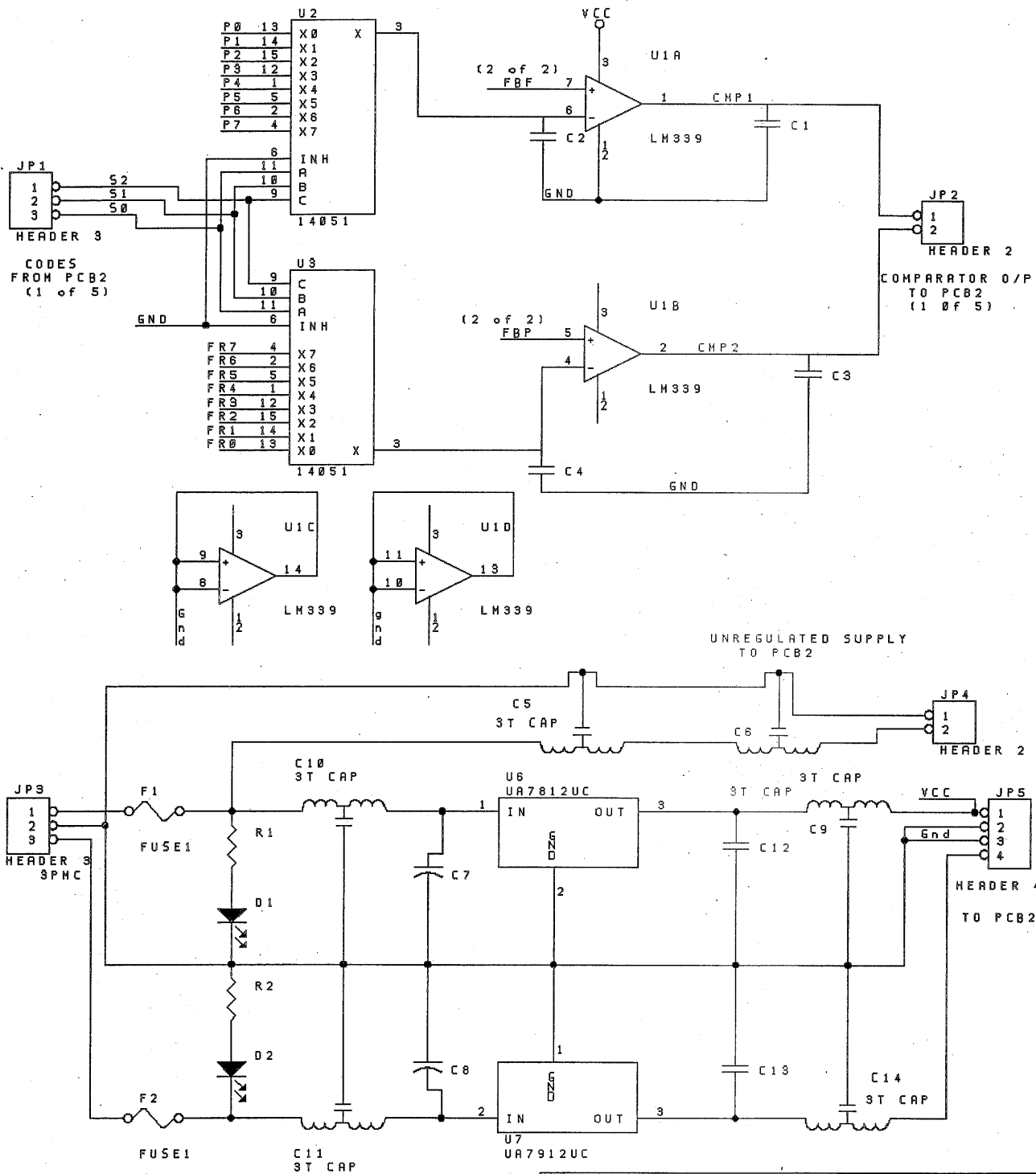


*VIEW OF PCB 1*

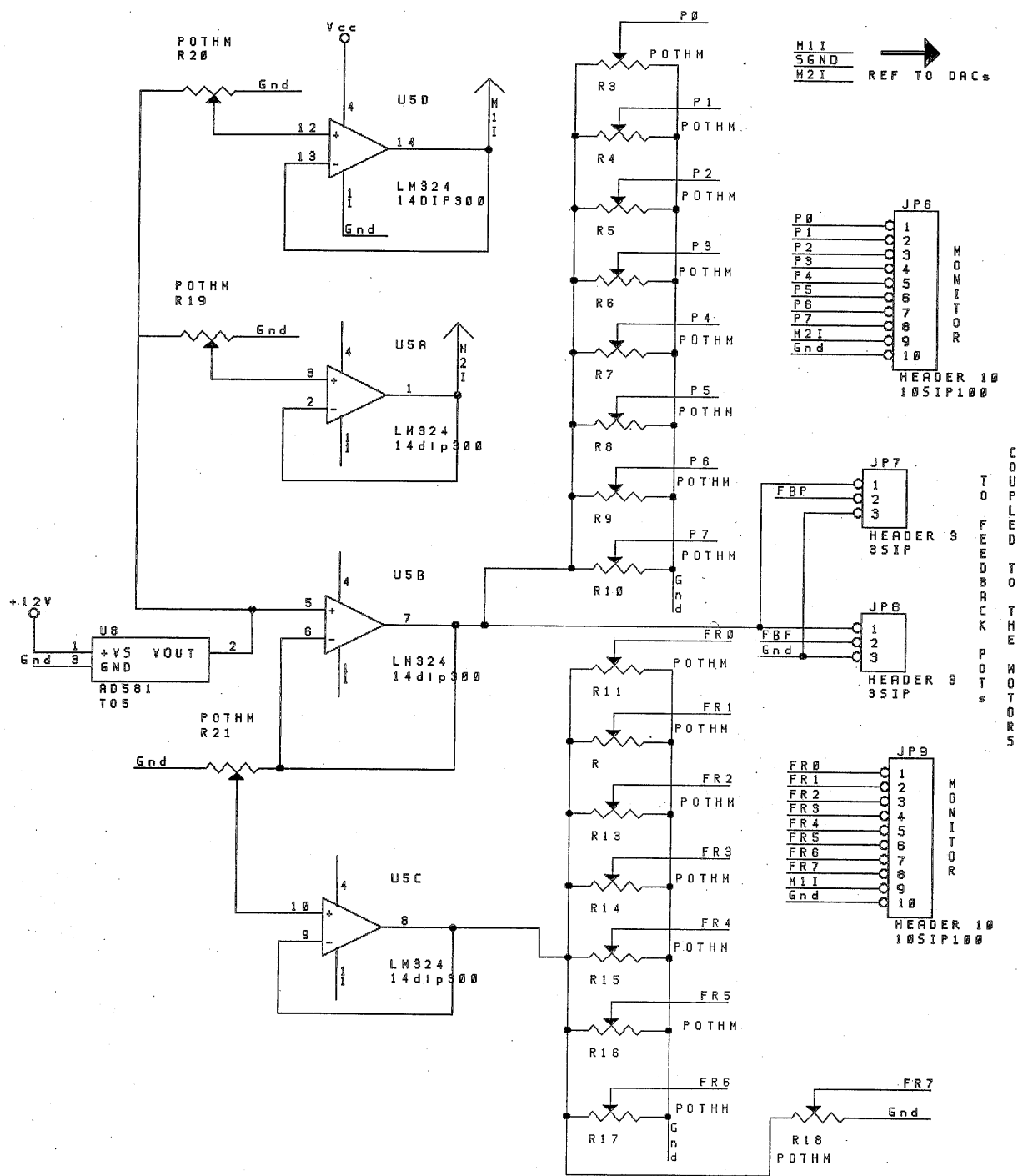


*VIEW OF PCB 2*

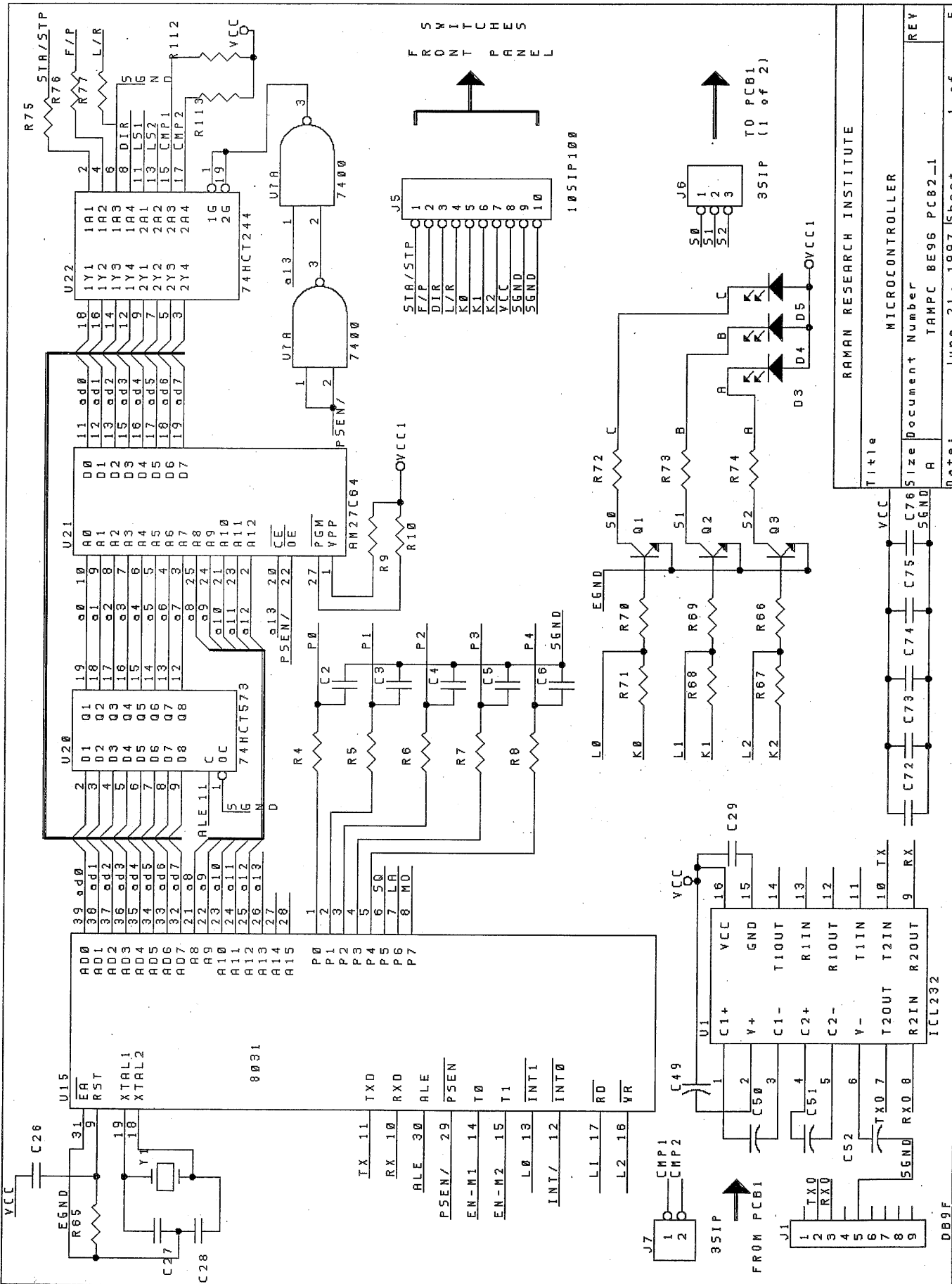




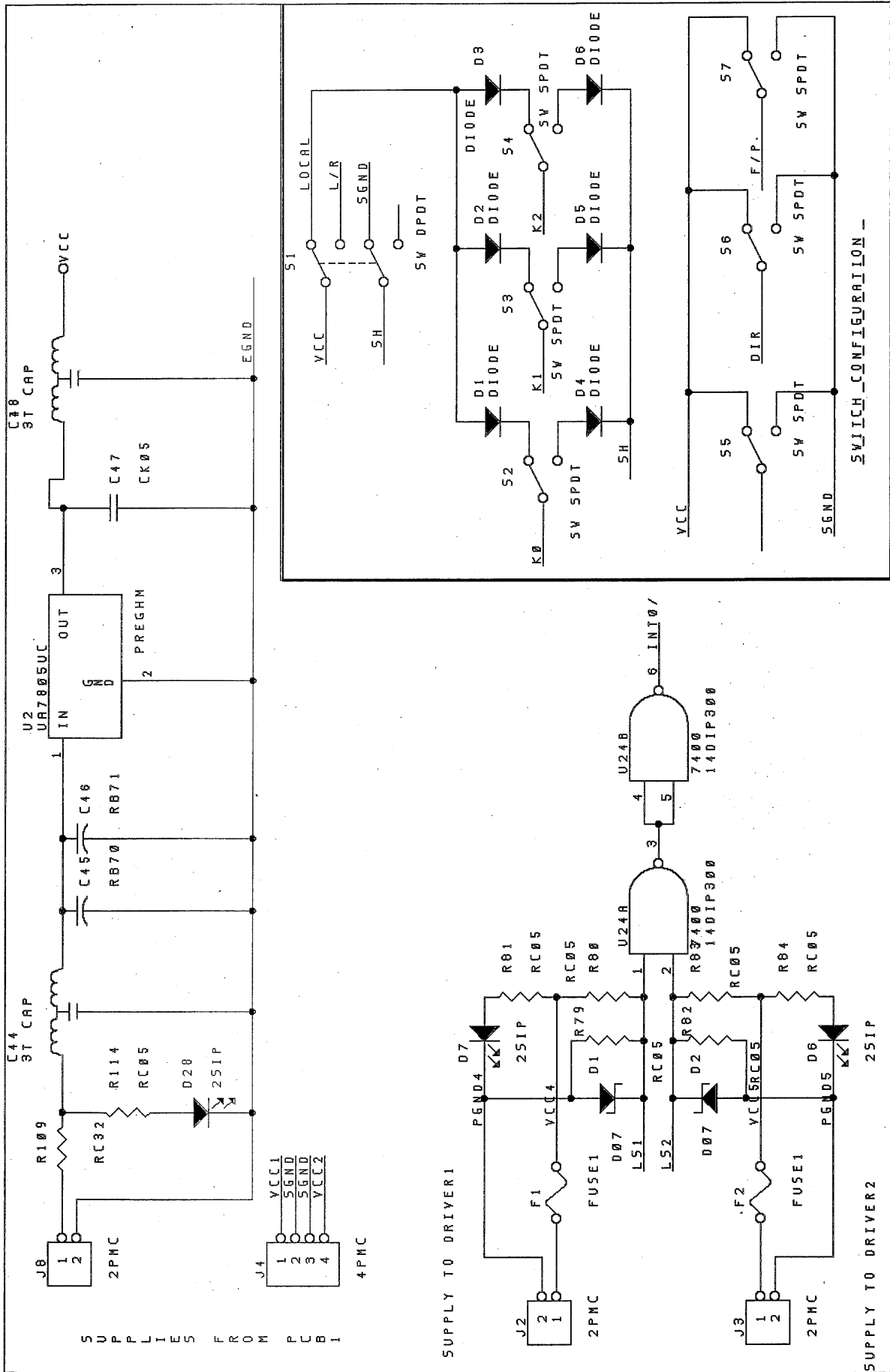
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REGULATED SUPPLY AND CODE MUXING		
Size	Document Number	REV
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Date:	June 21, 1997	Sheet 1 of 2



RAMAN RESEARCH INSTITUTE		
Title		
REFERENCE ADJUSTMENTS		
Size	Document Number	REV
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Date:	June 21, 1997	Sheet 2 of 2

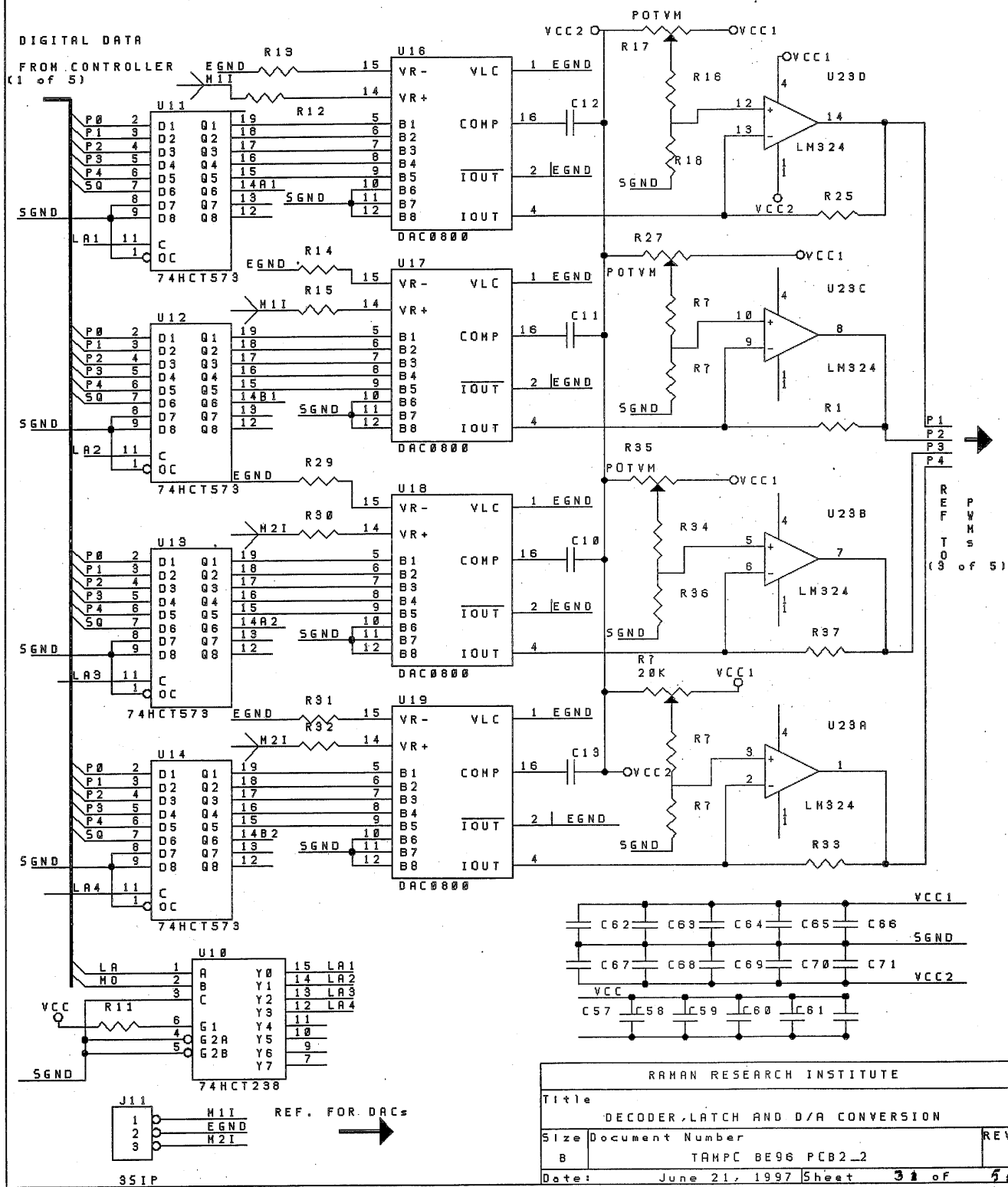


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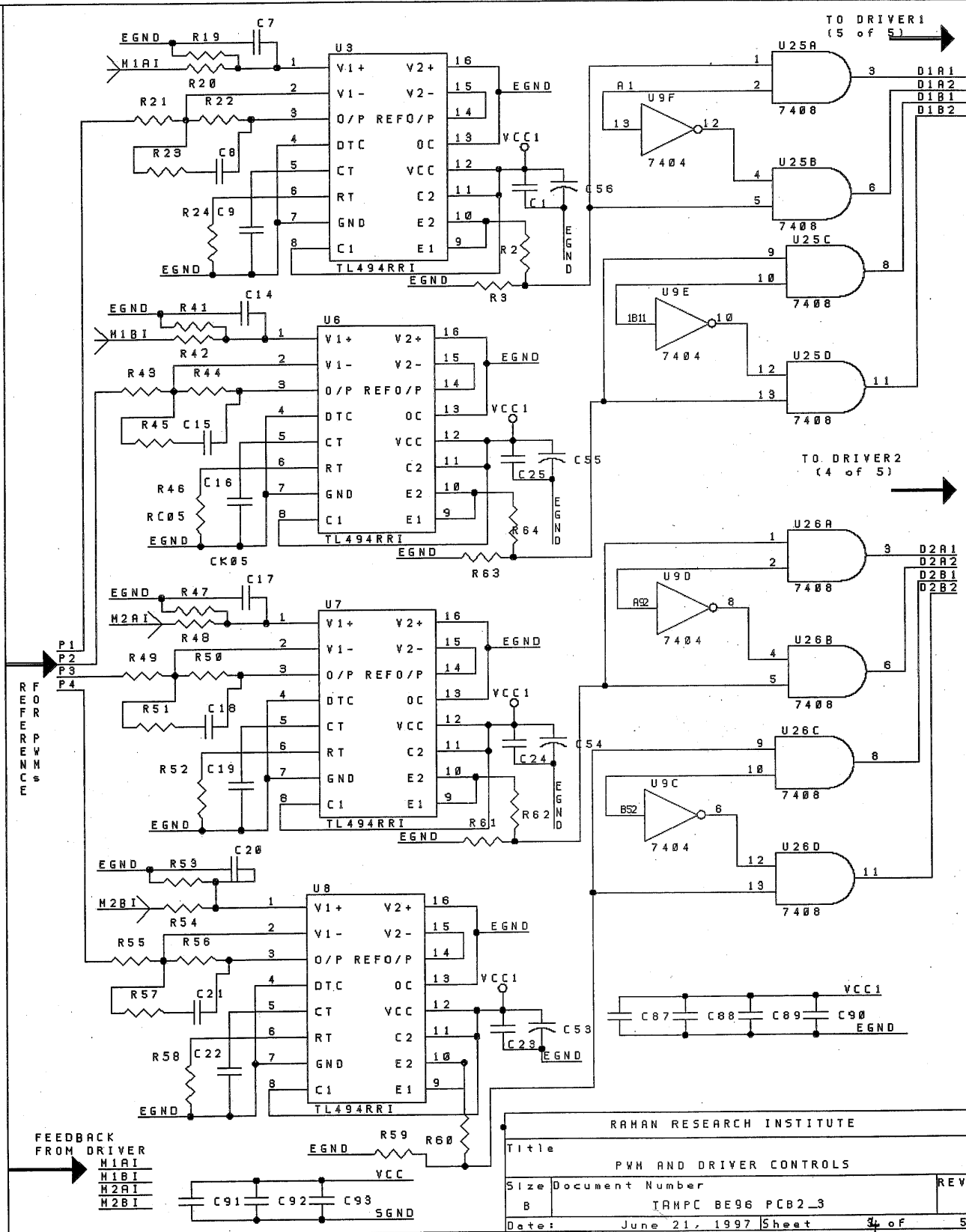


RAMAN RESEARCH INSTITUTE

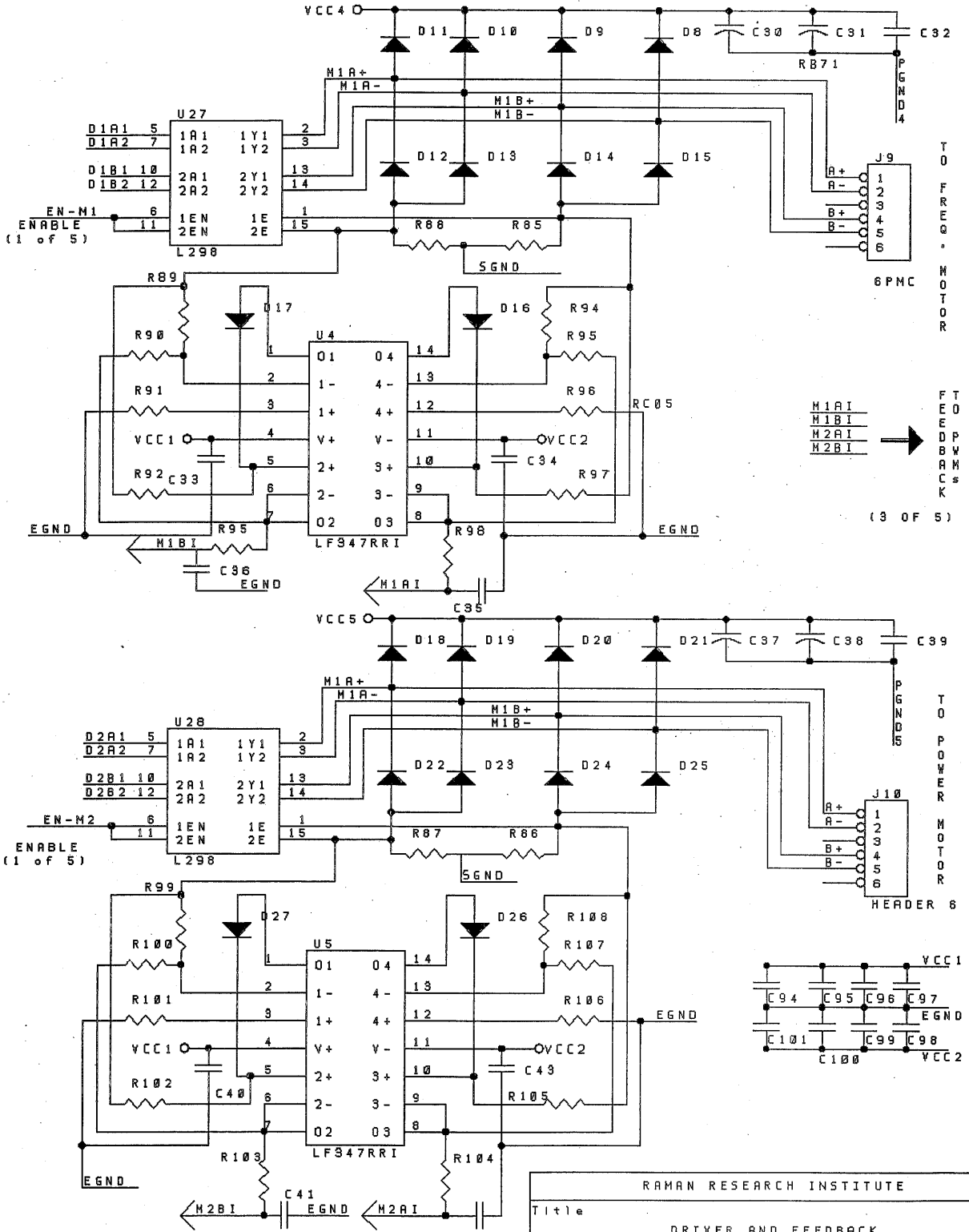
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Size	Document Number
REV	RAM
	TAMPC BE96 PCB2_5



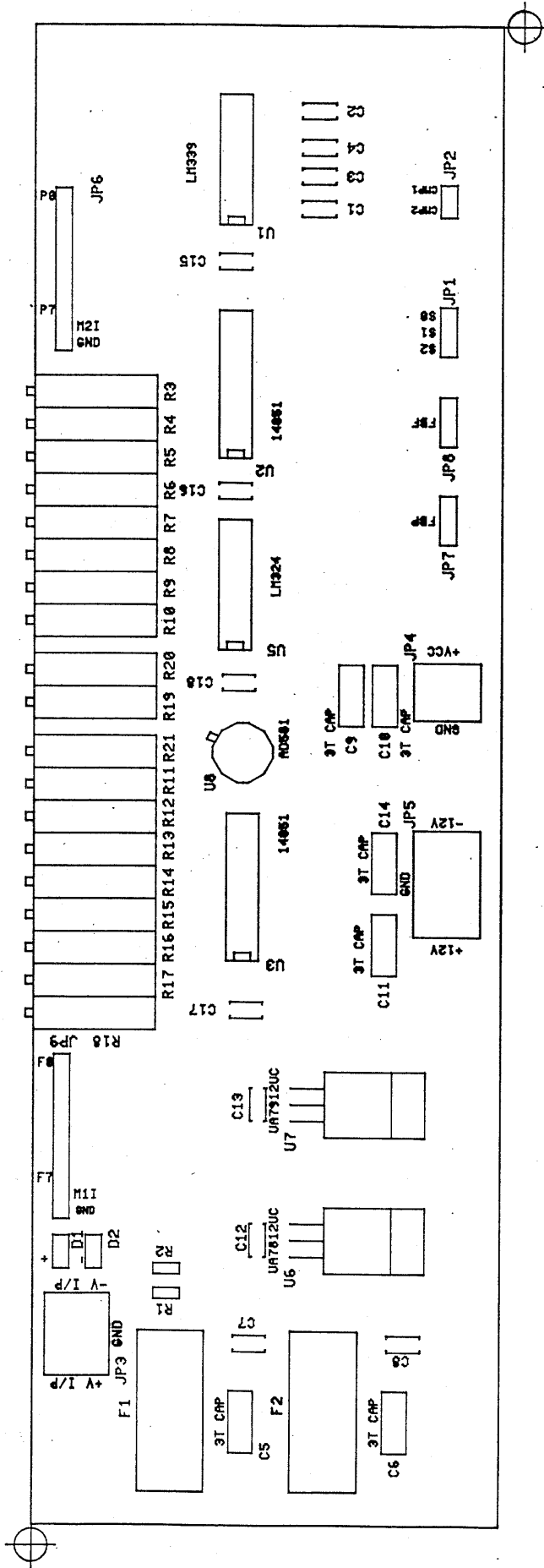
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Title DECODER, LATCH AND D/A CONVERSION		
Size B	Document Number TAMPC BE96 PCB2_2	REV
Date: June 21, 1997	Sheet 3 of 5	REV



RAHAN RESEARCH INSTITUTE			
Title			
PWM AND DRIVER CONTROLS			
Size	Document Number	REV	
B	TRMPC BE96 PCB2_3		
Date:	June 21, 1997	Sheet	3 of 5

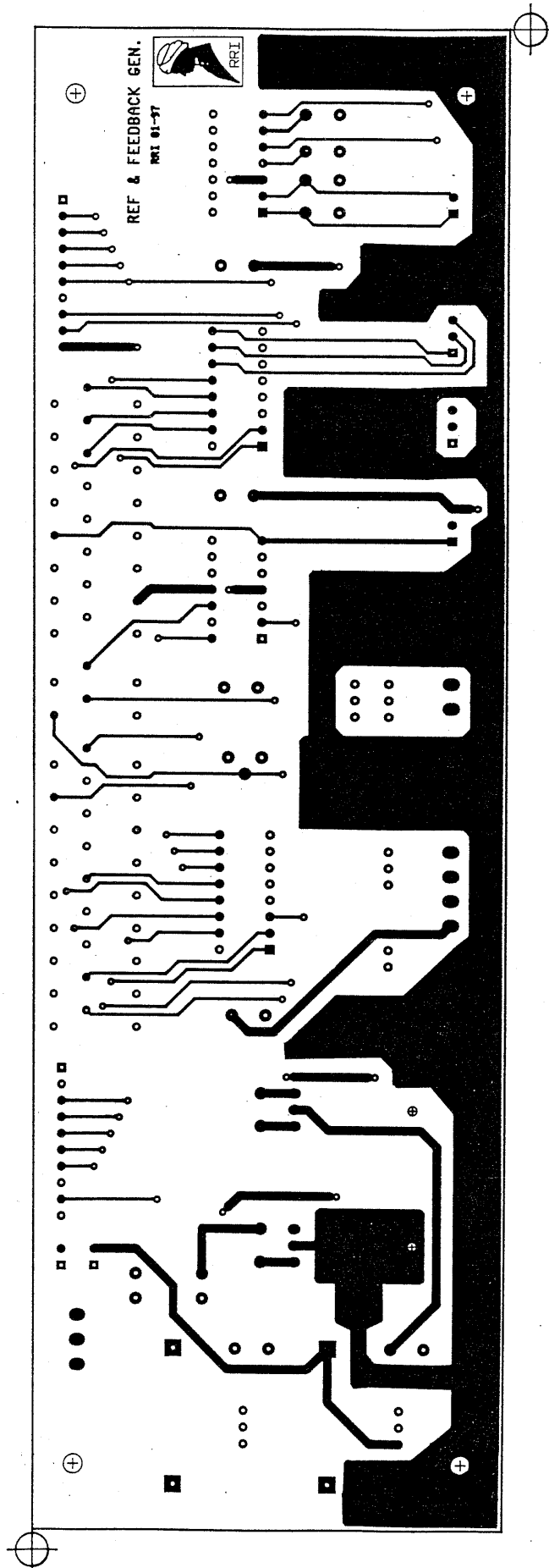


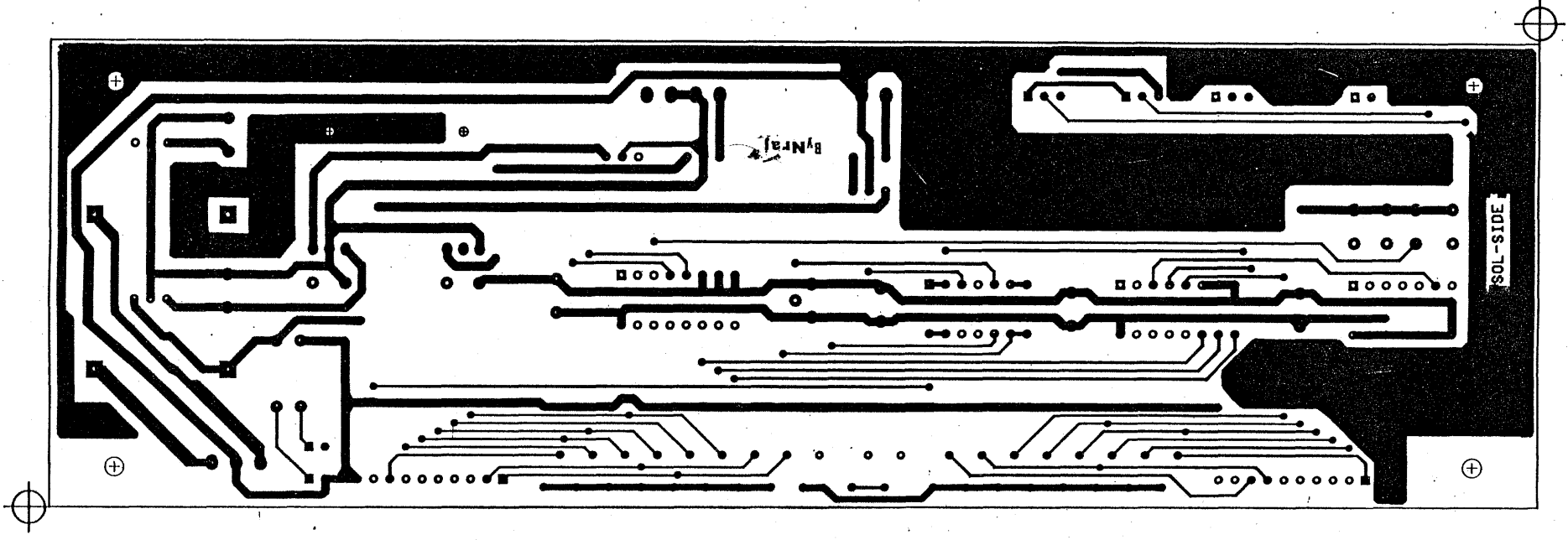
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DRIVER AND FEEDBACK			
Size	Document Number	REV	
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Date:	June 21, 1997	Sheet	5 of 5

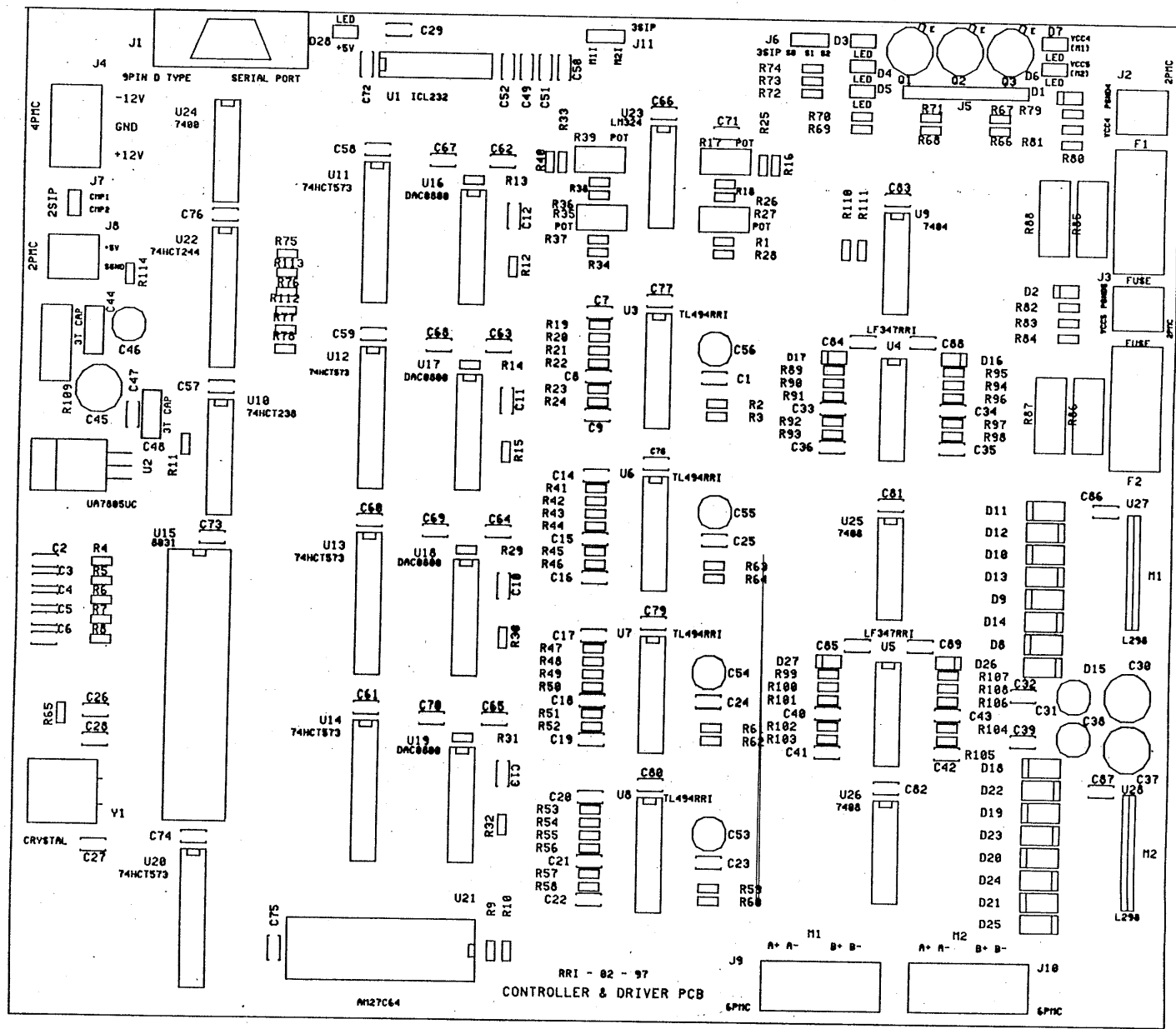


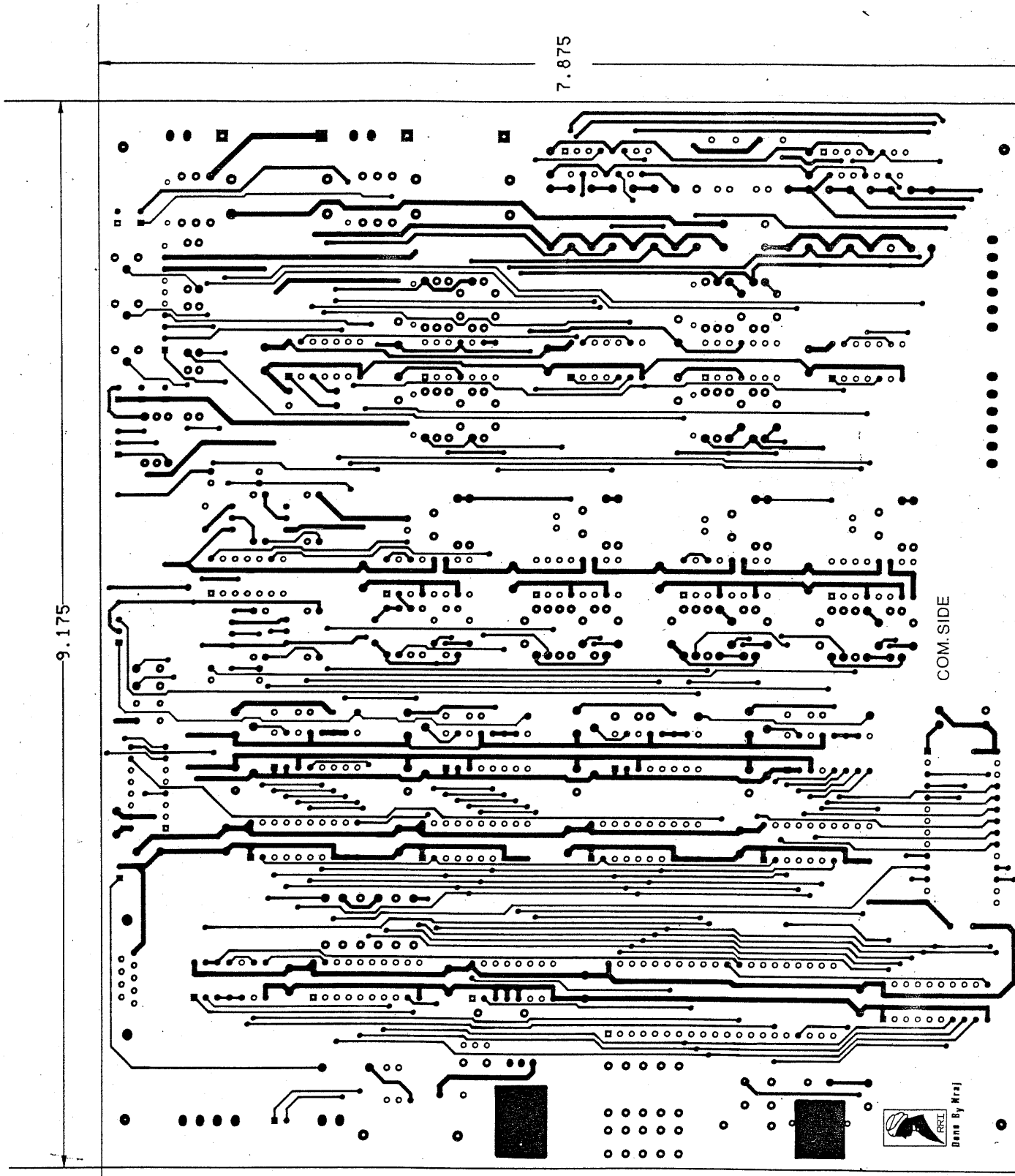
PCB-1 COMPONENT LAYOUT

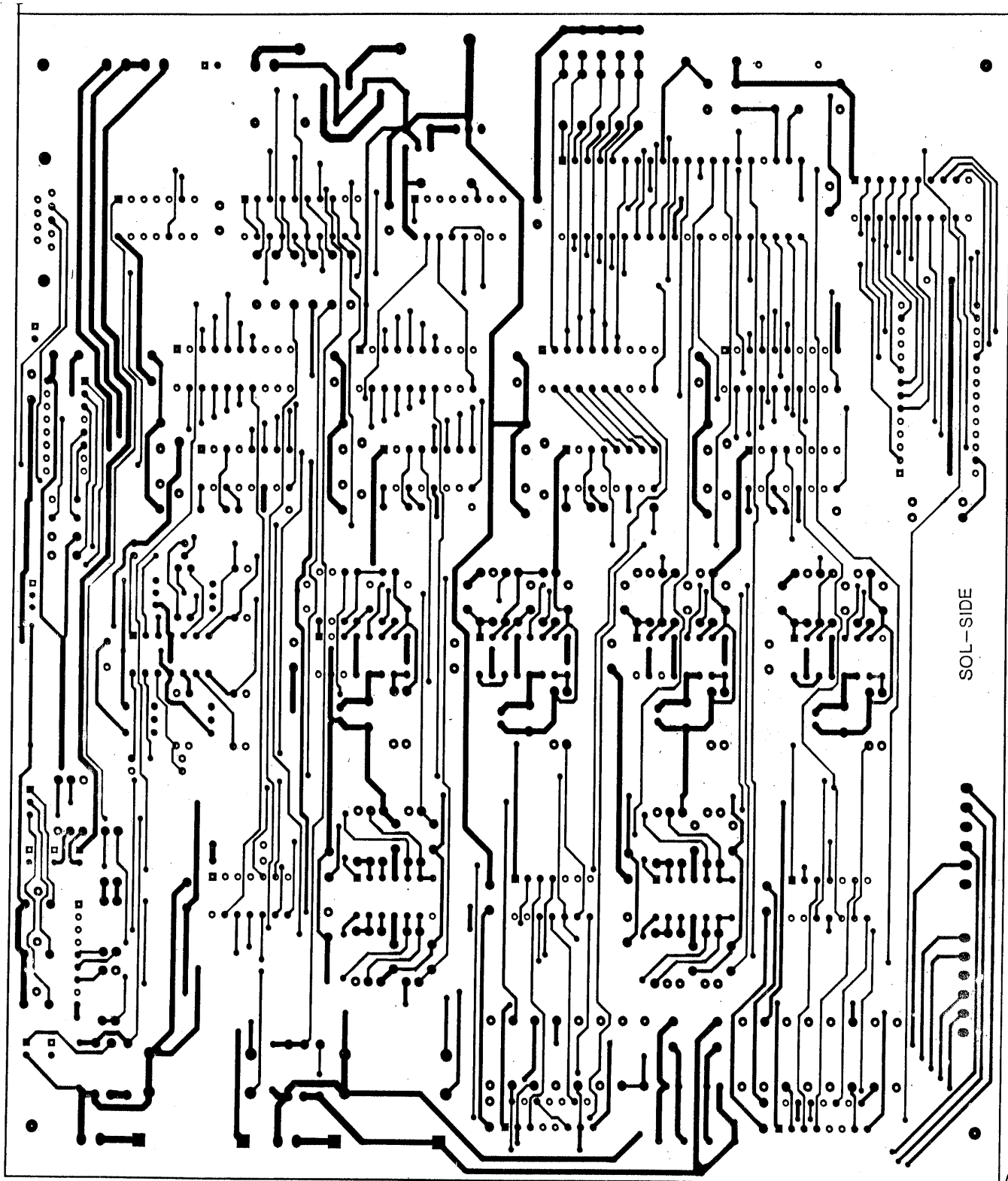












**LIST OF COMPONENTS OF PCB-1**  
**Reference Settings and Regulators**

Item	Quantity	Reference	Part
1	4	C1,C2,C3,C4	
2	6	C5,C6,C9,C10,C11,C14	3T CAP
3	1	C7	.33uf
4	1	C8	33uf
5	2	C12,C13	.01uf/16V
6	2	D2,D1	LED
7	2	F1,F2	FUSE/250mA
8	2	JP3,JP1	HEADER 3
9	2	JP4,JP2	HEADER 2
10	1	JP5	HEADER 4
11	2	R1,R2	1.8K
12	1	U1	LM339
13	2	U2,U3	MC14051
14	1	U6	UA7812UC
15	1	U7	UA7912UC
16	2	JP9,JP6	HEADER 10
17	2	JP7,JP8	HEADER 3
18	8	R11,R13,R14,R15,R16,R17, R18,R	10K
19	8	R3,R4,R5,R6,R7,R8,R9,R10	50K
20	3	R19,R20,R21	5K
21	1	U5	LM324
22	1	U8	AD581

**Connectors/Headers**

JP1	Codes from PCB 2
JP2	Comparator o/p to PCB 2
JP3	Supply
JP4	Unregulated supply to PCB 2
JP5	Regulated supply to PCB 2
JP6	Monitoring power reference values
JP7	To power feedback pot
JP8	To frequency feedback pot
JP9	Monitoring frequency reference values

**LIST OF COMPONENTS OF PCB-2**  
**Controller**

Item	Quantity	Reference	Part
1	16	C1,C7,C8,C14,C15,C17,C18, C20,C21,C23,C24,C25,C33, C34,C40,C43	
2	5	C2,C3,C4,C5,C6	6800pf
3	8	C9,C16,C19,C22,C35,C36, C41,C42	.01uf
4	42	C10,C11,C12,C13,C29,C32, C39,C57,C58,C59,C60,C61, C62,C63,C64,C65,C66,C67, C68,C69,C70,C71,C72,C73, C74,C75,C76,C87,C88,C89, C90,C91,C92,C93,C94,C95, C96,C97,C98,C99,C100, C101	.1uf
5	1	C26	10uf
6	2	C27,C28	33pf
7	2	C30,C37	100uf/63v
8	8	C31,C38,C45,C46,C53,C54, C55,C56	
9	1	C47	.01uf/16V
10	4	C49,C50,C51,C52	22uf/25V
11	6	D1,D2,D3,D4,D5,D6	DIODE/switch
12	2	D1,D2	DIODE ZENER
13	6	D3,D4,D5,D6,D7,D28	LED
14	16	D8,D9,D10,D11,D12,D13, D14,D15,D18,D19,D20,D21, D22,D23,D24,D25	DIODE/FR102
15	4	D16,D17,D26,D27	DIODE
16	2	F1,F2	FUSE/500mA
17	1	J1	CON9
18	4	J2,J3,J7,J8	HEADER 2
19	1	J4	HEADER 4
20	1	J5	HEADER 10
21	2	J6,J11	HEADER 3
22	2	J9,J10	HEADER 6
23	3	Q1,Q2,Q3	2N2222
24	4	R1,R25,R33,R37	470
25	17	R2,R4,R5,R6,R7,R8,R13, R14,R24,R29,R31,R46,R52, R58,R60,R62,R64	4.7K
26	11	R3,R59,R61,R63,R67,R68, R71,R79,R81,R82,R84	2.7K

## Appendix

27	11	R9,R10,R11,R75,R76,R77, R78,R110,R111,R112,R113	5.6K
28	21	R12,R15,R30,R32,R89,R90, R91,R92,R94,R95,R96,R97, R99,R100,R101,R102,R105, R106,R107,R108,R114	2.2K
29	4	R16,R26,R34,R40	110K
30	4	R17,R27,R35,R39	20K
31	4	R18,R28,R36,R38	220
32	8	R19,R22,R41,R44,R47,R50, R53,R56	330K
33	8	R20,R21,R42,R43,R48,R49, R54,R55	1.2K
34	4	R23,R45,R51,R57	
35	1	R65	8.2K
36	3	R66,R69,R70	33K
37	3	R72,R73,R74	1.8K
38	2	R83,R80	12K
39	4	R85,R86,R87,R88	3.3/1W
40	4	R93,R98,R103,R104	1.5K
41	1	R109	82/1W
42	1	S1	SW DPDT
43	6	S2,S3,S4,S5,S6,S7	SW SPDT
44	1	U1	ICL232
45	1	U2	UA7805UC
46	4	U3,U6,U7,U8	TL494RRI
47	2	U4,U5	LF347RRI
48	1	U9	7404
49	1	U10	74HCT238
50	5	U11,U12,U13,U14,U20	74HCT573
51	1	U15	80C31 BH
52	4	U16,U17,U18,U19	DAC0800
53	1	U21	AM27C64
54	1	U22	74HCT244
55	1	U23	LM324
56	1	U24	7400
57	2	U25,U26	7408
58	2	U27,U28	L298
59	1	Y1	CRYSTAL(11.0592Mhz)

### Connectors/headers

J1 RS 232 Connector	J6 Codes to PCB 1
J2 Supply to Driver 1	J7 Comparator o/p from PCB1
J3 Supply to Driver 2	J8 Unregulated supply from PCB 1
J4 Regulated supply from PCB1	J9 To motor 1
J5 Front panel switches	J10 To motor 2



## **Bibliography:**

Intel Component Data Catalog

Intel 8-bit Embedded Controller

RCA High-speed CMOS Logic ICs ( Harris Semiconductor )

Linear Data Book ( National Semiconductor Corporation )

Data Conversion Products Data Book ( Analog Devices )

Operational Amplifiers - Design and Applications ( Burr - Brown )

PC Systems Programming ( Abacus )

# 8031/8051/8751 SINGLE COMPONENT 8-BIT MICROCOMPUTER

- 8031 - Control Oriented CPU With RAM and I/O
  - 8051 - An 8031 With Factory Mask-Programmable ROM
  - 8751 - An 8031 With User Programmable/Erasable EPROM
- 
- 4K x 8 ROM/EPROM
  - Boolean Processor
  - 128 x 8 RAM
  - MCS-48® Architecture Enhanced with:
  - Four 8-Bit Ports, 32 I/O Lines
  - Non-Paged Jumps
    - Direct Addressing
    - Four 8-Register Banks
    - Stack Depth Up to 128-Bytes
    - Multiply, Divide, Subtract, Compare
  - Two 16-Bit Timer/Event Counters
  - Most Instructions Execute in 1µs
  - High-Performance Full-Duplex Serial Channel
  - 4µs Multiply and Divide
  - External Memory Expandable to 128K
  - Compatible with MCS-80®/MCS-85® Peripherals

The Intel® 8031/8051/8751 is a stand-alone, high-performance single-chip computer fabricated with Intel's highly-reliable +5 Volt, depletion-load, N-Channel, silicon-gate HMOS technology and packaged in a 40-pin DIP. It provides the hardware features, architectural enhancements and new instructions that are necessary to make it a powerful and cost effective controller for applications requiring up to 64K bytes of program memory and/or up to 64K bytes of data storage.

The 8051/8751 contains a non-volatile 4K x 8 read only program memory; a volatile 128 x 8 read/write data memory; 32 I/O lines; two 16-bit timer/counters; a five-source, two-priority-level, nested interrupt structure; a serial I/O port for either multi-processor communications, I/O expansion, or full duplex UART; and on-chip oscillator and clock circuits. The 8031 is identical, except that it lacks the program memory. For systems that require extra capability, the 8051 can be expanded using standard TTL compatible memories and the byte oriented MCS-80 and MCS-85 peripherals.

The 8051 microcomputer, like its 8048 predecessor, is efficient both as a controller and as an arithmetic processor. The 8051 has extensive facilities for binary and BCD arithmetic and excels in bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44% of one-byte, 41% two-byte, and 15% three-byte instructions. With a 12 MHz crystal, 58% of the instructions execute in 1µs, 40% in 2µs and multiply and divide require only 4µs. Among the many instructions added to the standard 8048 instruction set are multiply, divide, subtract and compare.

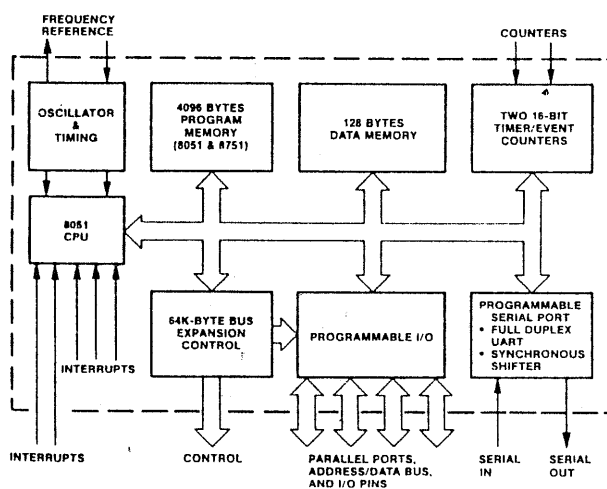


Figure 1.  
Block Diagram

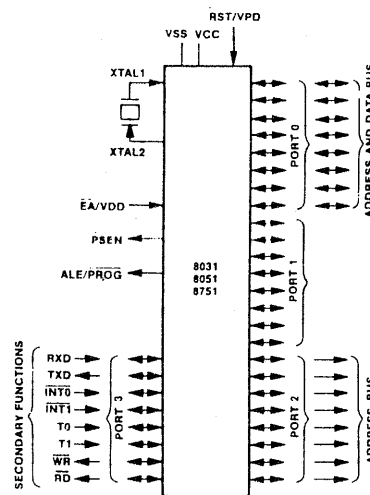


Figure 2.  
Logic Symbol

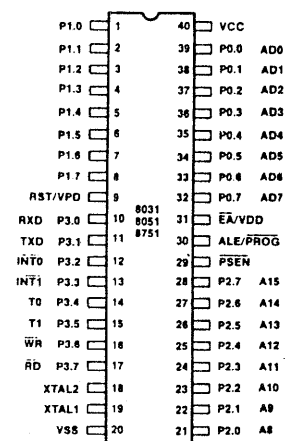


Figure 3. Pin Configuration

**ABSOLUTE MAXIMUM RATINGS\***

Ambient Temperature Under Bias . . . . 0°C to +70°C  
 Storage Temperature . . . . . -65°C to +150°C  
 Voltage on any  
   Pin to V<sub>SS</sub> . . . . . -0.5V to V<sub>CC</sub> + 0.5V  
 Voltage on V<sub>CC</sub> to V<sub>SS</sub> . . . . . -0.5V to 6.5V  
 Maximum I<sub>OL</sub> per I/O pin . . . . . 15 mA  
 Power Dissipation . . . . . 1.0W\*

\*This value is based on the maximum allowable die temperature and the thermal resistance of the package.

*\*Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

**NOTICE:** Specifications contained within the following tables are subject to change.

**D.C. CHARACTERISTICS** (T<sub>A</sub> = 0°C to 70°C; V<sub>CC</sub> = 5V ± 20%; V<sub>SS</sub> = 0V)

Symbol	Parameter	Min	Typ <sup>(3)</sup>	Max	Unit	Test Conditions
V <sub>IL</sub>	Input Low Voltage (Except $\bar{E}A$ )	-0.5		0.2 V <sub>CC</sub> - 0.1	V	
V <sub>IL1</sub>	Input Low Voltage ( $\bar{E}A$ )	-0.5		0.2 V <sub>CC</sub> - 0.3	V	
V <sub>IH</sub>	Input High Voltage (Except XTAL1, RST)	0.2 V <sub>CC</sub> + 0.9		V <sub>CC</sub> + 0.5	V	
V <sub>IH1</sub>	Input High Voltage (XTAL1, RST)	0.7 V <sub>CC</sub>		V <sub>CC</sub> + 0.5	V	
V <sub>OL</sub>	Output Low Voltage <sup>(6)</sup> (Ports 1, 2, 3)			0.45	V	I <sub>OL</sub> = 1.6 mA <sup>(1)</sup>
V <sub>OL1</sub>	Output Low Voltage <sup>(6)</sup> (Port 0, ALE, $\bar{P}SEN$ )			0.45	V	I <sub>OL</sub> = 3.2 mA <sup>(1)</sup>
V <sub>OH</sub>	Output High Voltage (Ports 1, 2, 3, ALE, $\bar{P}SEN$ )	2.4			V	I <sub>OH</sub> = -60 μA V <sub>CC</sub> = 5V ± 10%
		0.75 V <sub>CC</sub>			V	I <sub>OH</sub> = -25 μA
		0.9 V <sub>CC</sub>			V	I <sub>OH</sub> = -10 μA
V <sub>OH1</sub>	Output High Voltage (Port 0 in External Bus Mode)	2.4			V	I <sub>OH</sub> = -800 μA V <sub>CC</sub> = 5V ± 10%
		0.75 V <sub>CC</sub>			V	I <sub>OH</sub> = -300 μA
		0.9 V <sub>CC</sub>			V	I <sub>OH</sub> = -80 μA <sup>(2)</sup>
I <sub>IL</sub>	Logical 0 Input Current (Ports 1, 2, 3)			-50	μA	V <sub>IN</sub> = 0.45V
I <sub>TL</sub>	Logical 1 to 0 Transition Current (Ports 1, 2, 3)			-650	μA	V <sub>IN</sub> = 2V
I <sub>LI</sub>	Input Leakage Current (Port 0, $\bar{E}A$ )			± 10	μA	0.45 < V <sub>IN</sub> < V <sub>CC</sub>
RRST	Reset Pulldown Resistor	50		150	KΩ	
CIO	Pin Capacitance			10	pF	Test Freq = 1 MHz, T <sub>A</sub> = 25°C
I <sub>CC</sub>	Power Supply Current: Active Mode, 12 MHz <sup>(4)</sup> Idle Mode, 12 MHz <sup>(4)</sup> Power Down Mode		11	20	mA	(5)
			1.7	5	mA	
			5	50	μA	

## 2764 (8K x 8) UV ERASABLE PROM

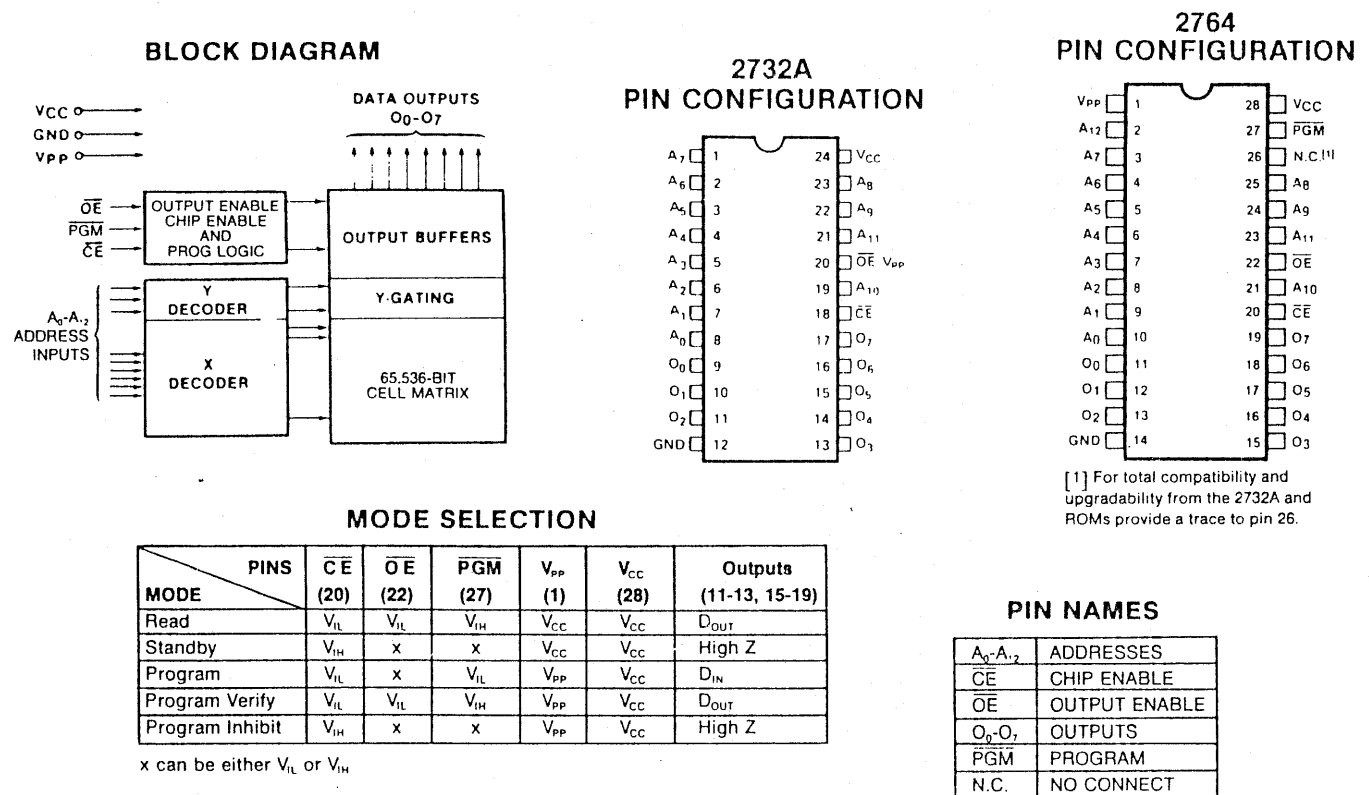
- 200 ns (2764-2) Maximum Access Time . . . HMOS\*-E Technology
- Compatible to High Speed 8MHz 8086-2 MPU . . . Zero WAIT State
- Two Line Control
- Pin Compatible to 2732A EPROM
- Industry Standard Pinout . . . JEDEC Approved
- Low Active Current...100mA Max.

The Intel® 2764 is a 5V only, 65,536-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The standard 2764 access time is 250ns with speed selection available at 200ns. The access time is compatible to high performance microprocessors, such as Intel's 8MHz 8086-2. In these systems, the 2764 allows the microprocessor to operate without the addition of WAIT states.

An important 2764 feature is the separate output control, Output Enable ( $\overline{OE}$ ) from the Chip Enable control ( $\overline{CE}$ ). The  $\overline{OE}$  control eliminates bus contention in multiple bus microprocessor systems. Intel's Application Note AP-72 describes the microprocessor system implementation of the  $\overline{OE}$  and  $\overline{CE}$  controls on Intel's EPROMs. AP-72 is available from Intel's Literature Department.

The 2764 has a standby mode which reduces the power dissipation without increasing access time. The active current is 150mA while the standby current is only 50mA. The standby mode is achieved by applying a TTL-high signal to the  $\overline{CE}$  input.

The 2764 is fabricated with HMOS\*-E technology, Intel's high-speed N-channel MOS Silicon Gate Technology.



\*HMOS is a patented process of Intel Corporation.

## ERASURE CHARACTERISTICS

The erasure characteristics of the 2764 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000 Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical 2764 in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the 2764 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the 2764 window to prevent unintentional erasure.

The recommended erasure procedure for the 2764 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15 W-sec/cm<sup>2</sup>. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 μW/cm<sup>2</sup> power rating. The 2764 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

## DEVICE OPERATION

The five modes of operation of the 2764 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V<sub>PP</sub>.

TABLE 1. MODE SELECTION

MODE \ PINS	$\overline{CE}$ (20)	$\overline{OE}$ (22)	PGM (27)	V <sub>PP</sub> (1)	V <sub>CC</sub> (28)	Outputs (11-13, 15-19)
Read	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>CC</sub>	V <sub>CC</sub>	D <sub>OUT</sub>
Standby	V <sub>IH</sub>	x	x	V <sub>CC</sub>	V <sub>CC</sub>	High Z
Program	V <sub>IL</sub>	x	V <sub>IL</sub>	V <sub>PP</sub>	V <sub>CC</sub>	D <sub>IN</sub>
Program Verify	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>PP</sub>	V <sub>CC</sub>	D <sub>OUT</sub>
Program Inhibit	V <sub>IH</sub>	x	x	V <sub>PP</sub>	V <sub>CC</sub>	High Z

x can be either V<sub>IL</sub> or V<sub>IH</sub>

## READ MODE

The 2764 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ( $\overline{CE}$ ) is the power control and should be used for device selection. Output Enable ( $\overline{OE}$ ) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t<sub>ACC</sub>) is equal to the delay from  $\overline{CE}$  to output (t<sub>CE</sub>). Data is available at the outputs after the falling edge of  $\overline{OE}$ , assuming that  $\overline{CE}$  has been low and addresses have been stable for at least t<sub>ACC</sub> - t<sub>OE</sub>.

## Standby Mode

The 2764 has a standby mode which reduces the active power current from 150mA to 50mA. The 2764 is placed in the standby mode by applying a TTL high signal to the  $\overline{CE}$  input. When in standby mode, the outputs are in a high impedance state, independent of the  $\overline{OE}$  input.

## Output OR-Tieing

Because EPROMs are usually used in larger memory arrays, Intel has provided a 2 line control function that accommodates this use of multiple memory connection. The two line control function allows for:

- the lowest possible memory power dissipation, and
- complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that  $\overline{CE}$  (pin 20) be decoded and used as the primary device selecting function, while  $\overline{OE}$  (pin 22) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

## PROGRAMMING (See Programming Instruction Section for Waveforms.)

Programming is the same as Intel's 2732A except that  $\overline{OE}/V_{PP}$  is not multiplexed. They have separate pins. Like the 2732A, **exceeding 21.5V will damage the 2764.**

Initially, and after each erasure, all bits of the 2764 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The 2764 is in the programming mode when V<sub>PP</sub> input is at 21V and  $\overline{CE}$  and PGM are both at TTL low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

For programming,  $\overline{CE}$  should be kept TTL low at all times while V<sub>PP</sub> is kept at 21V. When the address and data are stable, a 50 msec, active low, TTL program pulse is applied to PGM input. A program pulse must be applied at each address location to be programmed. You can program any location at any time—either individually, sequentially, or at random. The program pulse has a maximum width of 55 msec.

Programming of multiple 2764s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled 2764s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the PGM input programs the paralleled 2764s.

**PROGRAMMING**

The programming specifications are described in the Data Catalog PROM/ROM Programming Instructions Section.

**ABSOLUTE MAXIMUM RATINGS\***

Temperature Under Bias	-10°C to +80°C
Storage Temperature	-65°C to +125°C
Input or Output Voltages with Respect to Ground	+6V to -0.6V
Program Supply Voltage with Respect to Ground During Programming	+22V to -0.6V

## \* COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**D.C. and A.C. Operating Conditions During Read**

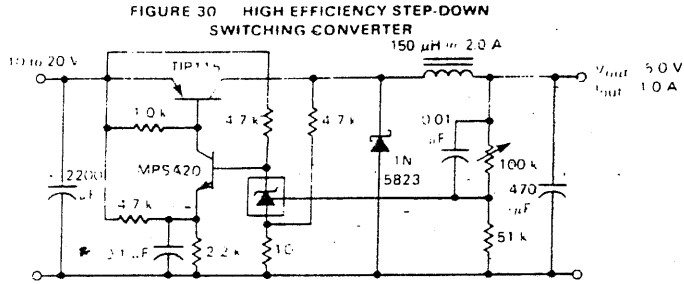
	2764	2764-2	2764-3	2764-4
Operating Temperature Range	0°C-70°C	0°C-70°C	0°C-70°C	0°C-70°C
V <sub>CC</sub> Power Supply <sup>1,2</sup>	5V ± 5%	5V ± 5%	5V ± 5%	5V ± 5%
V <sub>PP</sub> Voltage <sup>2</sup>	V <sub>PP</sub> = V <sub>CC</sub>	V <sub>PP</sub> = V <sub>CC</sub>	V <sub>PP</sub> = V <sub>CC</sub>	V <sub>PP</sub> = V <sub>CC</sub>

**READ OPERATION****D.C. AND OPERATING CHARACTERISTICS**

Symbol	Parameter	Limits			Unit	Conditions
		Min	Typ <sup>3</sup>	Max		
I <sub>LI</sub>	Input Load Current			10	μA	V <sub>IN</sub> = 5.25V
I <sub>LO</sub>	Output Leakage Current			10	μA	V <sub>OUT</sub> = 5.25V
I <sub>PP1</sub> <sup>2</sup>	V <sub>PP</sub> Current Read			15	mA	V <sub>PP</sub> = 5.25V
I <sub>CC1</sub> <sup>2</sup>	V <sub>CC</sub> Current Standby			50	mA	$\overline{CE} = V_{IH}$
I <sub>CC2</sub> <sup>2</sup>	V <sub>CC</sub> Current Active		70	150	mA	$\overline{CE} = \overline{OE} = V_{IL}$
V <sub>IL</sub>	Input Low Voltage	-0.1		+0.8	V	
V <sub>IH</sub>	Input High Voltage	2.0		V <sub>CC</sub> +1	V	
V <sub>OL</sub>	Output Low Voltage			0.45	V	I <sub>OL</sub> = 2.1 mA
V <sub>OH</sub>	Output High Voltage	2.4			V	I <sub>OH</sub> = -400 μA

- NOTES: 1. V<sub>CC</sub> must be applied simultaneously or before V<sub>PP</sub> and removed simultaneously or after V<sub>PP</sub>.  
 2. V<sub>PP</sub> may be connected directly to V<sub>CC</sub> except during programming. The supply current would then be the sum of I<sub>CC</sub> and I<sub>PP1</sub>.  
 3. Typical values are for T<sub>A</sub> = 25°C and nominal supply voltages.

# TL431,A Series



TEST	CONDITIONS	RESULTS
Line Regulation	$V_{in} = 10\text{V to } 20\text{V}$ , $I_o = 1.0\text{A}$	53 mV (1.1%)
Load Regulation	$V_{in} = 15\text{V}$ , $I_o = 0\text{A to } 1.0\text{A}$	25 mV (0.5%)
Output Ripple	$V_{in} = 10\text{V}$ , $I_o = 1.0\text{A}$	50 mV <sub>p-p</sub> P.A.R.D.
Output Ripple	$V_{in} = 20\text{V}$ , $I_o = 1.0\text{A}$	100 mV <sub>p-p</sub> P.A.R.D.
Efficiency	$V_{in} = 15\text{V}$ , $I_o = 1.0\text{A}$	82%

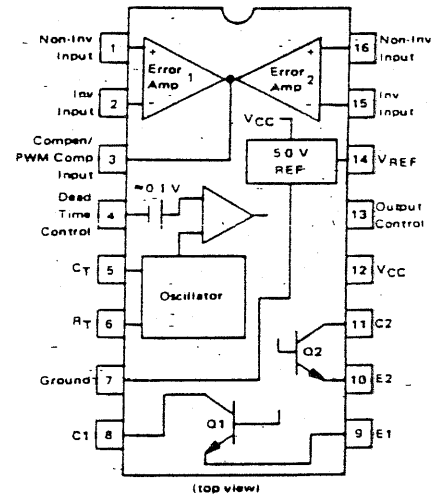


**MOTOROLA**

## SWITCHMODE PULSE WIDTH MODULATION CONTROL CIRCUITS

The TL494 is a fixed frequency, pulse width modulation control circuit designed primarily for Switchmode power supply control. This device features:

- Complete Pulse Width Modulation Control Circuitry
- On-Chip Oscillator With Master Or Slave Operation
- On-Chip Error Amplifiers
- On-Chip 5 Volt Reference
- Adjustable Dead-Time Control
- Uncommitted Output Transistors Rated to 500 mA Source Or Sink
- Output Control For Push-Pull Or Single-Ended Operation
- Undervoltage Lockout



The TL494C is specified over the commercial operating range of 0°C to 70°C. The TL494I is specified over the industrial range of -25°C to 85°C. The TL494M is specified over the full military range of -55°C to 125°C.

# TL494

## SWITCHMODE PULSE WIDTH MODULATION CONTROL CIRCUITS

SILICON MONOLITHIC INTEGRATED CIRCUITS



J SUFFIX  
CERAMIC PACKAGE  
CASE 620-10



N SUFFIX  
PLASTIC PACKAGE  
CASE 648-08

### ORDERING INFORMATION

Device	Temperature	
	Range	Package
TL494CN	0° to +70°C	Plastic DIP
TL494CJ	0 to +70°C	Ceramic DIP
TL494IN	25 to +85°C	Plastic DIP
TL494IJ	25 to +85°C	Ceramic DIP
TL494M	55 to +125°C	Ceramic DIP

# TL494

FIGURE 1 — BLOCK DIAGRAM

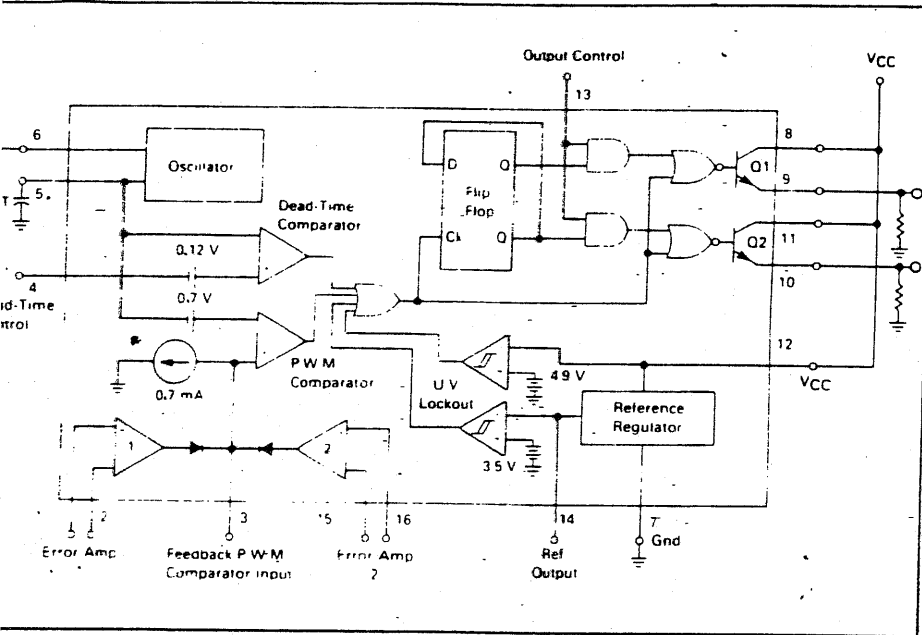
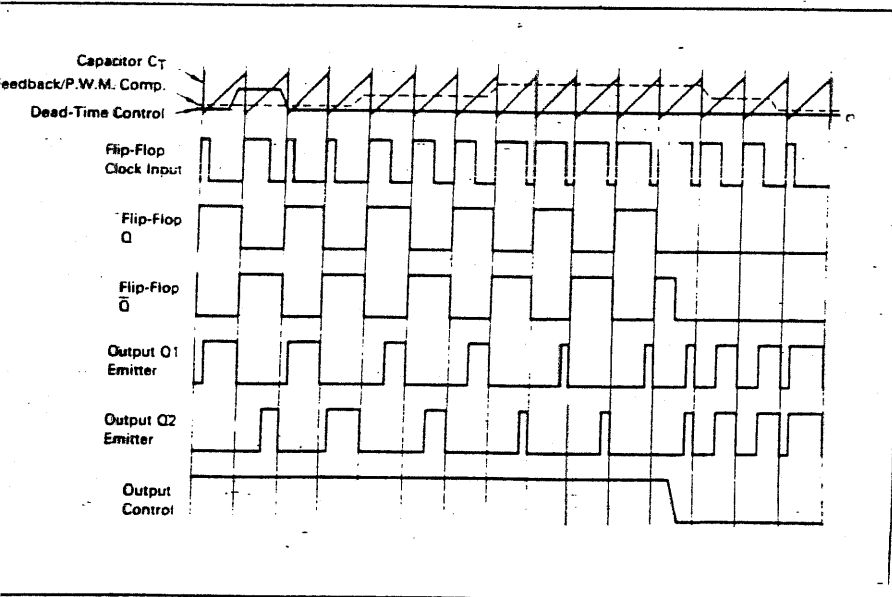


FIGURE 2 — TIMING DIAGRAM



# TL494

## MAXIMUM RATINGS (Full operating ambient temperature range applies unless otherwise noted)

Rating	Symbol	TL494C	TL494I	TL494M	Unit
Power Supply Voltage	V <sub>CC</sub>	42	42	42	V
Collector Output Voltage	V <sub>C1</sub> , V <sub>C2</sub>	42	42	42	V
Collector Output Current (each transistor) (I <sub>C</sub> )	I <sub>C1</sub> , I <sub>C2</sub>	500	500	500	mA
Amplifier Input Voltage Range	V <sub>IR</sub>	-0.3 to 42	0.3 to 42	0.3 to 42	V
Power Dissipation (T <sub>A</sub> = 45°C)	P <sub>D</sub>	1000	1000	1000	mW
Operating Junction Temperature	T <sub>J</sub>				
Plastic Package		125	125	—	°C
Ceramic Package		150	150	150	°C
Operating Ambient Temperature Range	T <sub>A</sub>	0 to 70	25 to 85	55 to 125	°C
Storage Temperature Range	T <sub>stg</sub>				
Plastic Package		55 to 125	55 to 125	—	°C
Ceramic Package		65 to 150	65 to 150	65 to 150	°C

NOTE 1: Maximum thermal limits must be observed.

## THERMAL CHARACTERISTICS

Characteristics	Symbol	N Suffix Plastic Package	J Suffix Ceramic Package	Unit
Thermal Resistance, Junction to Ambient	R <sub>θJA</sub>	80	100	°C/W
Derating Ambient Temperature	T <sub>A</sub>	45	50	°C

## RECOMMENDED OPERATING CONDITIONS

Condition/Value	Symbol	TL494			Unit
		Min	Typ	Max	
Power Supply Voltage	V <sub>CC</sub>	7.0	15	40	V
Collector Output Voltage	V <sub>C1</sub> , V <sub>C2</sub>	—	30	40	V
Collector Output Current (each transistor)	I <sub>C1</sub> , I <sub>C2</sub>	—	—	200	mA
Amplifier Input Voltage	V <sub>in</sub>	-0.3	—	V <sub>CC</sub> - 2.0	V
Current into Feedback Terminal	I <sub>fb</sub>	—	—	±3	mA
Reference Output Current	I <sub>ref</sub>	—	—	10	mA
Timing Resistor	R <sub>T</sub>	1.8	30	500	kΩ
Timing Capacitor	C <sub>T</sub>	0.0047	0.001	10	μF
Oscillator Frequency	f <sub>osc</sub>	1.0	40	200	kHz

## ELECTRICAL CHARACTERISTICS (V<sub>CC</sub> = 15 V, C<sub>T</sub> = 0.01 μF, R<sub>T</sub> = 12 kΩ unless otherwise noted.)

For typical values T<sub>A</sub> = 25°C, for min/max values T<sub>A</sub> is the operating ambient temperature range that applies unless otherwise noted.

Characteristic	Symbol	TL494C,I			TL494M			Unit
		Min	Typ	Max	Min	Typ	Max	

## REFERENCE SECTION

Reference Voltage (I <sub>O</sub> = 10 mA)	V <sub>ref</sub>	4.75	5.0	5.25	4.75	5.0	5.25	V
Line Regulation (V <sub>CC</sub> = 7.0 V to 40 V)	Reg <sub>line</sub>	—	20	25	—	20	25	mV
Load Regulation (I <sub>O</sub> = 10 mA to 10 mA)	Reg <sub>load</sub>	—	30	15	—	30	15	mV
Short-Circuit Output Current (V <sub>ref</sub> = 0 V)	I <sub>SC</sub>	15	35	75	15	35	75	mA



# LINEAR INTEGRATED CIRCUITS

## Dual Full-Bridge Driver Power

*Amuth*

### FEATURES

- Operating Supply Voltage up to 46V
- Total Saturation Voltage 3.4V max at 1A
- Overtemperature Protected
- Operates in Switched and Linear Regulation Modes
- 25W Power-Tab Package for Low Installed Cost
- Individual Logic Inputs for Each Driver
- Channel-Enable Logic Inputs for Driver Pairs

### DESCRIPTION

The L298 is a power integrated circuit usable for driving resistive and inductive loads. This device contains four push-pull drivers with separate logic inputs. Two enable inputs are provided for power down and chopping. Each driver is capable of driving loads up to 2A continuously.

Logic inputs to the L298 have high input thresholds (1.85V) and hysteresis to provide trouble-free operation in noisy environments normally associated with motors and inductors. The L298 input currents and thresholds allow the device to be driven by TTL and CMOS systems without buffering or level shifting.

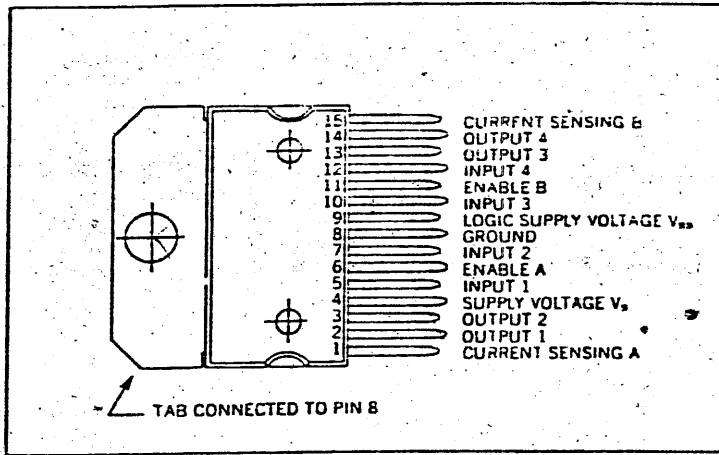
The emitters of the low-side power drivers are separately available for current sensing. Feedback from the emitters can be used to control load current in a switching mode, or can be used to detect load faults.

Separate logic and load supply lines are provided to reduce total IC power consumption. Power consumption is reduced further when the enable inputs are low. This makes the L298 ideal for systems that require low standby current, such as portable or battery-operated equipment.

### ABSOLUTE MAXIMUM RATINGS

Power Supply, $V_s$ .....	50V
Logic Supply Voltage, $V_{SS}$ .....	7V
Input and Inhibit Voltage, $V_i, V_{inhibit}$ .....	-0.3V to +7V
Peak Output Current (each channel), $I_o$	
Non-Repetitive ( $t = 100\mu s$ ).....	3A
Repetitive (80% on - 20% off; $t_{ON} = 10ms$ ).....	2.5A
IC Operation.....	2A
Sensing Voltage, $V_{sense}$ .....	-1V to +2.3V
Total Power Dissipation ( $T_{case} = 75^\circ C$ ), $P_{tot}$ .....	25W
Storage and Junction Temperature, $T_{sig}, T_j$ .....	-40°C to +150°C

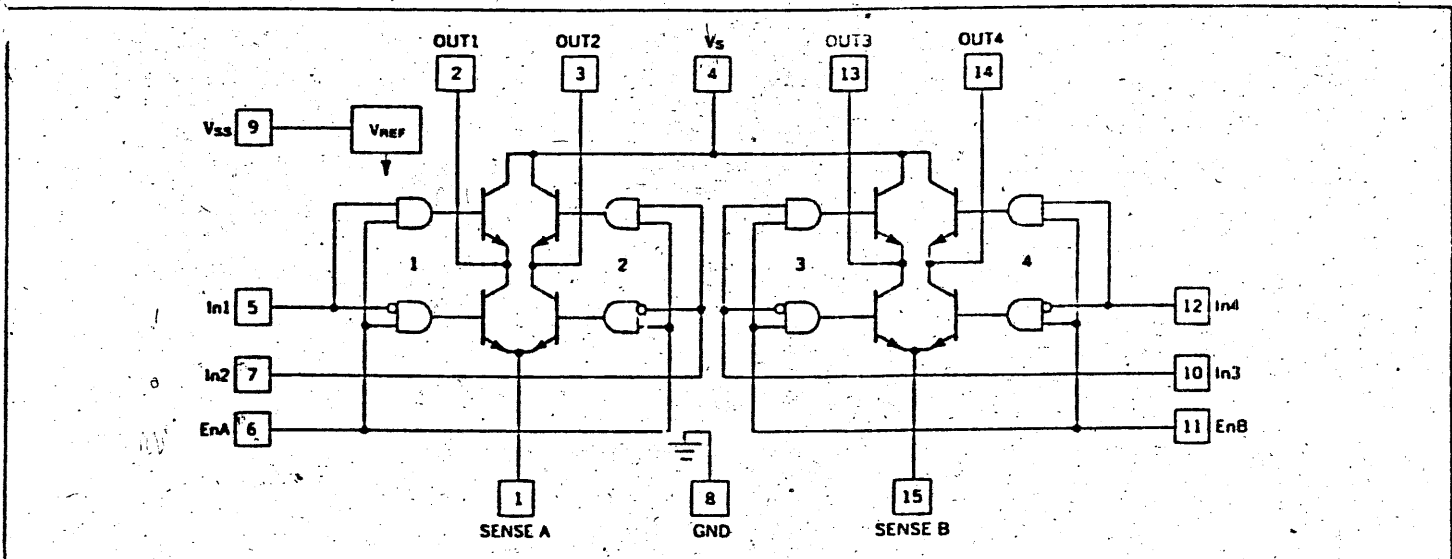
### CONNECTION DIAGRAM



### THERMAL DATA

Thermal Resistance Junction-Case, $R_{th j-case}$ .....	3°C/W max.
Thermal Resistance Junction-Ambient, $R_{th j-amb}$ .....	35°C/W max.

### BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (for each channel,  $V_s = 42V$ ,  $V_{ss} = 5V$ ,  $T_j = 25^\circ C$ )

PARAMETERS	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Voltage (Pin 4), $V_s$	Operative Condition	$V_{IH} + 2.5$		46	V
Logic Supply Voltage (Pin 9), $V_{ss}$		4.5		7	V
Quiescent Supply Current (Pin 4), $I_s$	$V_{inn.} = H$ $V_i = L$		3	7	mA
	$I_L = 0$ $V_i = H$		15	20	
	$V_{inn.} = L$			1	
Quiescent Current from $V_{ss}$ (Pin 9), $I_{ss}$	$V_{inn.} = H$ $V_i = L$		5	10	mA
	$I_L = 0$ $V_i = H$		1.5	3	
	$V_{inn.} = L$		1	1.5	
Input Low Voltage (Pins 5, 7, 10, 12), $V_i L$		-0.3		1.5	V
Input High Voltage (Pins 5, 7, 10, 12), $V_i H$		2.3		$V_{ss}$	V
Low Voltage Input Current (Pins 5, 7, 10, 12), $I_{iL}$	$V_i = L$			-10	$\mu A$
High Voltage Input Current (Pins 5, 7, 10, 12), $I_{iH}$	$V_i = H$		30	100	
Inhibit Low Voltage (Pins 6, 11), $V_{inn. L}$		-0.3		1.5	V
Inhibit High Voltage (Pins 6, 11), $V_{inn. H}$		2.3		7	V
Low Voltage Inhibit Current (Pins 6, 11), $I_{inn. L}$	$V_{inn.} = L$			-10	$\mu A$
High Voltage Inhibit Current (Pins 6, 11), $I_{inn. H}$	$V_{inn.} = H \leq V_{ss} - 0.6V$		30	100	
Source Saturation Voltage, $V_{CE sat(H)}$	$I_L = 1A$		1.2	1.8	V
	$I_L = 2A$		1.8	2.8	
Sink Saturation Voltage, $V_{CE sat(L)}$	$I_L = 1A$		1.2	1.8	V
	$I_L = 2A$		1.7	2.6	
Total Drop, $V_{CE sat}$	$I_L = 1A$			3.4	V
	$I_L = 2A$			5.2	
Sensing Voltage (Pins 1, 15), $V_{sens}$		$-1^{(1)}$		2	V
Source Current Turn-Off Delay, $T_1(V_i)$	$0.5 V_i$ to $0.9 I_L^{(2)}$		1.7		$\mu s$
Source Current Fall Time, $T_2(V_i)$	$0.9 I_L$ to $0.1 I_L^{(2)}$		0.2		$\mu s$
Source Current Turn-On Delay, $T_3(V_i)$	$0.5 V_i$ to $0.1 I_L^{(2)}$		2.5		$\mu s$
Source Current Rise Time, $T_4(V_i)$	$0.1 I_L$ to $0.9 I_L^{(2)}$		0.35		$\mu s$
Sink Current Turn-Off Delay, $T_5(V_i)$	$0.5 V_i$ to $0.9 I_L^{(3)}$		0.7		$\mu s$
Sink Current Fall Time, $T_6(V_i)$	$0.9 I_L$ to $0.1 I_L^{(3)}$		0.2		$\mu s$
Sink Current Turn-On Delay, $T_7(V_i)$	$0.5 V_i$ to $0.1 I_L^{(3)}$		1.5		$\mu s$
Sink Current Rise Time, $T_8(V_i)$	$0.1 I_L$ to $0.9 I_L^{(3)}$		0.2		$\mu s$
Commutation Frequency, $f_c$	$I_L = 2A$		25	40	KHz

1) Sensing voltage can be  $-1V$  for  $t \leq 50\mu s$ ; in steady state  $V_{sens} \min \geq -0.5V$ .

2) See figure 1a.

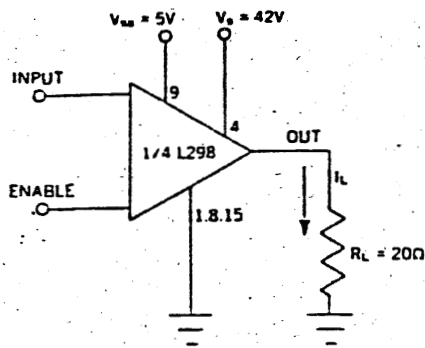
3) See figure 2a.

elkom ag

Elektronische Komponenten  
Dorfstrasse 30.

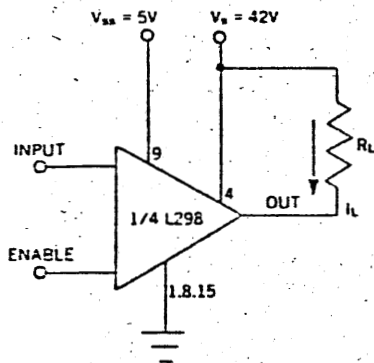
**SWITCHING CHARACTERISTICS**

Figure 1. Switching times test circuits.



NOTE: For INPUT chopper, set EN = H.

Figure 2. Switching Times Test Circuits.



NOTE: For INPUT chopper, set EN = H.

Figure 1a. Source Current Delay Times vs. Input or Enable Chopper

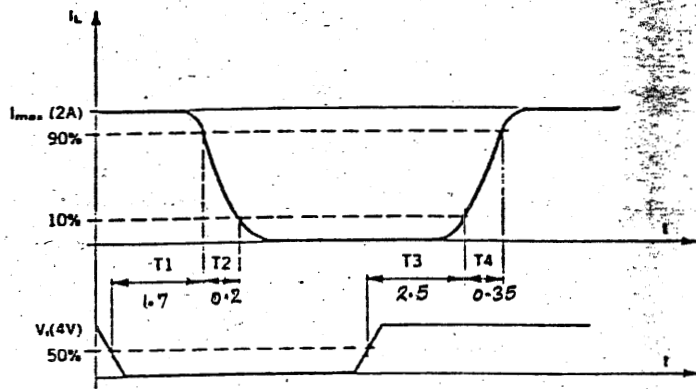
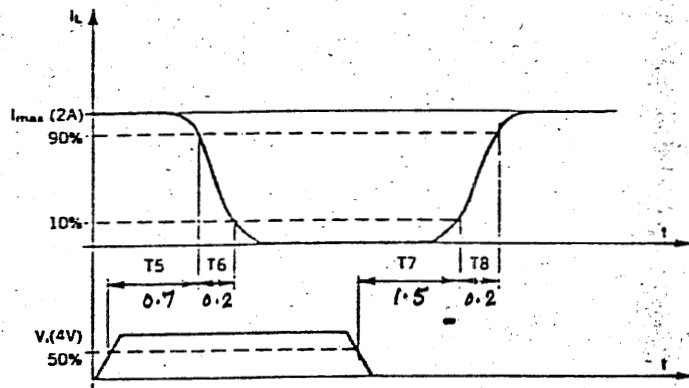
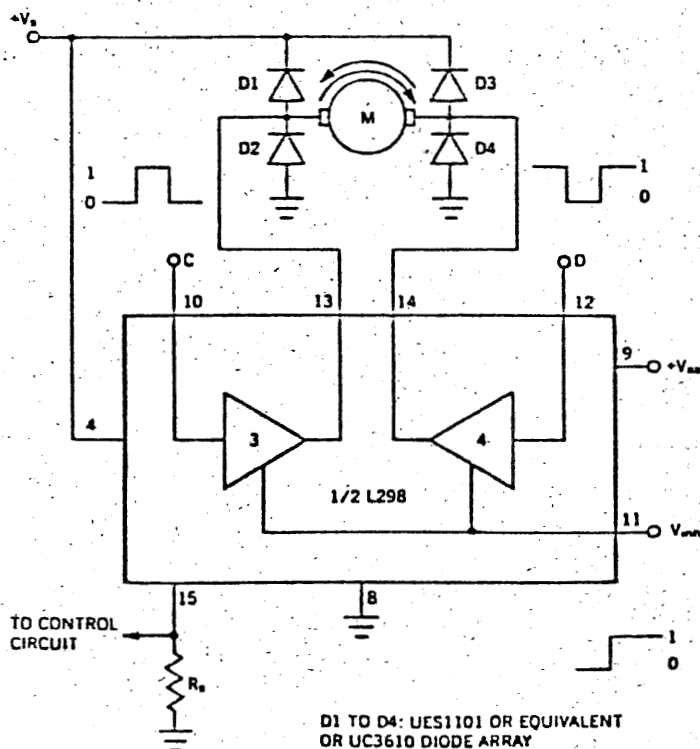


Figure 2a. Sink Current Delay Times vs. Input or Enable Chopper.



**APPLICATIONS**

Figure 3. Bi-Directional DC Motor Control.



D1 TO D4: UES1101 OR EQUIVALENT OR UC3610 DIODE ARRAY

	INPUTS	FUNCTION
V <sub>inh.</sub> = H	C = H; D = L	Turn right
	C = L; D = H	Turn left
	C = D	Fast motor stop
V <sub>inh.</sub> = L	C = X; D = C	Free running motor stop

L = Low  
H = High  
X = Don't Care

# ICL232 +5 Volt Powered Dual RS-232 Transmitter/Receiver



## GENERAL DESCRIPTION

The ICL232 is a dual RS-232 transmitter/receiver interface circuit that meets all EIA RS-232C specifications. It requires a single +5V power supply, and features two on-board charge pump voltage converters which generate +10V and -10V supplies from the 5V supply.

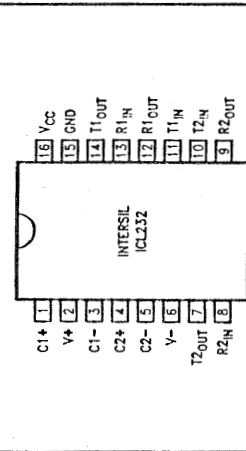
The drivers feature true TTL/CMOS input compatibility, slew-rate-limited output, and 300 ohms power-off source impedance. The receivers can handle up to ±30 volts, and have a 3 to 7 kilohms input impedance. The receivers also have hysteresis to improve noise rejection.

## Typical Applications

- Any System Requiring RS-232 Communications Port:
- Computers—Portable and Mainframe
- Peripherals—Printers and Terminals
- Portable Instrumentation
- Modems
- Dataloggers

## ORDERING INFORMATION

Part	Temperature Range	Package
ICL232CPE	0°C to +70°C	16 Pin Plastic DIP
ICL232CJE		16 Pin CERDIP
ICL232PIE	-25°C to +85°C	16 Pin Plastic DIP
ICL232JIE		16 Pin CERDIP
ICL232MJE	-55°C to +125°C	16 Pin CERDIP



Outline Drawing (PE, JE)  
Figure 1: Pin Configuration

0100-2

## FEATURES

- Meets All RS-232C Specifications
- Requires Only Single +5V Power Supply
- Onboard Voltage Quadrupler
- Low Power Consumption
- ESD Protection > 2000V
- 2 Drivers
- ±5V Output Swing for +5V Input
- 300 Ohms Power-off Source Impedance
- Output Current Limiting
- TTL/CMOS Compatible
- 30 V/μs Maximum Slew Rate
- 2 Receivers
- ±30V Input Voltage Range
- 3 to 7 kohms Input Impedance
- 0.5V Hysteresis to Improve Noise Rejection
- All Critical Parameters are Guaranteed Over the Entire Commercial, Industrial and Military Temperature Ranges

## ICL232

### ABSOLUTE MAXIMUM RATINGS

- V<sub>CC</sub> to ground ..... +6 Volts
- V<sup>+</sup> to ground ..... +12 Volts
- V<sup>-</sup> to ground ..... -12 Volts
- Input Voltages
- T<sub>1in</sub>, T<sub>2in</sub> ..... -0.3 to (V<sub>CC</sub> + 0.3V)
- R<sub>1in</sub>, R<sub>2in</sub> ..... ±30V
- Output Voltages
- T<sub>1out</sub>, T<sub>2out</sub> ..... (V<sup>+</sup> + 0.3) to (V<sup>-</sup> - 0.3V)
- R<sub>1out</sub>, R<sub>2out</sub> ..... -0.3 to (V<sub>CC</sub> + 0.3V)
- Short Circuit Duration
- T<sub>1out</sub>, T<sub>2out</sub> ..... Continuous
- Continuous Total Power Dissipation (T<sub>a</sub> = 25°C)  
CERDIP Package ..... 500mW  
Plastic Package ..... 375mW  
derate 9.5 mW/°C above 70°C  
derate 7.0 mW/°C above 70°C

- Storage Temperature Range ..... -55°C to +150°C
- Lead Temperature (Soldering, 10 sec) ..... +300°C
- Operating Temperature Range
- ICL232C ..... 0°C to +70°C
- ICL232I ..... -25°C to +85°C
- ICL232M ..... -55°C to +125°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the conventional sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

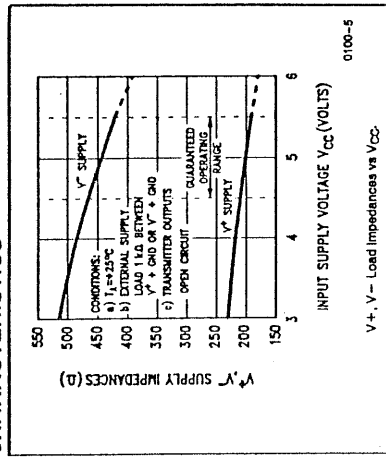
### ELECTRICAL CHARACTERISTICS

Test Conditions: V<sub>CC</sub> = +5V, T<sub>a</sub> = operating temperature range, Test Circuit as in Figure 3 (unless otherwise specified)

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Typ / Max	
T <sub>OUT</sub>	Transmitter Output Voltage Swing	T <sub>1out</sub> , T <sub>2out</sub> loaded with 3 kΩ to ground	±5	±9	±10 V
I <sub>CC</sub>	Power Supply Current	Outputs Unloaded, T <sub>a</sub> = 25°C		5	10 mA
V <sub>IL</sub>	T <sub>in</sub> Input Logic Low				0.8 V
V <sub>IH</sub>	T <sub>in</sub> Input Logic High			2.0	V
I <sub>p</sub>	Logic Pullup Current	T <sub>1in</sub> , T <sub>2in</sub> = 0V		15	230 μA
V <sub>in</sub>	RS-232 Input Voltage Range		-30		-30 V
F <sub>in</sub>	Receiver Input Impedance	V <sub>in</sub> = ±3V, ±25V	3.0	5.0	7.0 kΩ
V <sub>IHL</sub>	Receiver Input Low Threshold	V <sub>CC</sub> = 5.0V, T <sub>a</sub> = 25°C	0.8	1.2	V
V <sub>IHH</sub>	Receiver Input High Threshold	V <sub>CC</sub> = 5.0V, T <sub>a</sub> = 25°C		1.7	2.4 V
V <sub>HYST</sub>	Receiver Input Hysteresis		0.2	0.5	1.0 V
V <sub>OL</sub>	TTL/CMOS Receiver Output Voltage Low	I <sub>out</sub> = 3.2mA		0.1	0.4 V
V <sub>OH</sub>	TTL/CMOS Receiver Output Voltage High	I <sub>out</sub> = -1.0mA		3.5	4.6 V
t <sub>pd</sub>	Propagation Delay	RS-232 to TTL or TTL to RS-232		0.5	μs
SR	Instantaneous Slew Rate	C <sub>L</sub> = 10 pF, R <sub>L</sub> = 3 kΩ, T <sub>a</sub> = 25°C (Notes 1, 2)		30	V/μs
SR <sub>t</sub>	Transition Region Slew Rate	R <sub>L</sub> = 3 kΩ, C <sub>L</sub> = 2500 pF Measured from +3V to -3V or -3V to +3V		3	V/μs
R <sub>out</sub>	Output Resistances	V <sub>CC</sub> = V <sup>+</sup> = V <sup>-</sup> = 0V, V <sub>out</sub> = -Z <sub>L</sub>		300	Ω
I <sub>SC</sub>	RS-232 Output Short Circuit Current	T <sub>1out</sub> , T <sub>2out</sub> shorted to GND		±10	mA

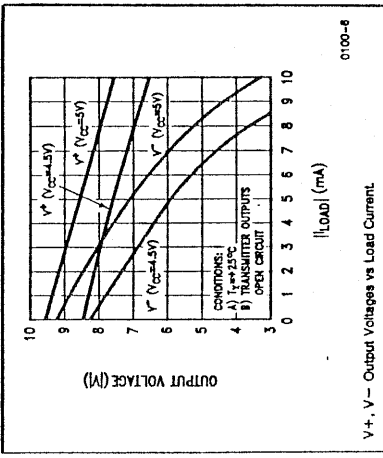
NOTE 1: Guaranteed by design.  
2: See Figure 5 for definition.

TYPICAL PERFORMANCE CHARACTERISTICS



0100-5

$V^+$ ,  $V^-$  - Load Impedances vs  $V_{CC}$ .



0100-6

$V^+$ ,  $V^-$  - Output Voltages vs Load Current.

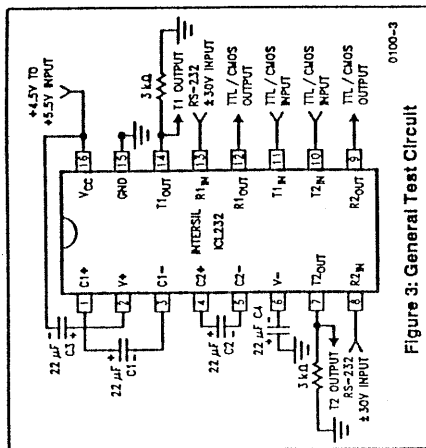


Figure 3: General Test Circuit

0100-3

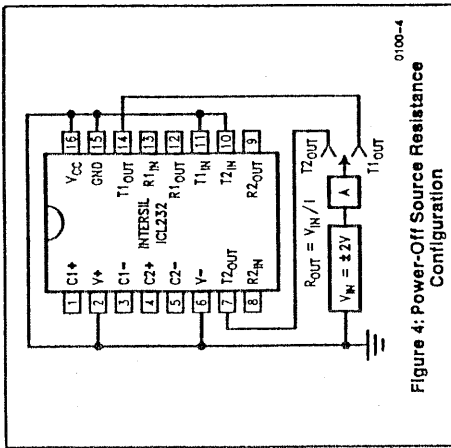


Figure 4: Power-Off Source Resistance Configuration

0100-4

DETAILED DESCRIPTION

The ICL232 is a dual RS-232 transmitter/receiver powered by a single +5V power supply which meets all EIA RS-232C specifications and features low power consumption. The functional diagram (Figure 2) illustrates the major elements of the ICL232. The circuit is divided into three sections: a voltage quadrupler, dual transmitters, and dual receivers.

Voltage Converter

The voltage quadrupler contains two charge pumps which use two phases of an internally generated clock to generate +10V and -10V. During phase two, the voltage on C1 is charged to  $V_{CC}$ . During phase two, the voltage on C1 is added to  $V_{CC}$ , producing a signal across C2 equal to twice  $V_{CC}$ . At the same time, C3 is also charged to  $2V_{CC}$ , and then during phase one, it is inverted with respect to ground to produce a signal across C4 equal to  $-2V_{CC}$ . The voltage converter accepts input voltages up to 5.5V. The output impedance of the doubler ( $V^+$ ) is approximately 200 ohms, and the output impedance of the inverter ( $V^-$ ) is approximately 450 ohms. The test circuit (Figure 3) uses 22 uF capacitors for C1-C4, however, the value is not critical. Increasing the values of C1 and C2 will lower the output impedance of the voltage doubler and inverter, and increasing the values of the reservoir capacitors, C3 and C4, lowers the ripple on the  $V^+$  and  $V^-$  supplies.

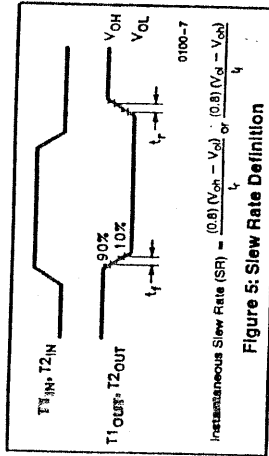


Figure 5: Slow Rate Definition

0100-7

Instantaneous Slow Rate (SR) =  $\frac{(0.8)(V_{OH} - V_{OL})}{t_r}$  or  $\frac{(0.8)(V_d - V_{OL})}{t_r}$

Transmitters

The transmitters are TTL/CMOS compatible inverters which translate the inputs to RS-232 outputs. The input logic threshold is about 26% of  $V_{CC}$  or 1.3V for  $V_{CC} = 5\text{V}$ . A logic 1 at the input results in a voltage of  $-5\text{V}$  and  $V^-$  at the output, and a logic 0 results in a voltage between +5V and ( $V^+ - 0.6\text{V}$ ). Each transmitter input has an internal 400 kilohm pullup resistor so any unused input can be left unconnected and its output remains in its low state. The output voltage swing meets the RS-232C specification of  $\pm 5\text{V}$  minimum with the worst case conditions of both transmitters driving 3kohm minimum load impedance,  $V_{CC} = 4.5\text{V}$ , and maximum allowable operating temperature. The transmitters have an internally limited output slew rate which is less than 30V/us. The outputs are short circuit protected and can be shorted to ground indefinitely. The powered down output impedance is a minimum of 300 ohms with  $\pm 2\text{V}$  applied to the outputs and  $V_{CC} = 0\text{V}$ .

Receivers

The receiver inputs accept up to  $\pm 30\text{V}$  while presenting the required 3 to 7 kilohms input impedance even if the power is off ( $V_{CC} = 0\text{V}$ ). The receivers have a typical input threshold of 1.3V which is within the  $\pm 3\text{V}$  limits, known as the transition region, of the RS-232 specification. The receiver output is 0V to  $V_{CC}$ . The output will be low whenever the input is greater than 2.4V and high whenever the input is floating or driven between +0.8V and  $-30\text{V}$ . The receivers feature 0.5V hysteresis to improve noise rejection.

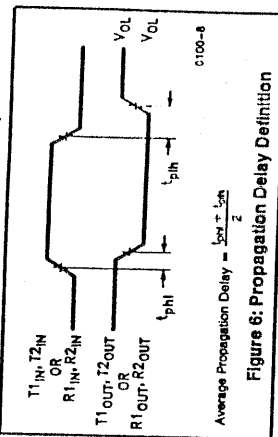


Figure 6: Propagation Delay Definition

0100-8

Average Propagation Delay =  $\frac{t_{PH} + t_{PL}}{2}$

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NOTE: All typical values have been characterized but are not tested.

## 7.9 Accessing the Serial Port from the BIOS

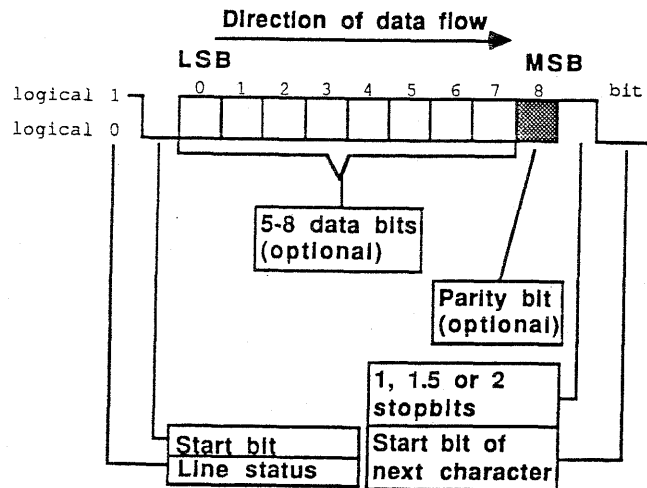
Computers in every part of the world communicate with each other and exchange data. Most of the time these computers use normal telephone lines for this communication. Phone lines only permit slow data transfer, but allow users to communicate from almost anywhere on the planet. Data transfers serially (i.e., one bit at a time), while the sender and receiver maintain similar *transfer protocols* (parameters for data transfer).

### Serial card

Since basic PC configurations aren't equipped for this type of data transmission, data transfer is only possible when the user adds an *asynchronous communication port* (IBM's catch phrase for an *RS-232 card*, or *serial interface card*).

This type of card enables data transfer between two computers direct through a cable or through phone lines. Both the sender and receiver require a *modem* to communicate using the latter method. Modems convert computer signals into acoustical signals which can then be transmitted over telephone lines.

In addition to hardware, data communication requires software which controls the RS-232 card. BIOS offers this software in four functions called by interrupt 14H. Before discussing these functions in detail, let's examine data transfer protocol.



Asynchronous transmission protocol

### Word length

As the figure above shows, only the two line states, 0 and 1 (also called high and low) are important. The line remains high if no data transmission takes place. If the line's state changes to low, the receiver knows that data is being transmitted. Between 5 and 8 bits transfer over the line, depending on the *word length*. Unfortunately the BIOS functions only support a word length of 7 or 8 bits. If the line is low during data transmission, this means that the bit to be sent is 0. High signals a set bit. The least significant bit is transferred first, and the most significant bit of the character to be transmitted is transferred last.

### Parity

The character can be followed by a *parity bit* which permits error detection during data transmission. Parity can be even or odd. For even parity, the parity bit augments the data word to be transmitted, so that an even number of bits results. For example, if the data word to be transmitted contains three bits set to 1, the parity bit becomes 1 so that the number of 1 bits increments to four, making an even number. If the data word contained an even number of 1 bits, the parity bit would be zero. For odd parity the parity bit is set in such a manner that the total number of 1 bits is odd.

### Stop bits

The *stop bits* signal the end of the transmission of data. Data transmission protocol permits 1, 1.5 and 2 stop bits. Some users are confused about the option of working with 1.5 stop bits, since some believe that you can't divide a bit. The explanation for this paradox comes from the data transmission protocol.

### Baud rate

Old standards dictate that data transfers at a rate of 300 *baud* (about 300 bits per second), and one stop bit. The signal for a 1 bit and the signal for a 0 bit are both *events*. Binary bits when transmitted in an analog environment such as phone lines may not be identical with baud rates. Since stop bits always have the value 1, the line would be high for 1/300 second. If instead you keep the line high for 1/200 second, 1.5 bits are transmitted. The line remains high until a new character transfers and sets the line transmitting the start bit to low.

Some interfaces work with negative logic. In such a case the conditions for 0 and 1 in the illustration above must be reversed. This doesn't change the basic principle of serial transmission.

### Protocol settings

Data transmission only works if the sender and receiver both match various protocol parameters. First the *baud rate* (the number of bits transmitted per second) must be set. The standard baud rates for data exchange over voice telephone lines are 300, 1200 and 2400 baud. These baud rates depend on the capabilities of the

modem in use. For a dedicated (data only) telephone line or for direct data transmission through a cable, speeds up to 9600 baud are possible. Up to 80 bytes per second or 4800 bytes per minute can be transmitted at 9600 baud.

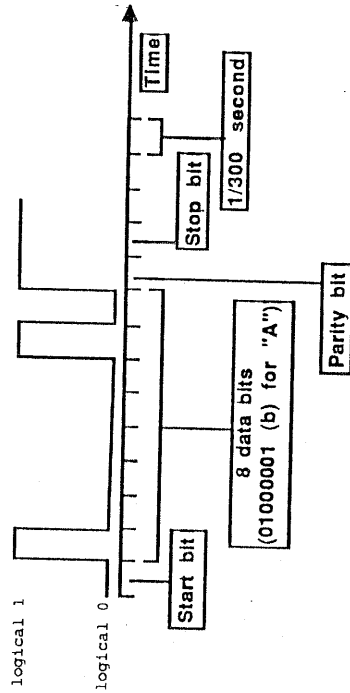
The *word length* depends on the data being transmitted. If the data consists of normal ASCII characters, a 7-bit word is enough, since the ASCII character set has only 128 characters. If the data encompasses the complete PC set of 256 characters, 8-bit words are more practical.

Next the necessity of a *parity check* should be determined, and whether even or odd parity should be used. In most cases parity checking is recommended, since phone lines do not always transmit all data correctly. The parity selected is unimportant, as long as both sender and receiver select the same parity.

The number of *stop bits* must be defined. One stop bit transmits successive characters faster than a setting of two stop bits. On the other hand, two stop bits increase the reliability of transmission.

#### Sample protocol

The following illustration shows a sample transmission of an "A" character with a protocol of 8 data bits, odd parity and one stop bit. Positive logic and a 300 baud transmission rate are assumed. Since the ASCII code of the "A" character is 65 (01000001(b)) and therefore contains only two 1 bits, the parity bit changes to 1 to set the number of 1 bits to an odd number.



Transmitting A character: 8-bit word length, 1 stop bit, odd parity and 300 baud

#### UART

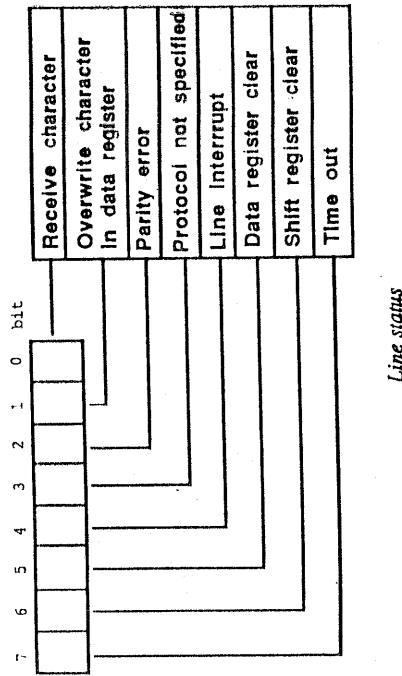
The brain of an RS-232 card is the UART (Universal Asynchronous Receiver Transmitter). You should be familiar with the design and capabilities of this processor, so that you can properly adapt programs to the error messages returned by the different BIOS functions.

#### Transfer registers

A character transmitted on a data line passes first to a register designated as a *transfer holding register*. It remains there until processing ends on the character preceding it. Then the character moves to the *transfer shift register* from where the UART transmits the character bit by bit over the data line. Depending on the configuration, parity and stop bits implement the stream of data. When the BIOS function passes the status of the data lines to the AH register, bits 5 and 6 indicate whether these two registers are empty.

#### Receiver registers

The *receiver shift register* accepts received data, then transmits the data to the *receiver data register* where the UART removes the parity and stop bits. If a previously received character is still in the data register, bit 1 of the line status sets to 1 to avoid overwriting. Bit 0 indicates that a character was received. If while processing the character, the UART discovers that a parity error occurred during the transmission, it sets bit 2 of the line status. If a breakdown occurs in the agreed-upon protocol (number of parity and stop bits), the action sets bit 3. The UART always sets bit 4 if the data line remains longer in low (0) status than required for the transmission of a character. Bit 7 signals a *time out* error. This occurs occasionally when the communication between the RS-232 card and the modem isn't working properly.



Function 0: Passing protocol

Before data can be transmitted or received, the UART must be informed of the number of stop bits, etc. Function 0 of interrupt 14H serves this purpose. The function number (0) enters the AH register, and the protocol passes to the AL register. The bits of the AL register indicate the various parameters:

Bits	Protocol
bit 0,1	Word length 10(b) - 7 bits 11(b) - 8 bits
bit 2	Number of Stop bits 0 - 1 Stop bit 1 - 2 Stop bits
bit 3,4	Parity check 00(b) - none 01(b) - odd 10(b) - even
bit 5 -7	Baud rate 000 - 110 Baud 001 - 150 Baud 010 - 300 Baud 011 - 600 Baud 100 - 1200 Baud 101 - 2400 Baud 110 - 4800 Baud 111 - 9600 Baud

After initialization the function loads the line status into the AH register.

#### Function 1: Transmit character

Function 1 transmits characters. During its call, the AH register must contain 1 and the AL register must contain the character to be transmitted. If the character was transmitted, bit 7 of the AH register changes to 0 after the function call. A 1 signals that the character could not be transmitted. The remaining bits correspond to the line status.

#### Function 2: Receive character

Function 2 receives characters. After calling this function the AL register contains the character received. AH contains the value 0 if no error occurred, otherwise the value corresponds to the line status.

#### Function 3: Line/modem status

Function 3 senses and returns the modem status and line status. It returns the line status in the AH register and the modem status in the AL register:

Bit 0	Modem ready to send status change
Bit 1	Modem on status change
Bit 2	Telephone ringing status change
Bit 3	Connection to receiver status change
Bit 4	Modem ready to send
Bit 5	Modem on
Bit 6	Telephone ringing
Bit 7	Connection to receiver modem

Bits 4 to 7 represent a duplication of bits 0 to 3. Bits 0 to 3 indicate whether the contents of bits 4 to 7 have changed since the last reading of the modem status. If this is the case, the corresponding bit contains the value 1. For example, if bit 2 contains the value 1, this means that the content of bit 6 has changed since the last reading. In reality it means that the phone just started to ring or has stopped ringing, depending on the previous value of bit 6.