PROJECT REPORT

ON

DESIGN AND FABRICATION OF HIGH BANDWIDTH POTENTIOSTAT AND GALVANOSTAT FOR ELECTROCHEMICAL STUDIES

(SEPT.15, 1998 TO DEC. 20, 1998)

By

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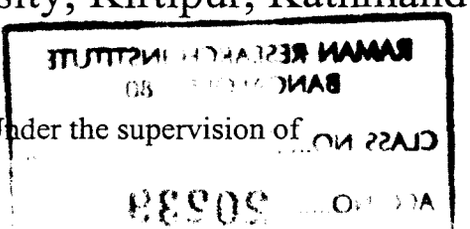

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Acknowledgements

I would like to express my sincere thanks to the Director, Raman Research Institute for kindly permitting me to work in the Institute and for providing the necessary facilities to carry out this project. I am grateful to Prof. G. S. Ranganath, Dean of Research, who invited me to visit the institute. I am also grateful to Prof. Shekhar Gurung, Head of Department, Central Department of Physics, Tribhuvan University, Kathmandu, Nepal for kindly giving me permission to visit RRI.

No words will be sufficient to express my gratitude to Prof. V. Lakshminarayanan, Raman Research Institute, who encouraged me all the way. His experienced and invaluable guidance always led me towards right way to deal with the problems. I would like to thank R. Subramanian, Ph.D. scholar at Raman Research Institute, who taught me the ABC... of electrochemical system and helped me through out the project.

Thanks are due to Mr. N. Ravi Shankar of Electrochemistry Laboratory RRI, Mr. Mani and Mr. Gokul of RRI workshop who helped me in fabricating the instrument. Thanks are also due to all the members of electronics laboratory for their help in every respect. I also thank to Mr. Radhakrisnan, LC Department RRI for his kind help during the project.

I am very much impressed by the hospitality of RRI and I thank all the staff members of administration and canteen. The help of Surajit, Udaya, Ujjal, Vishwanath, Subashree, Amarnath, Giridhar, Amitabh and all other friends at RRI will always remain in my mind as a symbol of good friendship.

Jagat Shakya

Contents

1. Introduction

Potentiostat and Galvanostat are among the most useful device used in Electrochemistry specially in Electrochemical Impedance Spectroscopy (EIS). Electrochemical experiments such as potentiometry, amperometry, diferential capacitance mesurement, impedance measurement, voltametry, coulometry etc. are done using Potentiostat / Galvanostat. One of the most useful application of potentiostat in material science is corrosion measurement. All these and other electrochemical methods requires controlling and measuring the electrical parameters of an electrode reaction, which is achieved by these devices.

Electrochemical experiments are done either by potential control method or by current control method. Potentiostat is used in potential controlled method to maintain the constant potential, between reference electrode RE and working electrode WE in three electrode electrochemical system, irrespective of changes in the impedance of the cell due to chemical reactions taking place in the cell. Similarly galvanostat is used in current controlled method which maintains constant current in the system irrespective of the changes in impedance of cell. Even though there are already so many researches had been done and a large number of literatures had been published in different era of time since the invention of vaccum tube electronics and many companies are producing fully computer controlled potentiostat, an attempt has been made to design and fabricate "relatively" high frequency high power potentostat / galvanostat, mainly due to two reasons. Firstly, commercially available potentiostats / galvanostats have complicated circutary, since they are made for general purpose, and poor high frequency response, though they are precious at low frequency. Secondly, such shortcomings are eliminated in some commercially available potentiostat but these are more expensive.

The high frequency control system is required in many electrochemical experiment, for example if the double layer capacitance (Cdl) typically is low and so as the uncompensated resistance (Ru) and electrode electrolyte interface resistance (Rt), in Randles Cell, then one must go to high frequency. Such type of experiments has also been performed for testing the performance of device built. Similarly mass transfer reaction like experiments require high current which is to be controlled with in certain limit of precision. The electrical parameter of the electrode can be controlled through a wide range of frequency band (0 to 1 MHz) and with a large current (about 1 ampere) using this "home made" potentiostat.

The whole instrument is based upon semiconductor electronics and the circuits have been kept as simple as possible. Since it is required to have some idea of cells and their electrical equivalent model, briefly they are introduced here. Operational amplifier is the main building block of the instrument, it's better to have ideas of operational amplifiers and their internal structure and mode of operations. But it is not possible here to discuss all the internal structure of the op-amp so it is considered as "black box amplifier" and its mode of operation are discussed here. The choice of operational amplifier has been done according to the specification provided by manufacturer. We are briefly discussing about AD844, CA3140 high frequency op-amps and PB58A high frequency high power op-amp.

1.1 Electrochemical cell and its electrical equivalent circuits

In electrochemistry some conducting materials called electrode are used either to study their properties or to measure potential or to supply current. The electrodes are immersed in an electrolyte (an electrically conductive solution). The collection of the electrodes, the solution and the container holding the solution are referred to as an electrochemical cell. The chemical reactions inside cell produces some potential difference between electrodes and electrolyte so current may flow in the cell. Generally two electrodes are required to complete the circuit. But in potential controlled system the potential of one electrode must be controlled with respect to some reference, so that three-electrode system is used in such cases. A potentiostat requires an electrochemical cell with three electrodes.

The three electrodes are called Working Electrode (WE), Reference Electrode (RE) and Counter (or Auxiliary) Electrode (CE).

Working Electrode

Working electrode is the sample understudy in an electrochemical system. The working electrode can be bare metal or coated. More generally, the electrochemical reactions being studied occur at the working electrode.

Reference Electrode

The reference electrode is used in measuring the working electrode potential. A reference electrode should have a constant electrochemical potential as long as no current flows through it. The most common lab references are the Saturated Calomel Electrode (SCE) and the Silver/Silver Chloride (Ag /AgCl) electrodes. In field probes, a pseudo-reference (a piece of the working electrode material) is often used.

Counter or Auxiliary Electrode

The counter electrode is a conductor that completes the cell circuit.
The auxiliary (counter) electrode in lab cells is generally an inert conductor like platinum or graphite. In field probes it's generally another piece of the working electrode material. The current that flows into the solution via the working electrode leaves the solution via the auxiliary electrode.

A potentiostat is an electronic device that controls the voltage difference between a working electrode and a reference electrode. Both electrodes are contained in a electrochemical cell. The potentiostat implements this control by injecting current into the cell through an auxiliary electrode. In almost all applications, the potentiostat measures the current flow between the working and auxiliary electrodes. The controlled variable in a potentiostat is the cell potential and the measured variable is the cell current.

AC Circuit Theory and Representation of Complex Impedance Values

Impedance definition: concept of complex impedance

Electrical resistance is the ability of a circuit element to resist the flow of electrical current. Ohm's law (Equation 1-1) defines resistance in terms of the ratio between voltage E and current I.

$R = E/I$ 1.1

While this is a well-known relationship, its use is limited to only one circuit element - the ideal resistor. An ideal resistor has several simplifying properties:

· It follows Ohm's Law at all current and voltage levels.
· Its resistance value is independent of frequency.
· AC current and voltage signals though a resistor is in phase with each other.

The real world contains circuit elements that exhibit much more complex behaviour. These elements force us to abandon the simple concept of resistance. In its place we use impedance, which is a more general circuit parameter. Like resistance, impedance is a measure of the ability of a circuit to resist the flow of electrical current. Unlike resistance, impedance is not limited by the simplifying properties listed above.

Electrochemical impedance is usually measured by applying an AC potential to an electrochemical cell and measuring the current through the cell. Suppose that we apply a sinusoidal potential excitation. The response to this potential is an AC current signal, containing the excitation frequency and it's harmonics. This current signal can be analysed as a sum of sinusoidal functions (a Fourier series).

Electrochemical Impedance is normally measured using a small excitation signal. This is done so that the cell's response is pseudo-linear. In a linear (or pseudo-linear) system, the current response to a sinusoidal potential will be a sinusoid at the same frequency but shifted in phase. See Figure 1-1

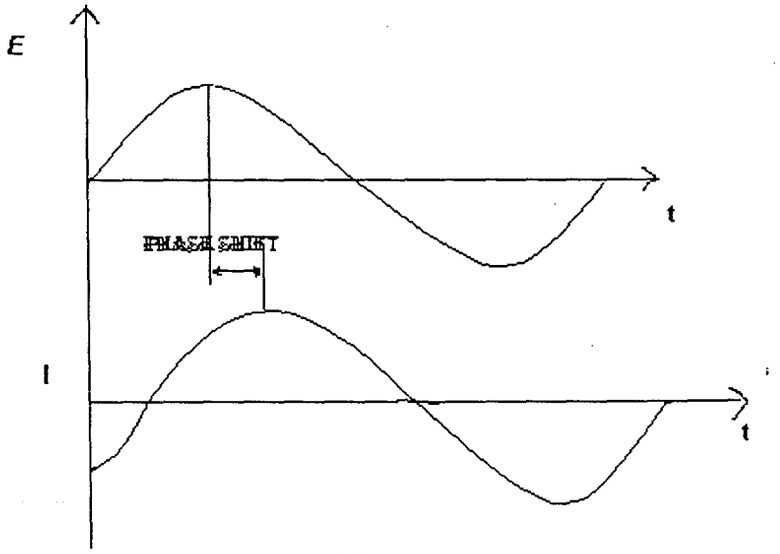


Figure 1-1
Sinusoidal Current Response in a Linear System

Introduction

The excitation signal, expressed as a function of time, has the form

$E(t) = E_o \cos(\omega t)$ 1.2

E(t) is the potential at time tr Eo is the amplitude of the signal, and w is the radial frequency. The relationship between radial frequency w (expressed in radians/second) and frequency f (expressed in hertz) is:

$\omega = 2\pi f$ 1.3

In a linear system, the response signal, I_t, is shifted in phase ϕ and has a different amplitude, I_0:

$I(t) = I_o \cos(\omega t - \phi)$ 1.4

An expression analogous to Ohm's Law allows us to calculate the impedance of the system as:

$$Z = \frac{E(t)}{I(t)} = \frac{E_o \cos(\omega t)}{I_0 \cos(\omega t - \phi)} = Z_o \frac{\cos(\omega t)}{\cos(\omega t - \phi)} \quad \text{.....1-5}$$

The impedance is therefore expressed in terms of a magnitude, Z_0, and a phase shift, ϕ.

If we plot the applied sinusoidal signal on the X-axis of a graph and the sinusoidal response signal I(t) on the Y-axis, an oval called a "Lissajous figure" is plotted. Analysis of Lissajous figures on oscilloscope screen was the accepted method of impedance measurement prior to the availability of lock-in amplifiers and frequency response analyzers.

Using Eulers relationship,

$\exp(j\phi) = \cos\phi + j \sin\phi$ The impedance is then represented as a complex number,

$Z = Zo \exp(j\phi) = Zo(\cos\phi + j \sin\phi)$.....1.6

In Equation (1-6) the expression for Z(w) is composed of a real and an imaginary part. If the real part is plotted on the Z axis and the imaginary part on the Y axis of a chart, we get a "Nyquist plot". See Figure 1-2. Notice that in this plot the y-axis is negative and that each point on the Nyquist plot is the impedance at one frequency.

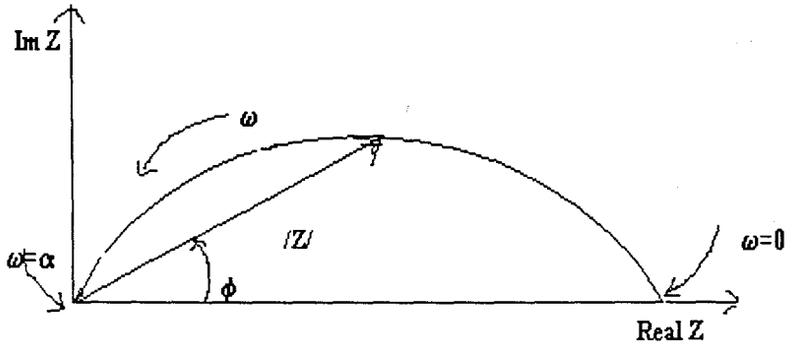


Figure 1-2 Nyquist Plot with Impedance Vector

Figure 1-2 has been annotated to show that low frequency data are on the right side of the plot and higher frequencies are on the left. This is true for EIS data where impedance usually falls as frequency rises (this is not true of all circuits). On the Nyquist plot the impedance can be represented as a vector of length |Z|. The angle between this vector and the x-axis is ϕ, where ϕ = arg(Z). Nyquist plots have one major shortcoming. When we look at any data point on the plot, we cannot tell what frequency was used to record that point. The Nyquist plot in Figure 1-2 results from the electrical circuit of Figure 1-3 The semicircle is characteristic of a single "time constant". Electrochemical Impedance plots often contain several time constants. Often only a portion of one or more of their semicircles is seen.

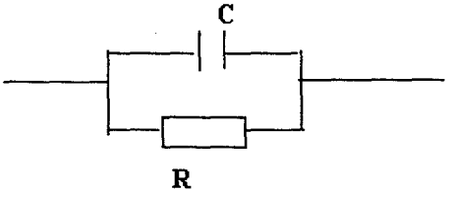


Figure 1-3 Simple Equivalent Circuit with One Time Constant

Another popular presentation method is the "Bode plot". The impedance is plotted with log frequency on the x-axis and both the absolute value of the impedance (|Z| =Z0) and phase-shift on the y-axis. The Bode plot for the electric circuit of Figure 1-3 is shown in Figure 1-4. Unlike the Nyquist plot, the Bode plot explicitly shows frequency information.

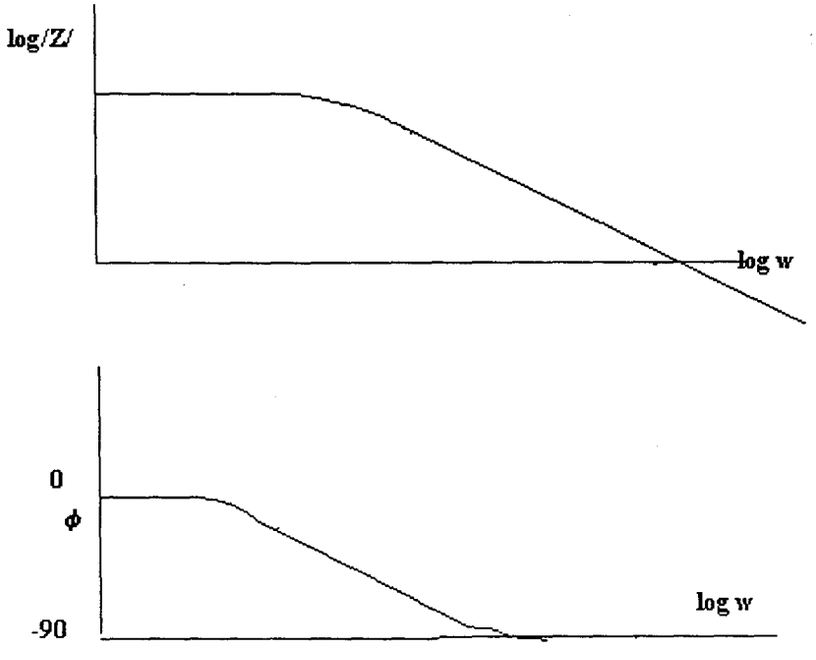


Figure 1-4 Bode Plot with One Time Constant

1.2 Electrochemistry - A Linear System?

Electrical circuit theory distinguishes between linear and non-linear systems (circuits). Impedance analysis of linear circuits is much easier than analysis of non-linear ones. The following definition of a linear system is taken from Signals and Systems by Oppenheim and Willsky:

A linear system ... is one that possesses the important property of superposition: If the input consists of the weighted sum of several signals, then the output is simply the superposition, that is, the weighted sum, of the responses of the system to each of the signals. Mathematically, let $y_1(t)$ be the response of a continuous time system to $x_1(t)$ and let $y_2(t)$ be the output corresponding to the input $x_2(t)$. Then the system is linear if:

1) The response to $x_1(t) + x_2(t)$ is $y_1(t) + y_2(t)$

2) The response to $ax_1(t)$ is $ay_1(t)$ ...

For a potentiostated electrochemical cell, the input is the potential and the output is the current. Electrochemical cells are not linear! Doubling the voltage will not necessarily double the current. However, electrochemical systems can be pseudo-linear. When we look at a small enough portion of a cell's current versus voltage curve, it seems to be linear. In normal EIS practice, a small (1 to 10 mV) AC signal is applied to the cell. The signal is small enough to confine ourselves to a pseudo-linear segment of the cell's current versus voltage curve. The cell's non-linear response to the DC potential is not measured because in EIS only the cell current at the excitation frequency is measured. If the system is non-linear, the current response will contain harmonics of the excitation frequency.

Some researchers have made use of this phenomenon. Linear systems should not generate harmonics, so the presence or absence of significant harmonic response allows one to determine the system's linearity. Other researchers have intentionally used larger amplitude excitation potentials. They use the harmonic response to estimate the curvature in the cell's current voltage curve.

Steady State Systems

Measuring an EIS spectrum takes time (often many hours). The system being measured must be at a steady state throughout the time required to measure the EIS spectrum. A common cause of problems in EIS measurements and their analysis is drift in the system being measured. In practice a steady state can be difficult to achieve. The cell can change through adsorption of solution impurities, growth of an oxide layer, build up of reaction products in solution, coating degradation, temperature changes, to list just a few factors. Standard EIS analysis tools may give wildly inaccurate results on a system that is not at a steady state.

Electrical Circuit Elements

EIS data is commonly analysed by fitting it to an equivalent electrical circuit model. Most of the circuit elements in the model are common electrical elements such as

resistors, capacitors, and inductors. To be useful, the elements in the model should have a basis in the physical electrochemistry of the system. As an example, most models contain a resistor that models the cell's solution resistance.

Some knowledge of the impedance of the standard circuit components is therefore quite useful. The common circuit elements are given , the equation for their current versus voltage relationship, and their impedance

Common Electrical Elements

Component	Current Vs Voltage	Impedance
resistor	E= IR	Z = R
inductor	E = L di/dt	Z = jωL
capacitor	I = C dE/dt	Z = 1/jωC

Notice that the impedance of a resistor is independent of frequency and has only a real component. Because there is no imaginary impedance, the current through a resistor is always in phase with the voltage.

The impedance of an inductor increases as frequency increases. Inductors have only an imaginary impedance component. As a result, an inductor's current is phase shifted 90 degrees with respect to the voltage.

The impedance versus frequency behaviour of a capacitor is opposite to that of an inductor. A capacitor's impedance decreases as the frequency is raised. Capacitor also has only an imaginary impedance component. The current through a capacitor is phase shifted -90 degrees with respect to the voltage.

Serial and Parallel Combinations of Circuit Elements

Very few electrochemical cells can be modelled using a single equivalent circuit element. Instead, EIS models usually consist of a number of elements in a network. Both serial and parallel combinations of elements occur. Fortunately, there are simple formulas that describe the impedance of circuit elements in both parallel and series combinations.

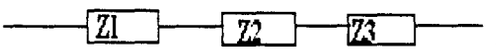


Figure 1-5 Impedances in Series

For linear impedance elements in series the equivalent impedance can be calculated as

$Zeq = Z_1 + Z_2 + Z_3$ .....(1-7)

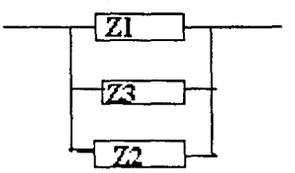


Figure 1-6 Impedances in Parallel

For linear impedance elements in parallel the equivalent impedance can be calculated as

$$\frac{1}{Z_{eq}} = \frac{1}{Z_1} + \frac{1}{Z_2} + \frac{1}{Z_3} \quad \text{..... (1-8)}$$

Physical Electrochemistry and Equivalent Circuit Elements

Electrolyte Resistance

Solution resistance is often a significant factor in the impedance of an electrochemical cell. A modern 3-electrode potentiostat compensates for the solution resistance between the counter and reference electrodes. However, any solution resistance between the reference electrode and the working electrode must be considered when the cell is modelled .

The resistance of an ionic solution depends on the ionic concentration, type of ions,

temperature and the geometry of the area in which current is carried. In a bounded area with area A and length 1 carrying a uniform current the resistance is defined as:

$$R = \rho \frac{l}{A} \text{ .....(1-9)}$$

where r is the solution resistivity. The conductivity of the solution, k , is more commonly used in solution resistance calculations. Its relationship with solution resistance is:

$$R = \frac{l}{kA} \Rightarrow k = \frac{l}{RA} \text{.....(1-10)}$$

Standard chemical handbooks list k values for specific solutions. For other solutions, one can calculate k from specific ion conductances. The units for k are Siemens per meter (S/m). The Siemen is the reciprocal of the ohm, so 1 S = 1/ohm.

Unfortunately, most electrochemical cells do not have uniform current distribution through a definite electrolyte area. The major problem in calculating solution resistance therefore concerns determination of the current flow path and the geometry of the electrolyte that carries the current. Fortunately, we don't usually calculate solution resistance from ionic conductances. Instead, it is found when we fit a model to experimental EIS data.

Double Layer Capacitance

A electrical double layer exists at the interface between an electrode and its surrounding electrolyte. This double layer is formed as ions from the solution "stick on" the electrode surface. Charges in the electrode are separated from the charges of these ions. The separation is very small, on the order of angstroms. Charges separated by an insulator form a capacitor. On a bare metal immersed in an electrolyte, you can estimate that there will be approximately 30 μF of capacitance for every cm^2 of electrode area. The value of the double layer capacitance depends on many variables including electrode potential, temperature, ionic concentrations, types of ions, oxide layers, electrode roughness, impurity adsorption, etc.

Besides these there are Polarisation resistance, charge transfer resistance diffusion impedance (Warburg impedance) , coating capacitance etc

Simple Equivalent Circuit Model

Model #1 - A Purely Capacitive Coating

A metal covered with an undamaged coating generally has a very high impedance. The equivalent circuit for such a situation is in Figure 1-7.

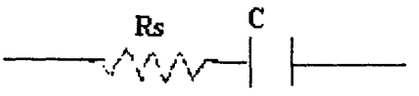
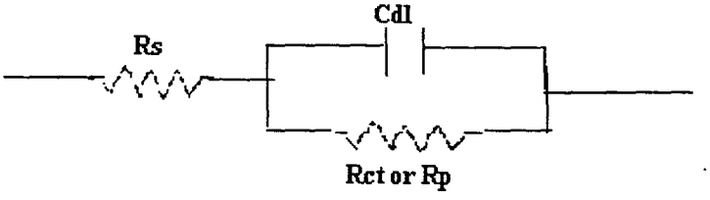


Figure 1-7
Purely Capacitive Coating

The model includes a resistor (due primarily to the electrolyte) and the coating capacitance in series.

Model #2 -- Randles Cell

The Randles cell is one of the simplest and most common cell models. It includes a solution resistance, a double layer capacitor and a charge transfer or polarisation resistance. In addition to being a useful model in its own right, the Randles cell model is often the starting point for other more complex models. The equivalent circuit for the



Randles cell is shown in Figure 1-8. The double layer capacitor is in parallel with the impedance due to the charge transfer reaction.

Figure 1-8
Randles Cell Schematic Diagram

There are other complex and more generalised models for cells, but being simple and useful we consider here this cell model throughout our study

2 Operational amplifiers

2.1 Introduction

The term operational amplifier, abbreviated op amp, was coined in the 1940s to refer to a special kind of amplifier that, by proper selection of external components, can be configured to perform a variety of mathematical operations. Early op amps were made from vacuum tubes consuming lots of space and energy. Later op-amps were made smaller by implementing them with discrete transistors. Today, op amps are monolithic integrated circuits, highly efficient and cost effective.

Almost all of our present work is based upon the op-amp so the basic idea behind such integrated circuit op-amp (IC op-amp) is discussed along with few elementary circuits, which are used in our instrument . It is not to be mentioned that at present semiconductor devices play indispensable roll in modern tecnology. Op-amp is one of such small linear device, which forms heart of many sophisticated electronic devices. One op-amp IC chip may contain thousands of transistors diodes capacitors and resistors altogether. The internal structure of Op-amp varies according to their special purpose of use, and different part numbers given by manufacturers identifies them. So it is not possible here to discuss about internal structure of all op-amp ,but they shear some common mechanism, like all of them have at least one transistorised differential amplifier (this circuit contains two transistors having two input and two outputs, the output voltage of this circuit is the difference between its two inputs) and many transistor amplifiers inside it ,to meet the properties of ideal op-amp.

Amplifier Basics

Before jumping into op amps, lets take a minute to review some amplifier fundamentals. An amplifier has an input port and an output port. In a linear amplifier, output signal = A x input signal, where A is the amplification factor or gain. Depending on the nature of input and output signals, we can have four types of amplifier gain:

Voltage (voltage out/voltage in)
Current (current out/current in)
Transresistance (voltage out/current in)
Transconductance (current out/voltage in)

Since most op amps are voltage amplifiers, we will limit our discussion to voltage amplifiers.

Thevenin's and Norton's Theorems

The input source to an amplifier may be represented either by a series circuit as in fig 1.2 or by a parallel network. This result is a special case of Thevenin and Norton's theorems. Thevenin's theorem states that "any two terminal linear network may be replaced by a voltage source equal to the open circuit voltage between the terminals in series with output impedance seen at this port".

In fig 2.1, V represents the open circuit voltage and Z is the impedance between two terminals. To find Z all independent voltage sources are short-circuited and all independent current sources are open-circuited and the impedance is "seen from outside in".

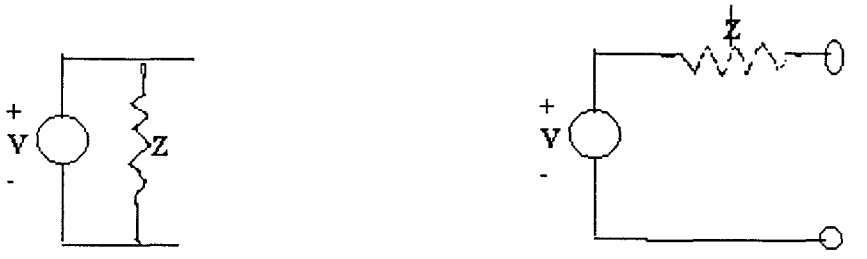


Fig 2.1

Norton's Theorem

The dual of Thevenin's theorem is Norton's theorem which states that "any two terminal linear network may be replaced by a current source equal to the short circuited current between the terminals in parallel with the output impedance seen at this port"

Thevenin's theorem can be used to derive a model of an amplifier, reducing it to the appropriate voltage sources and series resistances. The input port plays a passive role, producing no voltage of its own, and its Thevenin equivalent is a resistive element, Ri. The output port can be modelled by a dependent voltage source, AVi, with output resistance, R_O. To complete a simple amplifier circuit, we will include an input source and impedance, VS and RS, and output load, RL. Figure 1 shows the Thevenin equivalent of a simple amplifier circuit.

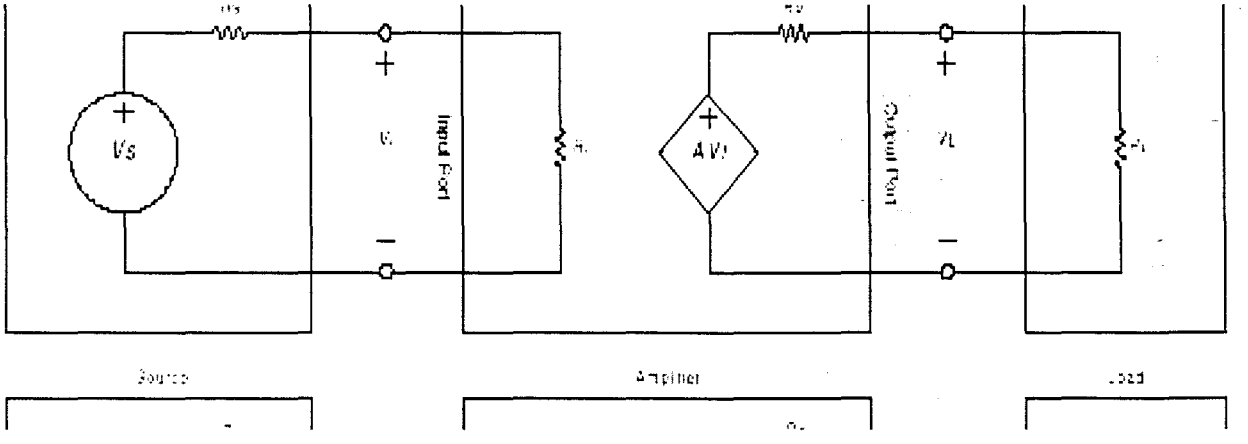


Figure 2.2 Thevenin Model of Amplifier with Source and Load

It can be seen that we have voltage divider circuits at both the input port and the output port of the amplifier. This requires us to re-calculate whenever a different source and/or load is used and complicates circuit calculations.

2.2 Ideal Op Amp Model

The Thevenin amplifier model shown in Figure 2.2 is redrawn in Figure 2.3 showing standard op amp notation. An op amp is a differential to single-ended amplifier. It amplifies the voltage difference, Vd = Vp - Vn, on the input port and produces a voltage, VO, on the output port that is referenced to ground.

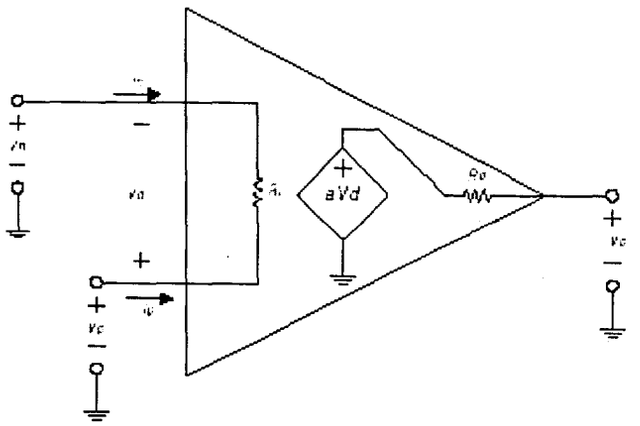


Figure 2.3 Standard Op Amp Notation

We still have the loading effects at the input and output ports as noted above. The ideal op amp model was derived to simplify circuit calculations and is commonly used by engineers in first-order approximation calculations. The ideal model makes three simplifying assumptions:

Gain is infinite a = α (1)
Input resistance is infinite Ri = α (2)
Output resistance is zero RO = 0 (3)

Applying these assumptions to Figure 2 results in the ideal op-amp model shown in Figure2.4.

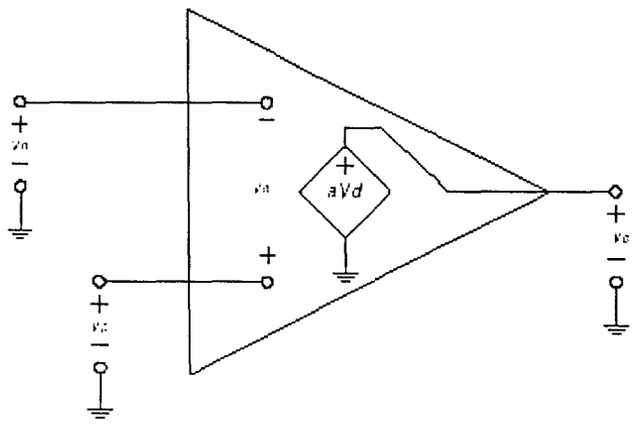


Figure 2.4 Ideal Op Amp Model

Other simplifications can be derived using the ideal op amp model:

$\Rightarrow \mathbf{I_n = I_p = 0}$ (4)

Because $R_i = \alpha$, we assume $I_n = I_p = 0$. There is no loading effect at the input.

$\mathbf{Vo = a\ Vd}$ (5)

Because $R_O = 0$ there is no loading effect at the output.

$\Rightarrow \mathbf{Vd = 0}$ (6)

If the op amp is in linear operation, VO must be a finite voltage. By definition $V_O = Vd \times a$. Rearranging, $Vd = V_O / a$. Since $a = \alpha$, $Vd = Vo / \alpha = 0$. This is the basis of the virtual short concept.

$\Rightarrow$ **Common mode gain = 0** (7)

The ideal voltage source driving the output port depends only on the voltage difference across its input port. It rejects any voltage common to Vn and Vp.

$\Rightarrow$ **Bandwidth** = α (8)
$\Rightarrow$ **Slew Rate** = α (9)
No frequency dependencies are assumed.

$\Rightarrow$ **Drift = 0** (10)

There are no changes in performance over time, temperature, humidity, power supply variations, etc.

Non-Inverting Amplifier

An ideal op amp by itself is not a very useful device since any finite input signal would result in infinite output. By connecting external components around the ideal op amp, we can construct useful amplifier circuits. Figure 2.5 shows a basic op amp circuit, the non-inverting amplifier. The triangular gain block symbol is used to represent an ideal op amp. The input terminal marked with a + (Vp) is called the non-inverting input; – (Vn) marks the inverting input.

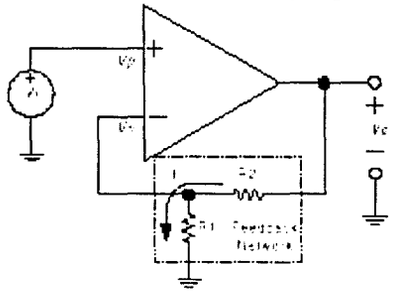


Figure 2.5 Non-Inverting Amplifier

To understand this circuit we must derive a relationship between the input voltage, Vi, and the output voltage, V_O. Remembering that there is no loading at the input,

Vp = Vi (2-1)

The voltage at Vn is derived from VO via the resistor network, R1 and R2, so that,

$$V_n = V_o \frac{R_1}{R_1 + R_2} = V_0 b \qquad (2\text{-}2)$$

where, $$b = \frac{R_1}{R_1 + R_2} \qquad (2\text{-}3)$$

The parameter b is called the feedback factor because it represents the portion of the output that is fed back to the input. Recalling the ideal model,

$V_O = aVd = a\,(Vp - Vn)$ (2-4)

Substituting,

$V_O = a(\,Vi - b\,V_O)$ (2-5)

and collecting terms yield,

$$A = \frac{V_0}{V_i} = \left(\frac{1}{b}\right)\left(\frac{1}{1 + 1/ab}\right) \qquad (2\text{-}6)$$

This result shows that the op amp circuit of Figure 2-5 is itself an amplifier with gain A. Since the polarity of Vi and V_O are the same, it is referred to as a non-inverting amplifier. A is called the close loop gain of the op amp circuit, whereas 'a' is the open loop gain. The product 'ab' is called the loop gain. This is the gain a signal would see starting at the inverting input and travelling in a clockwise loop through the op amp and the feedback network.

Closed Loop Concepts and Simplifications

Substituting $a = \alpha$ (1) into (2-6) results in,

$$A = \frac{1}{b} = 1 + \frac{R_2}{R_1} \qquad (2\text{-}7)$$

Recalling that in equation (6) we state that Vd, the voltage difference between Vn and Vp, is equal to zero and therefore, Vn = Vp. Still they are not shorted together. Rather there is said to be a virtual short between Vn and Vp. The concept of the virtual short further

simplifies analysis of the non-inverting op amp circuit in Figure 4. Using the virtual short concept, we can say that,

Vn = Vp = Vi (2-8)

Realising that finding Vn is now the same resistor divider problem solved in (2-2) and substituting (2-8) into it, we get,

$$V_i = V_o \frac{R_1}{R_1 + R_2} = V_0 b \qquad (2\text{-}9)$$

Rearranging and solving for A, we get,

$$A = \left(\frac{1}{b}\right) = 1 + \frac{R_1}{R_2} \qquad (2\text{-}10)$$

The same result is derived in equation (2-7). Using the virtual short concept reduced solving the non-inverting amplifier, shown in Figure 2.5, to solving a resistor divider network.

Inverting Amplifier

Figure 2.6 shows another useful basic op amp circuit, the inverting amplifier. The triangular gain block symbol is again used to represent an ideal op amp. The input terminal, + (Vp), is called the non-inverting input, whereas – (Vn) marks the inverting input. It is similar to the non-inverting circuit shown in Figure 4 except that now the signal is applied to the inverting terminal via R_1 and the non-inverting terminal is grounded.

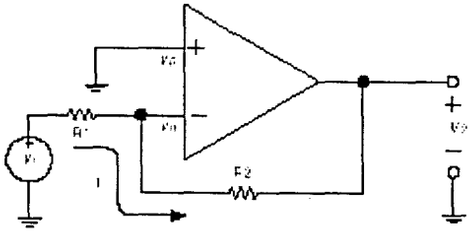


Figure 2.6 Inverting Amplifier

To understand this circuit, we must derive a relationship between the input voltage, Vi and the output voltage, V_O. Since Vp is tied to ground,

$$Vp = 0 \qquad (2\text{-}11)$$

Remembering that there is no current into the input, the voltage at Vn can be found using superposition. First let $V_O = 0$,

$$V_n = V_i\left(\frac{R_2}{R_1 + R_2}\right) \qquad (2\text{-}12)$$

Next let Vi = 0,

$$V_n = V_o\left(\frac{R_1}{R_1 + R_2}\right) \qquad (2\text{-}13)$$

Combining

$$V_n = V_0\left(\frac{R_1}{R_1 + R_2}\right) + V_i\left(\frac{R_2}{R_1 + R_2}\right) \qquad (2\text{-}14)$$

Remembering equation (14), $V_O = aVd = a(Vp - Vn)$, substituting and rearranging,

$$A = \frac{V_0}{V_i} = 1 - \left(\frac{1}{b}\right)\left(\frac{1}{1 + 1/ab}\right) \qquad (2\text{-}15)$$

where

$$b = \frac{R_1}{R_1 + R_2}$$

Again we have an amplifier circuit. Because b ≤1, the closed loop is an inverting amplifier.

Closed Loop Concepts and Simplifications

Substituting $a = \alpha$ (1) into (2-15) results in

$$A = 1 - \frac{1}{b} = -\frac{R_2}{R_1} \qquad (2\text{-}16)$$

Recall that in equation (2-6) we stated that Vd, the voltage difference between Vn and Vp, was equal to zero so that Vn = Vp. Still they are not shorted together. Rather there is said to be a virtual short between Vn and Vp. The concept of the virtual short further simplifies analysis of the inverting op amp circuit in Figure 2.6. Using the virtual short concept, we can say that

$$Vn = Vp = 0 \qquad (2\text{-}17)$$

In this configuration, the inverting input is a virtual ground. We can write the node equation at the inverting input as

$$\frac{V_n - V_i}{R_1} + \frac{V_n - V_0}{R_2} = 0 \qquad (2\text{-}18)$$

Since Vn = 0, rearranging, and solving for A we get

$$A = 1 - \frac{1}{b} = -\frac{R_2}{R_1} \qquad (2\text{-}19)$$

The same result is derived more easily than in (2-16). Using the virtual short (or virtual ground) concept reduced solving the inverting amplifier, shown in Figure 2.6, to solving a single node equation.

Simplified Op Amp Circuit Diagram

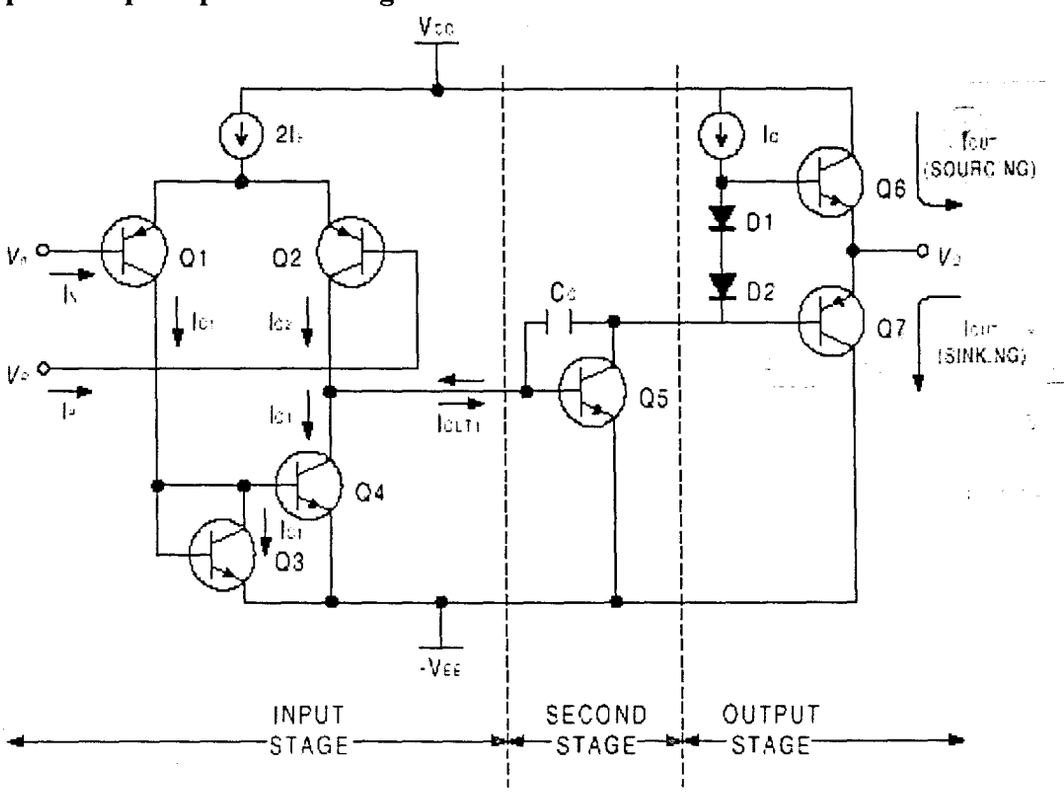


Figure 2.7. Simplified Op Amp Circuit Diagram

Op-amp

Real op amps are not ideal. They have limitations. To understand and discuss the origins of these limitations, see the simplified op amp circuit diagram shown in Figure 2.7.

Although simplified, this circuit contains the three basic elements normally found in op amps:

Input stage
Second stage
Output stage

The function of the input stage is to amplify the input difference, Vp - Vn, and convert it to a single-ended signal. The second stage further amplifies the signal and provides frequency compensation. The output stage provides output drive capability.

Input Stage

Symmetry of the input stage is key to its operation. Each transistor pair, Q1-Q2 and Q3-Q4, is matched as closely as possible. Q3 is diode connected. This forces the collector current in Q3 to equal I_{C1}. The base-emitter junctions of Q3 and Q4 are in parallel so they both see the same V_{BE} . Because Q4 is matched to Q3, its collector current is also equal to I_{C1}. This circuit is called a current mirror. Current source $2I_E$ is divided between Q1 and Q2. This division depends on the input voltages, Vp and Vn. When Vp is more positive than Vn, Q1 carries more current than Q2, and I_{C1} is larger than I_{C2}. The current mirror action of Q3-Q4 causes I_{out1} to flow into the collector-collector junction of Q2-Q4. When Vn is more positive than VP, Q2 carries more current than Q1 and I_{C2} is larger than I_{C1}. The current mirror action of Q3-Q4 causes I_{OUT1} to flow out of the collector-collector junction of Q2-Q4. I_{out1} is the single-ended signal out of the first stage and is proportional to the differential input, Vp - Vn.

$$I_{out1} = gm_1(Vp - Vn).$$

The term gm_1 is called the *transconductance* of the input stage. The input stage is a transconductance amplifier.

Second Stage

The second stage converts I_{out1} into a voltage and provides frequency compensation. If I_{out1} flows into the collector-collector junction of Q2-Q4, the second stage output voltage is driven positive. If I_{out1} flows out of the collector-collector junction of Q2-Q4, the second stage output voltage is driven negative. The second stage is a *transresistance* amplifier. The capacitor, C_C, in the second stage provides internal frequency compensation. It causes the gain to role off as the frequency increases. Without C_C , external compensation is required to prevent the op amp from oscillating in most applications.

Output Stage

The output stage is a typical class AB, push-pull amplifier. The emitter follower configuration of Q6 and Q7 provides current drive for the output load, with unity voltage gain. The output stage is a current amplifier.

2.3 Op Amp Specifications

Op amp circuits at moderate gain and frequency generally has very good agreement between actual performance and ideal performance. As gain and/or frequency is increased, however, certain op amp limitations come into play that effect circuit performance. In theory, with proper understanding of the internal structures and processes used to fabricate an op amp, we could calculate these effects. Thankfully this is not necessary, as manufacturers provide this information in data sheets. Proper interpretation of data sheet specifications is required when selecting an op amp for an application.

(A_V)Large-signal voltage amplification

The ratio of the peak-to-peak output voltage swing to the change in input voltage required driving the output.

(A_{VD}) Differential voltage amplification

The ratio of the change in the output to the change in differential input voltage producing it with the common-mode input voltage held constant.

Unity gain bandwidth

The range of frequencies within which the open-loop voltage amplification is greater that unity.

Input capacitance

The capacitance between the input terminals with either input grounded.

CMRR (Common-mode rejection ratio)

The ratio of differential voltage amplification to common-mode voltage amplification. (This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.)

Supply current

The current into the V_{CC}+ or V_{CC}- terminal of an integrated circuit.

IIB (Input bias current)

The average of the currents into the two input terminals with the output at the specified level.

IIO (Input offset current)

The difference between the currents into the two input terminals with the output at the specified level.

IOS (Short-circuit output current)

The maximum output current available from the amplifier with the output shorted to ground, to either supply, or to a specified point.

PD(Total power dissipation)

The total dc power supplied to the device less any power delivered from the device to a load.

Ri (Input resistance)

The resistance between the input terminals with either input grounded.

Rid (Differential input resistance)

The small-signal resistance between two ungrounded input terminals.

Ro Output resistance

The resistance between an output terminal and ground.

SR (Slew rate)

The average time rate of change of the closed-loop amplifier output voltage for a step-signal input.

tr (Rise time)

The time required for an output voltage step to change from 10% to 90% of its final value.

Total response time

The time between a step-function change of the input signal and the instant at which the magnitude of the output signal reaches, for the last time, a specified level range (±V) containing the final output signal level.

V_I (Input voltage range)

The range of voltage that if exceeded at either input may cause the operational amplifier to cease functioning properly.

V_{IO} Input offset voltage

The dc voltage that must be applied between the input terminals to force the quiescent dc output voltage to zero or other level, if specified.

VICR Common-mode input voltage range

The range of common-mode input voltage that if exceeded may cause the operational amplifier to cease functioning properly.

Differential input voltage

The voltage at the non-inverting input with respect to the inverting input.

Common-mode input impedance

The parallel sum of the small-signal impedance between each input terminal and ground.

Zo Output impedance

The small-signal impedance between the output terminal and ground.

THD + N (Total harmonic distortion plus noise)

The ratio of the RMS noise voltage and RMS harmonic voltage of the fundamental signal to the total RMS voltage at the output.

GBW Gain bandwidth product

The product of the open-loop voltage amplification and the frequency at which it is measured.

Slew Rate at Unity Gain

Slew rate, SR, is the rate of change in the output voltage caused by a step input. Its units are V/ms or V/ms. Figure 2.8 shows slew rate graphically. Referring back to Figure 2.7, voltage change in the second stage is limited by the charging and discharging of capacitor C_C. The maximum rate of change occurs when either side of the differential pair is conducting $2I_E$. This is the major limit to slew rate. Essentially, $SR = 2\ I_E / C_C$. However, there are op amps that work on different principles where this is not true. The requirement to have current flowing in or out of the input stage to change the voltage out of the second stage requires an error voltage at the input anytime the output voltage of an op amp is changing. An error voltage on the order of 120 mV is required for an op amp with a bipolar input to realise full slew rate. This can be as high as 1V to 3V for JFET or MOSFET input. Capacitor, C_C, is added to make the op amp unity gain stable.

Some op amps come in de-compensated versions where the value of C_C is reduced. This increases realisable bandwidth and slew rate, but the engineer must ensure the stability of the circuit by other means. To increase slew rate, the bias currents within the op amp are increased.

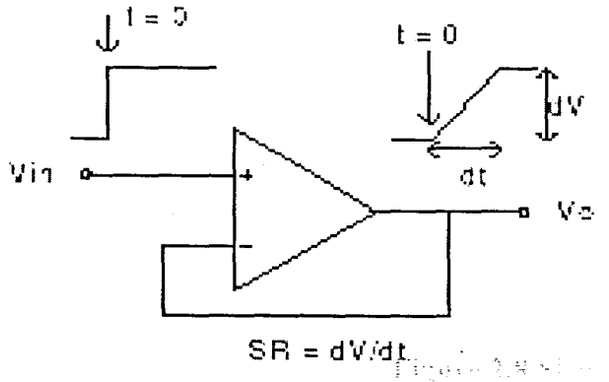


Figure 2.8 Slew Rate

Settling Time

It takes a finite time for a signal to propagate through the internal circuitry of an op amp. Therefore, it takes a certain period of time for the output to react to a step change in the input. Also the output normally overshoots the target value, experiences damped oscillation, and settles to a final value. Settling time, t_s, is the time required for the output voltage to settle to within a specified percentage of the final value given a step input. Figure 2.9 shows this graphically.

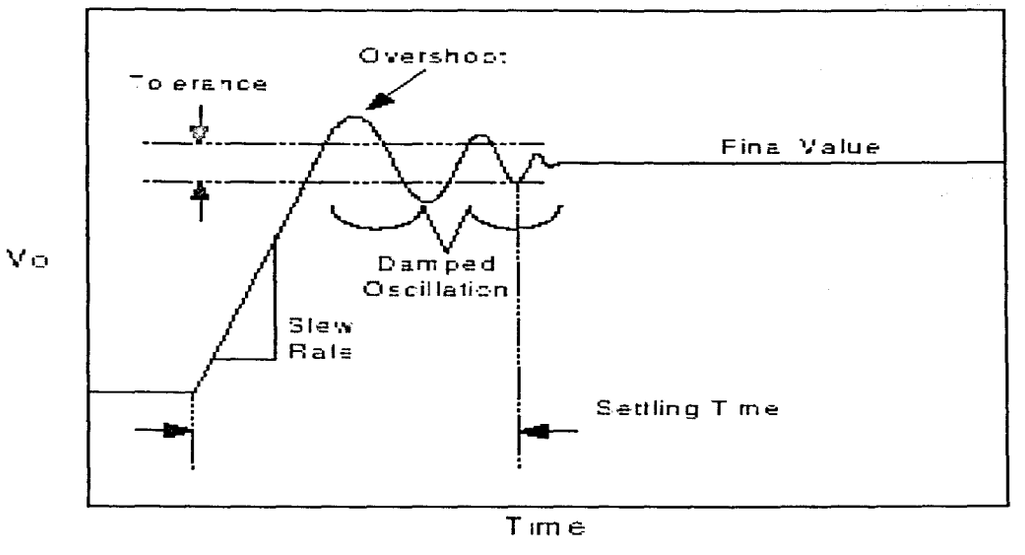


Figure2.9 SettlingTime

For high frequency application the settling time must be as possible as small.

2.4 Some circuits using op-amps

Voltage Follower

Fig 2.10 shows the op-amp version of emitter follower i.e. voltage follower. Referring to the fig 2.5, it is simply a noninverting amplifier with R_1 infinite and R_2 zero and gain equal to 1. This type of unity gain amplifier is frequently used to isolate the stages for high input impedance and low output impedance and called sometimes as *buffer*

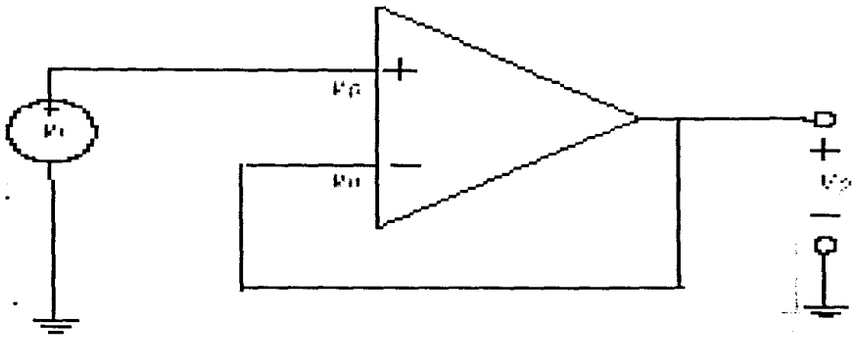
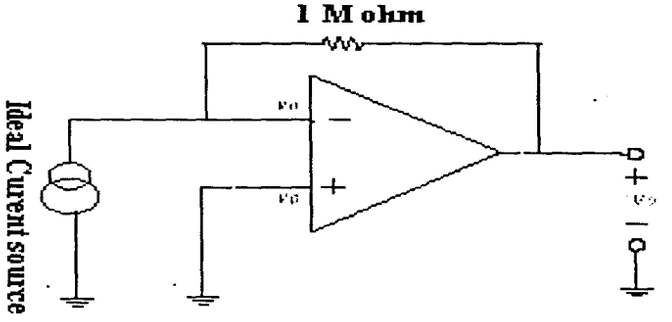


Fig 2.10

Here in our project **CA3140** has been used as voltage follower. Some times one can use a resistor typically 1 k ohm between output to inverting input.

Current to voltage converter

Considering the ideal current source (having zero impedance), the fig 2.11 is simple example of current to voltage converter. Few microampere current can be converted into 1-volt output voltage. Since the noninverting input is grounded, the inverting input is at virtual ground all the current that produces in ideal current source (considering very high input impedance of op-amp) flows through the external resistor. Hence out put voltage is proportional to input current, by the relation, $I_{in} = -V_0/R$



Current to voltage converter

Fig 2.11

Summing amplifier

Fig 2.12. shows a basic summing amplifier. Since noninverting input is grounded, the inverting input is at virtual ground. The current flowing through all the input sources flows through the feedback resistor R4 so

$V_1/ R_1 + V_2/ R_2 + V_3/ R_3 = - V_0/ R_4$

If $R_1 = R_2 = R_3 = R_4$ then $V_0 = -(V1 + V_2 + V_3)$

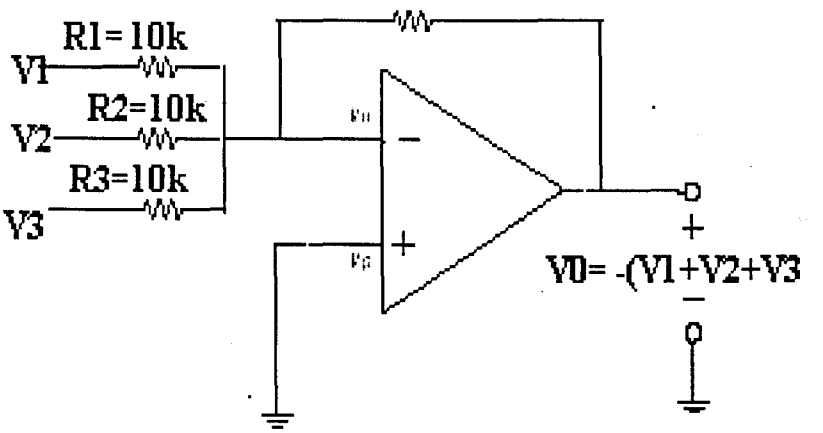


Fig 2.12

We have used this summing configuration in the input stage of control amplifier of potentiostat.

Instrumentational amplifier

A differential amplifier has 2 inputs and one or two outputs. Its output reads the difference between two inputs multiplied by some factor, which is determined by external circuitry. Fig 2.13 shows a classic differential amplifier, which has gain R2/R1.It is some times referred as substractor also.

The term instrumentational amplifier is used for a high gain dc-coupled differential amplifier with single ended output, high input impedance and high CMRR. The circuit given in fig. 2.13 also acts as instrumentational amplifier, but its input impedance is relatively low, so to raise the input impedance two buffer voltage followers are used in each input points. This type of configuration is shown in fig 2.14 and called instrumentational amplifier. The output $V_0 = R_2/R_1 (V_2 - V_1)$. If $R_2 = R_2$ then the output is just the difference between the two input signals. The disadvantage of this circuit is it requires high CMRR of both followers and also of the difference amplifier. It also requires precise resistor

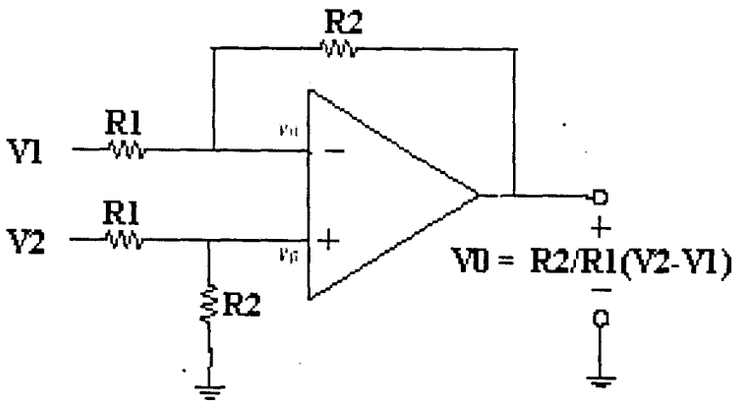


Fig 2.13

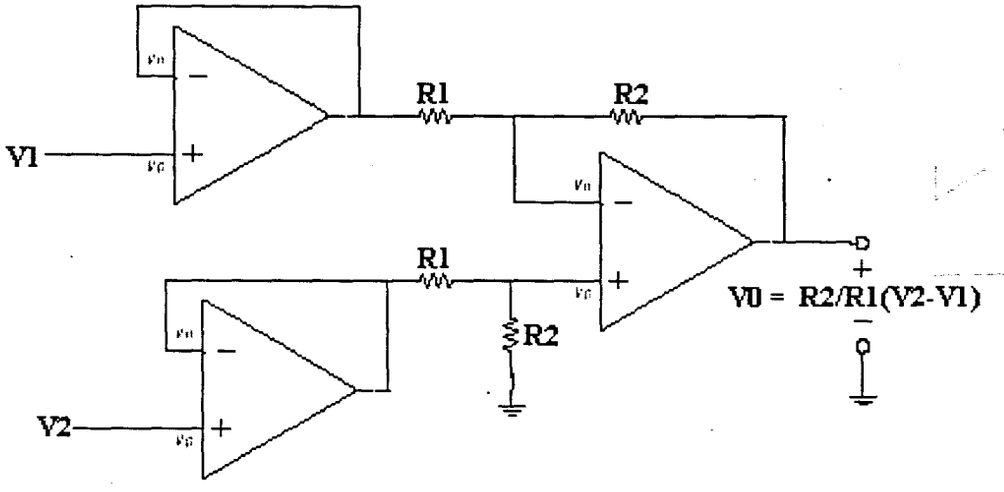


Fig 2.14

We have used this configuration to measure the current in potentiostat. CA3140 serves as two-voltage follower and AD 844 acts as differential amplifier in our configuration.

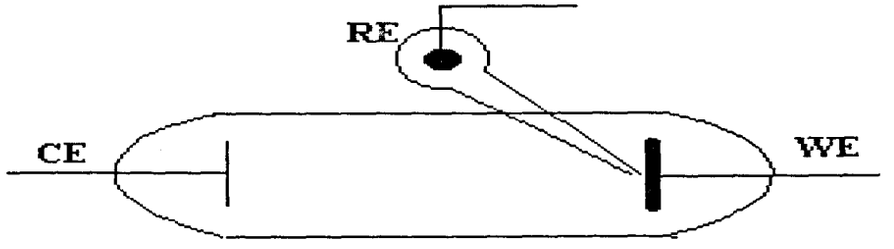
3 POTENTIOSTATS AND GALVANOSTATS

A potentiostat is a device, which controls the potential between *working electrode* (WE) and reference *electrode* (RE) at a fixed desired potential. The potential may be programmable varying with time. A minimum three-electrode electrochemical system is desirable for this electrode potential control system. The potential of working electrode, lying in its electrolyte environment, is controlled with respect to Reference electrode (RE)

The reference electrode is designed such that any current that passes through it must not disturb the interfacial potential between RE and solution, such electrode is termed as non-polarisable electrode. Even though modern potentiostats limits such current to very small amount (in the order of pico ampere), proper designation of it is desirable.

A third electrode called counter electrode (CE) is used to supply the current that flows through the cell. Since WE is located in resistive medium, when a current I. flows through the cell there will be potential gradient around the WE due to iRu drop, where Ru (called as uncompensated resistance) is the solution resistance between WE and RE.

For a physical size of electrode Ru will be pretty large, so a method is adopted to minimise Ru. RE is enclosed in nonconducting envelope having only small hole, which communicates between electrolyte inside and the electrolyte around WE. The vessels tip is kept closed to surface of WE; this configuration used to minimise Ru is called Luggin capillary. In practice Ru can never be zero. Fig 3.1 shows a conventional representation of RE in Luggin capillary.



Conventional representation of reference electrode contained in Luggin Capillary

Fig 3.1

There are several possible configurations for potentiostat: we discuss about some simplest configurations here. Fig 3.2 (a) shows a simple single op-amp potentiostat, in which the control input is given to the noninverting input of the op-amp. Output of op-amp is connected with CE. RE is connected to inverting input of op-amp, which makes a negative feedback path between output and inverting input. WE is grounded. Since

the noninverting input potential Vp = Vin and inverting input potential Vn = Vref. Then by the relation for op-amp inputs Vp = Vn, it can be clearly seen that Vin = Vref.

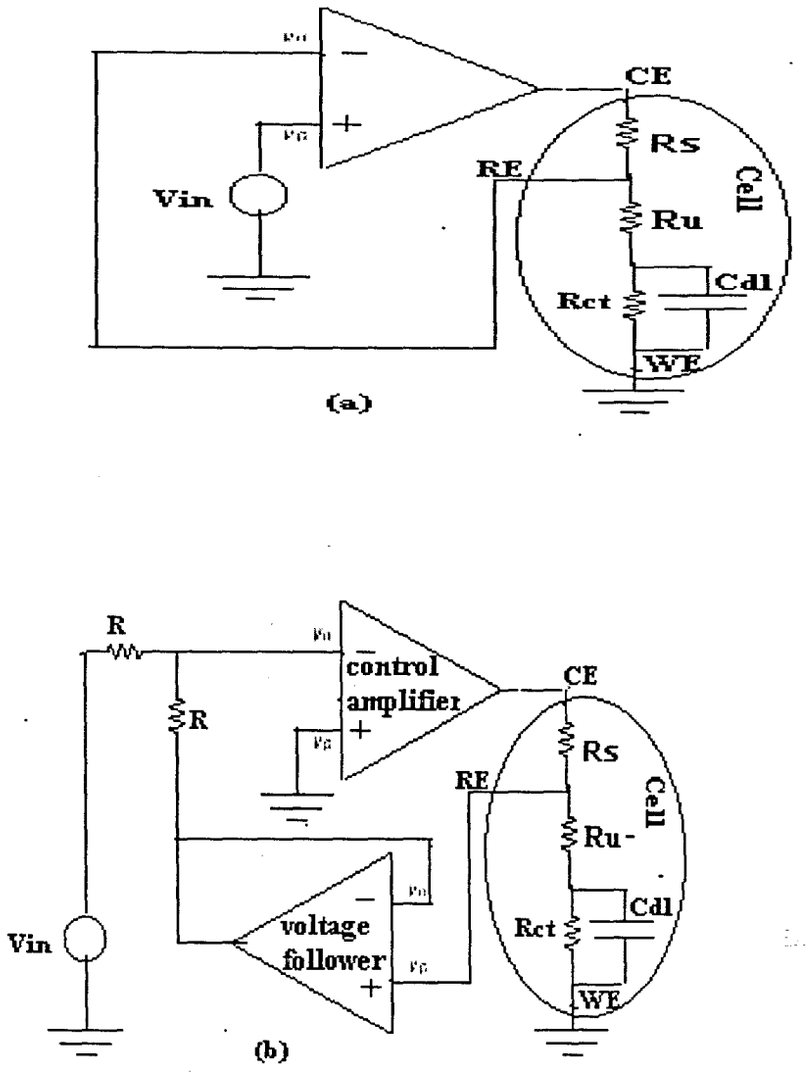


Fig 3.2

Fig (a) circuit is of practical use, if current required is very small, and if WE has only resistive impedance, then one can use this circuit to control the potential. The op-amp in this case should be some FET (MOSFET) device such as CA3140 which has very small input bias current. If bipolar op-amp like 741 , which has input bias current some tenth of nanoamperes , is used for this purpose, then there will be an error of the order of 0.1 V in the WE potential, for $10^5\Omega$ impedance of RE.

A modification of the circuit (a) is given in (b), in which the problem of bias current is eliminated upto certain level by using FET voltage follower. Here voltage

follower (in our case CA3140) acts as isolator or buffer. It is true that slight complication in frequency response arises due to the addition of voltage follower but it has to be paid for improvement of sensitivity. Another modification in this circuit is the summing configuration in the inverting input. One can apply more than one input simultaneously (Not shown in fig), through a resistor R at the same summing point of inverting input of *control amplifier.*

If E_{WR} is the potential difference between WE and RE then,

$E_{WR} = E_W - IR_U - E_{ref}$ (3-1)

Since WE is grounded, E_W is zero here. The output of voltage follower is just

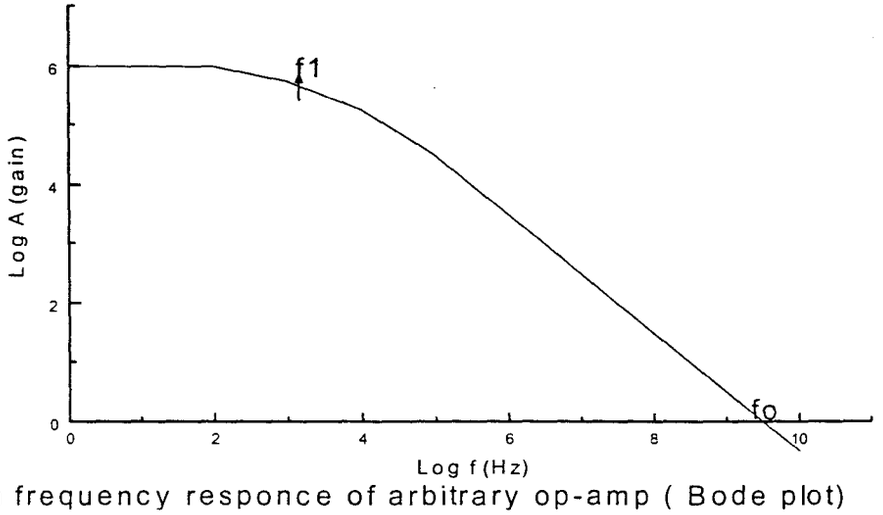
$E_{RW} = - E_{WR} = IR_U + E_{ref}$ (3-2)

In the summing node, which is at virtual ground, of op-amp, using krichoff's law (Sum of total current at a junction is zero)

$$\frac{E_{RW}}{R} + \frac{V_{in}}{R} = 0 \Rightarrow -E_{RW} = -\left(IR_U + E_{ref}\right) = V_{in} = E_{WR} \qquad (3\text{-}3)$$

In this manner the potential E_{WR} is controlled in this configuration.

Here we have considered the op-amp as ideal one, which has very high gain irrespective of frequency of stimulus. This is not true for all practical potentiostat as well as op-amps. Manufacturers' datasheet only gives the responses in ideal cases. The question of frequency response is quite tedious than that is considered. Since the feedback path in a potentiostat includes the cell itself, the dynamic behaviour of a potentiostat depends upon the type of cell under study at higher frequencies. The theories of dynamic responses are reviewed in detail (voraunhofer and Banks 1972, Harrar and Pomernaki 1973).



Gain frequency responce of arbitrary op-amp (Bode plot)

Fig 3.3

Potentiostat

We are going to discuss ,in a crude way, that what factor does in general affect the frequency response of potentiostat. Most op-amps have a frequency response of the type as shown in fig3.3. It is a Bode plot X-axis of which is log of frequency and Y-axis is log of gain. The point F1 is called high frequency turnover point or 3db below point, this is the turning point of the gain versus frequency plot of op-amp. Beyond this frequency F1, the gain decreases by 20db/decade (or in Bode plot by the slop -1). The gain reaches at 1(log 1 = 0) at the frequency Fo, called gainbandwidth product and which is given in datasheet). At further higher frequency the slop changes to -2. Same process occurs in case of phase (For detail with refer to any standard electronics book), The phase difference between input and output reaches almost 90 degree at F1 and remains constant when the gain decreases with -1 slope in Bode plot. At the unity gain frequency Fo the phase difference reaches to 180 degree. Further increase in frequency makes the phase shift more than unity, but this makes the output in same phase with that of inverting input due to 180 degree phase shift. Potentiostat if operated in these high frequencies, easily converted in to oscillator!! due to positive feedback rather than negative

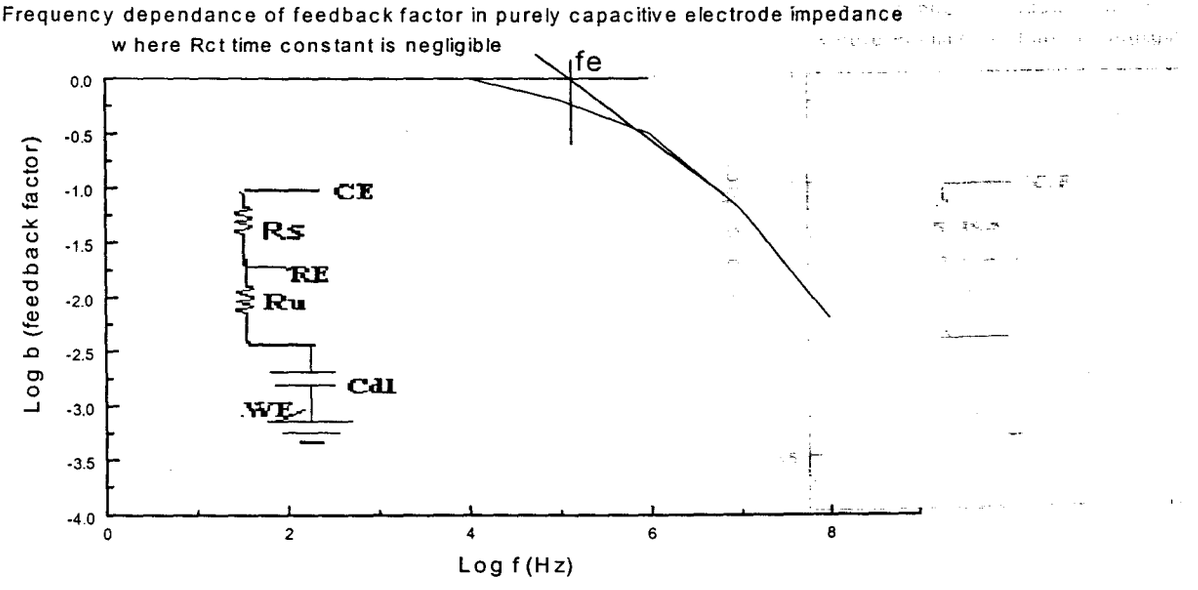


Fig 3.4

Considering the fig 3.2 (b) and the equivalent circuit of purely capacitive cell (Where Rct = 0 or negligible for high frequency), then feedback factor for negative feedback becomes, $b = \dfrac{1/2\pi f C_{dl}}{R_S + R_U + 1/2\pi f C_{dl}}$ .....(3-4)

At frequency $f_e = \{2\pi(R_U + R_S)C_{dl}\}^{-1}$, the feedback factor decreases with a slope -1 in Bode plot. If there are significant resistance R_{ref} in RE lead and capacitance C_{ref} between RE to WE then the feedback factor again takes turn at the frequency $f_r = \{2\pi R_{ref} C_{refl}\}^{-1}$ and decreases by negative slop of -2 in the Bode plot (-40db/decade). As the negative feedback factor decreases the gain increases driving the potentiostat towards oscillation. By doing proper cell adjustment this second turning frequency can be made very large. There are various techniques described in literature to minimise such shortcomings (Ref: Robert Greef, J.physics E Sci.Instrum., Vol. 11, 1978). One must take care of such limitation by proper handling the devices. We will discuss some simple tricks, which will be useful for handling our "home made" devices in later topics.

We are basically intended to design a potentiostat which has large bandwidth, which can be operated upto few mega hertz frequency without any distortion, attenuation and phase shift. In our preliminary testing period we used the fig 3.2 (b) type configuration with AD844 as control amplifier and voltage follower since it has large bandwith 60 MHz and high slew rate 2000V/μs. But AD844, which has complementary bipolar junction is not suitable for voltage follower and it draws sufficient amount of current. So we used CA3140 as voltage follower, which is 4.5 MHz, BiMOS op-amp with MOSFET input and Bipolar output and it has slew rate 9V/μs. We used *Stanford Research System DS 340* function generator as signal source (50Ω output impedance) and the output is viewed in *oscilloscope(1 MΩ input impedance)* with different dummy cells.

With a dummy cell in which Rs = 1.2 kΩ and Ru + Rct =1 kΩ and Cdl = 0 the output (potential at RE) was same as input for a frequency range of 0.1 Hz to 1.2 MHz , when input potential was sine wave of rms value 20 mV. There were 180° phase shift upto 400kHz ,upto 1.2 MHz a phase shift of 150° (+30°) appeared in the output.

With another dummy cell where Rs = 1.2 kΩ , Ru = 20Ω , Rct = 1 kΩ and Cdl = 0.1μF there were zero phase shift and no attenuation in the RE potential with respect to WE (ground) up to 300kHz .The RE potential was same upto 1.2 MHz but the phase shift was 60° at this potential.

When Cdl = 10 μF and all other circuit remaining same the RE potential was same upto 600 kHz with phase shift 20°. The Bode plot of the gain Vs frequency for this dummy cell is shown in Fig3.5, and the Bode plot of phase Vs frequency is shown in Fig3.6. As compared to commercially available *PAR 263A* potentiostat this result was much satisfactory, since it can operate 1.5 decade more than PRA 263A in the frequency band.

But the configuration has some limitation on its current output , since AD844 can deliver maximum 50mA output current , as specified by the manufacturer. For many experiment in which the current requirement are low it can safely be used but the power booster in the output of control amplifier is desirable for various type of application.

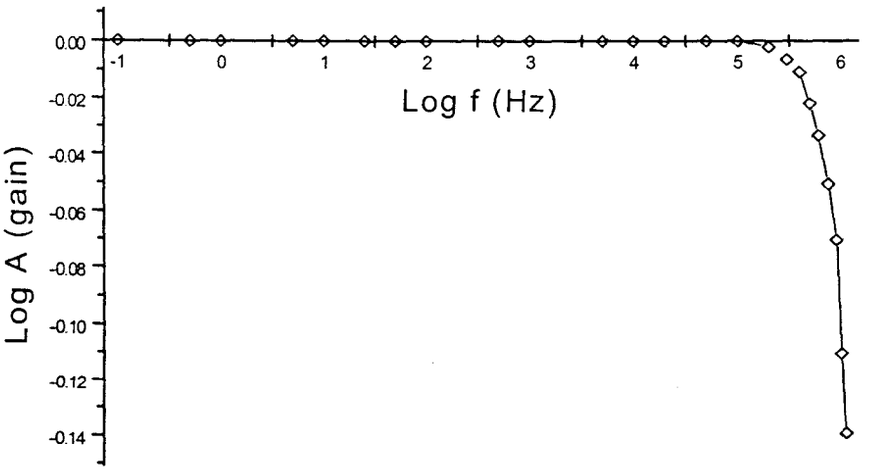


Fig3.5

Bode plot of feedback voltage gain (RE potential divided by input voltage in dummy cell) with frequency , when Cdl = 10 microfarad, Rs=1200 ohm , Ru=20 ohm, Rct=1000ohm

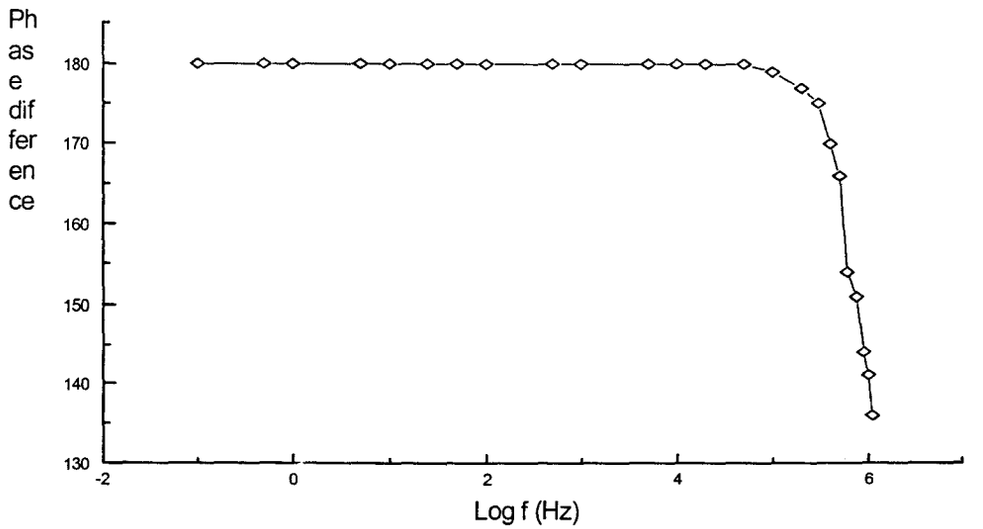


Fig3.6

The plot of frequency Vs the phase difference between input and the RE potential of dummy cell when sinusoidal signal of 20mV was applied, in the potentiostatic configuration of Fig 3.2 (b). Dummy cell with Cdl=10microfarad, Ru=20ohm, Rs=1.2kohm and Rct=1kohm

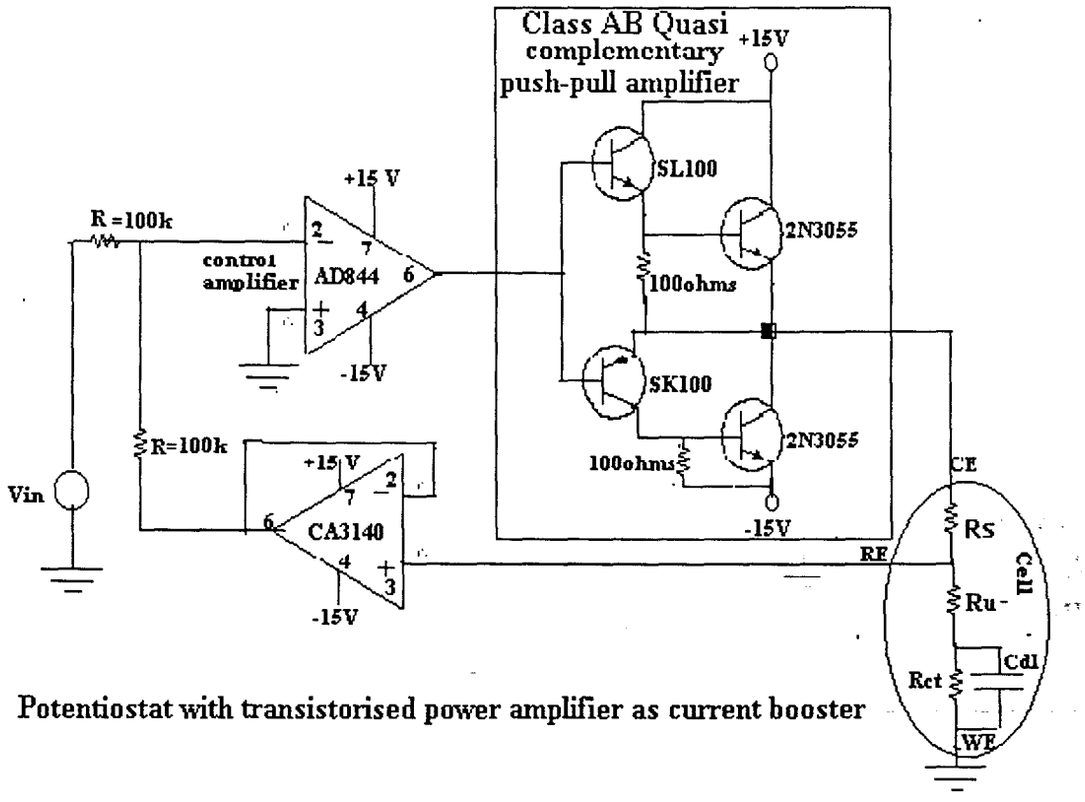
3.1 Current booster

Some electrochemical applications require high voltage as well as high current. The low power op-amp like AD 844 can't deliver high voltage and current so some sort of boosting of current as well as voltage is required.

The frequency response of single transistor power amplifier is seriously limited due to the transformer characteristics that require at the output. So two transistor complementary push-pull class AB amplifier, which has low output impedance due to emitter follower configuration, can be used to boost the current. If large current is required one can use quasi-complementary symmetry push-pull configuration, in which 2 moderate power complementary (NPN and PNP) transistors and 2 high power similar (or complementary) transistors are used. Two darlington pairs are formed in this configuration. We used moderate power transistor SL100 and SK100 (Complementary NPN and PNP) and 2 power NPN power transistor 2N3055. Fig 3.7 shows the configuration, which we used for boosting the cell, current

Previous type of dummy cell was used to test the frequency response of the combination, but there was large attenuation at about 20 kHz frequency and 20 mV of input sinusoidal signal. Similarly large phase shift occurred at higher frequency. The Bode plot of the voltage gain Vs frequency is as shown in Fig3.8 (The plot of phase Vs frequency is not shown).

Current booster



Potentiostat with transistorised power amplifier as current booster

Fig 3.7

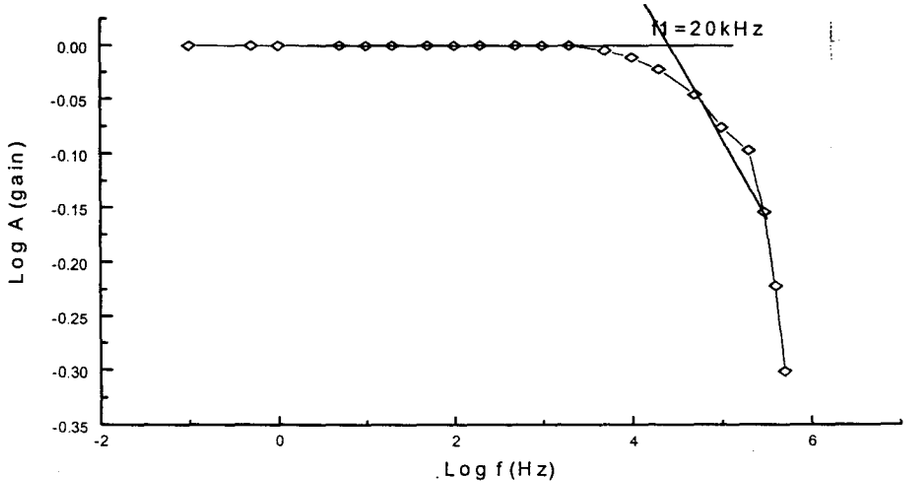


Fig 3.8

The Bode plot of the gain(RE potential divided by input potential in the dummy cell as previous) Vs frequency

Current booster

The above configuration has very poor frequency response so we used some high(moderate) frequency high current power op-amp. PB58A is one that we used as current booster. Here are some features of PB58A as given by manufacturer.

FEATURES

- WIDE SUPPLY RANGE — ±15V to ±150V
- HIGH OUTPUT CURRENT —
  - 1.5A Continuous (PB58)
  - 2.0A Continuous (PB58A)
- VOLTAGE AND CURRENT GAIN
- HIGH SLEW — 50V/ms Minimum (PB58)
  75V/ms Minimum (PB58A)
- PROGRAMMABLE OUTPUT CURRENT LIMIT
- HIGH POWER BANDWIDTH — 320 kHz Minimum
- LOW QUIESCENT CURRENT — 12mA Typical

APPLICATIONS

- HIGH VOLTAGE INSTRUMENTATION
- Electrostatic TRANSDUCERS & DEFLECTION
- Programmable Power Supplies Up to 280V p-p

PB58A has small signal bandwidth, with ±30 volt power supply , 1 MHz at voltage gain 3. It has also comparatively high slew rate, which is useful figure for our use. PB58A has external current limit resistance R_{CL}, from pin number 1 to pin number 2 , The value of R_{CL} is calculated as,

$+I_L = 0.65/ (R_{CL} + 0.01)$,
$-I_L = 0.65/R_{CL}$.

Where R_{CL} is in Ω and I_L is in Ampere. We have limited the load current to 1.3 Ampere by putting $R_{CL} = 0.5\ \Omega$.

Cascading two amplifiers within a feedback loop has many advantages, but also requires careful consideration of several amplifier and system parameters. The most important of these are gain, stability, slew rate, and output swing of the driver. Operating the booster amplifier in higher gains results in a higher slew rate and lower output swing requirement for the driver, but makes stability more difficult to achieve. For the stability, the gain of the booster is fixed to minimum value and the driver (control amplifier in our case) is free to control overall gain. The slew rate of the closed loop is the booster gain times the slew rate of control amplifier maximum upto slew rate of booster. Here control amplifier AD844 has very high slew rate 2000 V/μs so overall slew rate is theoretically equal to the slew rate of booster 75 V/ μs. The slew rate decreases by minimising the booster gain but this is to be paid for the stability.

Current booster

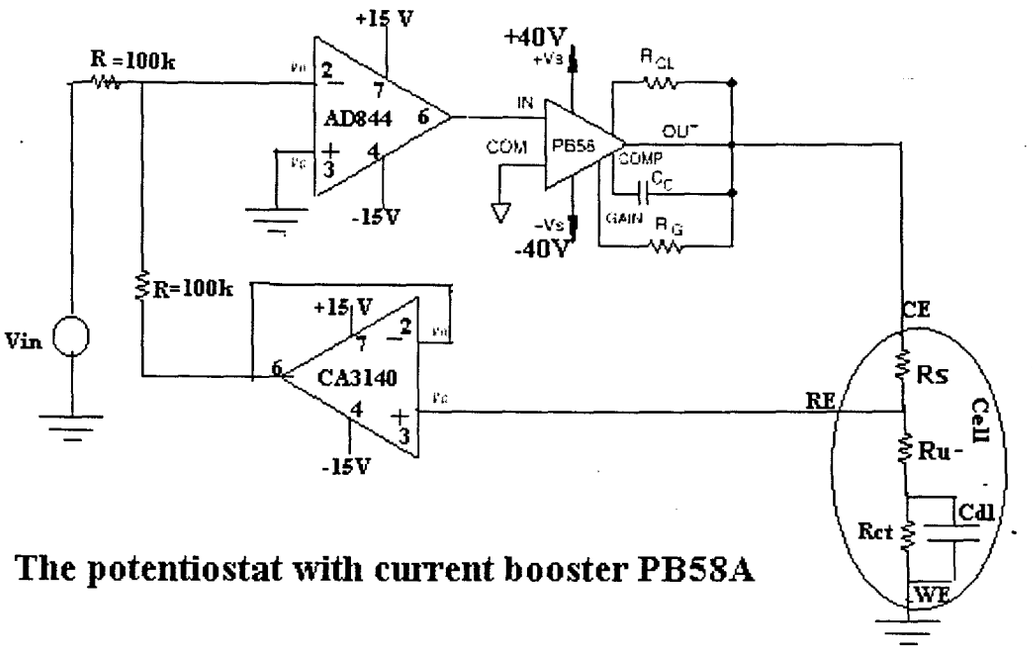
The phase shift inside the closed loop is minimised by using a compensation capacitor Cc between the pin 1 to 8 in PB58A. This value is given in datasheet , we have used 10pf for this purpose.

The gain of booster is set by using an external resistance R_G between pin number 7 to 1 by the following relation. (Given by datasheet, which can be realised by studding the internal equivalent circuit , see datasheet of PB58A)

$$R_G = \left[\left(A_V - 1\right)3.1k\Omega\right] - 6.2k\Omega$$

$$\text{or, } A_V = \frac{R_G + 6.2k\Omega}{3.1k\Omega} + 1$$

Where A_V is the gain of booster. R_G is kept equal to zero in our configuration for stability so that the gain of booster remains minimum(=3).



The potentiostat with current booster PB58A

Fig 2.10

The power booster is inserted in the loop of the control amplifier and cell through voltage follower forming a closed negative feedback loop as shown in Fig 2.10. Since the control amplifier supply voltage is ±15 volts, the control amplifier output can oscillate upto ±11V (see data sheet). The power booster has constant gain of 3 so for it to oscillate it requires more than 35 Volts. Even though the booster works at ±15 V, to avoid the saturation ±40 V supply is given to it. The whole PB58A power op-amp is mounted in a proper heat sink. For small value of Cdl (Not purely capacitive cell in Electrochemist's terminology) it can control the potential upto 1 MHz !! within 10% error and about 30 degree phase shift.

The dc performance of the potentiostat is another measure of accuracy. The voltage follower CA3140 has maximum dc error of 5 mV. This figure is pretty large, but it can be minimised by using the null offset option (see the datasheet).

3.2 Measurement of Cell Current

Cell current measurement requires another important consideration. Since the whole cell is 'inside' the loop of the feedback to control amplifier, one cannot insert any mechanical or passive current measuring instrument in the loop. If one does so the whole circuitry will be disturbed and can't get required result within certain limit of accuracy. Direct current measuring is rather difficult and not accurate method. Many current measuring instruments actually measure voltage that is produced across a known resistor when the current flows through that resistor. There are basically two methods of measuring current in a cell, which are discussed in many literatures and followed by the electrochemist and the instrument manufacturers.

1) Using Instrumentational amplifier.
2) Using current to voltage converter.

1) Cell current measurement by instrumentational amplifier

As already mentioned the three op-amps configuration (Two CA3140 and one AD844) as shown in fig 3.10 forms so called instrumentational amplifier. It measures the difference between two inputs. Here all the resistances are equal (10k ±1%) so the gain of the instrumentational amplifier is 1. It draws negligible amount of current from the cell current path . A resistance of known value R is inserted between the booster output (not shown in fig) and the counter electrode and across it the two inputs of instrumentational amplifier is connected. If Vo is the voltage read at the output of Instrumentational amplifier due to a flow of current I in the cell then,

$$I = Vo/R$$

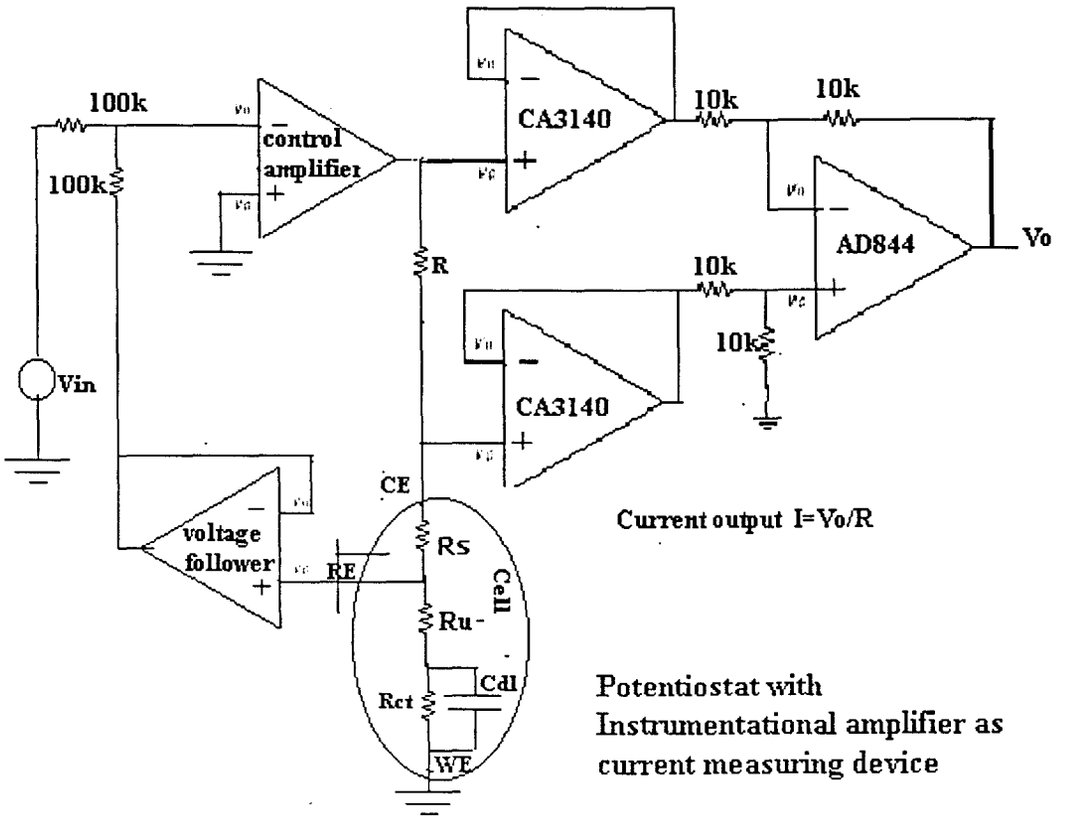


Fig 3.10

Thus the current is read in this configuration. The main advantage of this configuration is that another power booster is not required for the measurement of current as in current to voltage converter and also low power op-amps which are used here are less or more free from the bandwidth and slew rate limitations.

2) Cell current measurement by current to voltage converter

In this configuration, as shown in fig 3.11, the working electrode is connected with the inverting input of the current to voltage converter with booster (Because the same amount of current that is given by the control amplifier booster must supply by the output of the converter). Since the noninverting input of the converter is grounded, the WE is at virtual ground and rest processes are same. A known resistance R is connected between the output of current to voltage converter to its inverting input. The whole current that flows through the cell is supplied through R so an inverted output voltage is set in the converter's output. If 'I' is the current flowing through the cell and Vo is output voltage then current through the cell is,

$$I = Vo/R$$

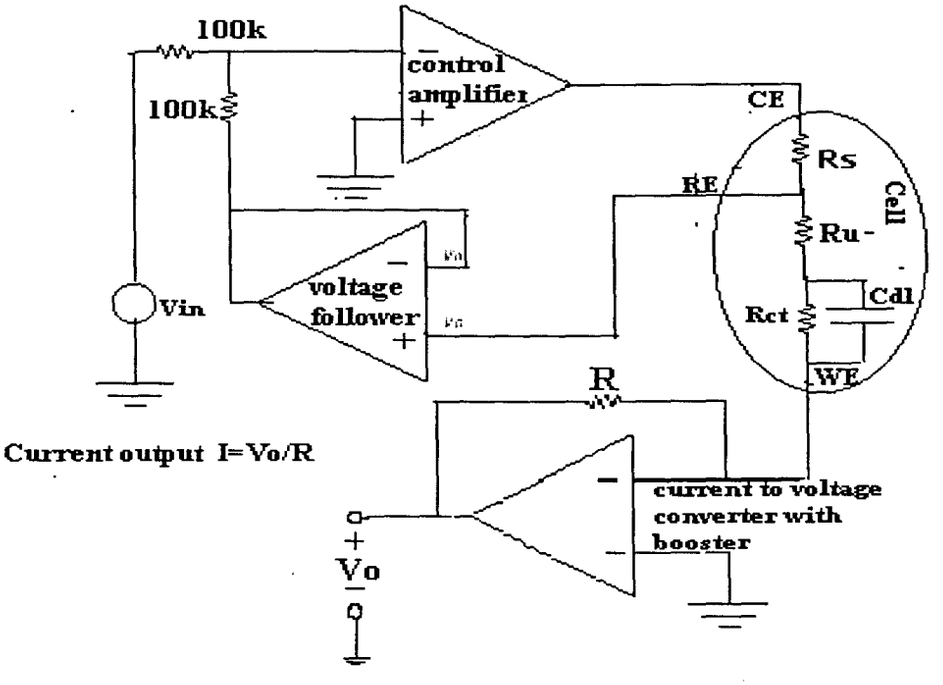


Fig 3.11

The main advantage of this configuration is that the feedback loop, which the cell forms, remains unaffected. But we prefer the instrumentational amplifier to measure the current not because the second method is worst but because of our slew rate and the high frequency requirement. Since we have used AD844 as the control amplifier here also for

the same reason Ad844 has to be used but AD844 has very small (50 ohm) inverting input resistance. So AD844 can't be used as converter.

Compensation of uncompensated resistance R_U

Since there are always some resistance between RE and the electrolyte surrounding of WE called RU, uncompensated resistance, which always wrong value of WE potential by an amount I R_U when a current I flows through the cell. There are many techniques described in literatures to decrease it. By electronic configuration the voltage drop across it can be compensated just by giving a positive feedback to the control amplifier. The positive is given through a potentiometer. A potentiometer of 10k and 10 turn can be applied for this purpose. One edge of potentiometer is grounded and another end is connected with the current output. The sliding end of potentiometer is connected to the control input through a resistor, which is equal to the resistance from input source to the inverting input of the control amplifier. Since current output is in phase with the input the input signal, the feedback will be positive feedback. If RU is known then a fraction R_U /R of current output can be fed back to compensate it where R is resistance across the two input of unity gain instrumentational amplifier measuring current.

If RU is not known then there is no hard and fast rule for the compensation (see ref.) and the positive feedback is increased below a point at which the potentiostat just start to oscillate.

3.3 Galvanostat

A galvanostat maintains constant current through the cell by the use of feedback circuitry. Whatever the change in cell impedance the galvanostat must maintain the same current. A simple galvanostat circuit is shown in fig 3.1

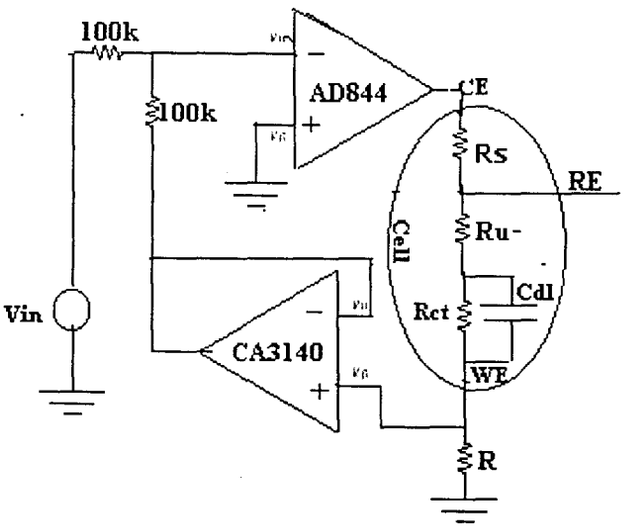


Fig 3.12

Fig 3.12 is like a potentiostatic circuit, only the difference here is that, the WE is connected with ground through an external resistance R and the feedback voltage follower is connected with WE in place of RE. If input potential Vin then the voltage follower input must be equal to Vin. If I is current flowing through the cell then,

$$I = \frac{V_{in}}{R}$$

By changing the value of R one can easily set the required value. A potentiostat can thus easily converted into galvanostat so we are not discussing the galvanostat in detail. Our potentiostat can operate in both modes. When the instrument is set to galvanostatic mode WE is connected to voltage follower and the instrumentational amplifier is connected across RE and WE. Similarly the current output in potentiostatic mode becomes potential output (potential between RE and WE) and the potential output in potentiostatic mode becomes current output in galvanostatic mode, but this flip is done internally so one can read current and potential as it is .

4.Design

4.1 Design and Fabrication

The instrument has been designed to operate for both potentiostatic and galvanostatic mode. The main circuit diagram is as shown in fig 4.1. All the values of the resistors and capacitors are as already mentioned. The printed circuit board (PCB) was designed using ORCAD PCB II software. The layout of PCB is given in Appendix 1.

To control the output current a current limiting resistance is connected between control output to the counter electrode (CE). There are two different resistors, which can be changed by using 2 pole-2 ways rotary switch marked as current range. At 'HI' mode there is 2 ohms resistor and at 'LO' mode there is 1000 ohms resistor.

To measure the current in the potentiostatic mode a resistor is connected between current range resistor to the counter electrode. The resistor is mounted in 5 ways-2 poles rotary switch, marked as 'current sensitivity'. The instrumentational amplifier inputs are connected across this resistor. The output of instrumentational amplifier directly reads the current in mA (in the potentiostatic mode) multiplied by the current sensitivity.

The resistances across the two inputs of instrumentational amplifier and the output current sensitivity multiplication factors have the following relations :

Current sensitivity	Resistances
×100	10 Ω
×10	100 Ω
×1	1000 Ω
×0.1	10000 Ω
×.0.01	100000 Ω

This instrument has its own power supply. A 30-0-30 Volts (100-mA) transformer has been used for main power supply to the instrument. By rectifying it , 1000 μF capacitors have been used to filter . It produces 42 Volts unregulated dc voltage . This 42-0-42 Volts dc supply has been given to the current booster. By the same 42-0-42 Volts dc supply 15-0-15 Volts dc has been regulated using 7815 and 7915 regulator ICs. This 15-0-15 Volts supply has been given to the rest of the op-amps.

The whole instrument has been fitted in a 15'×10'×8' aluminium box. Two LED DPMs (Digital Panel Meter) of 2 Volts range have been mounted in the front panel of the instrument. One reads dc current and another reads dc potential output . The power supply for the panel meter is separate. This is supplied by another transformer and 5 Volts regulator (7805 IC).

In the galvanostatic mode the instrumentational amplifier comes across RE and WE and reads the potential difference between RE and WE .Similarly the voltage follower connects with WE and the inverter connected in the output of the voltage follower reads the current. The current sensitivity resistance in the galvanostatic mode comes between WE and ground. The current multiplication factor is same as in the case of the potentiostatic mode.

Before doing the experiment rest potential between WE and RE should be measured and required value of potential has to be given . For this purpose three way two pole rotary switch has been used and marked as 'mode'. At the dummy mode the instrumentational amplifier comes across RE and WE, while rest of the internal circuitry is disconnected to the cell. The internal feedback circuitry is completed by using a 'dummy' cell (10 kΩ and 1 kΩ) . At this mode both current DPM and potential DPM read the rest potential of the WE.

In the 'set' mode still the instrumentational amplifier is connected to RE and WE and rest of internal circuit is disconnected to the cell. But the potential DPM is connected to the variable end of dc potentiometer, which is graduated and can supply a dc voltage -1 volt to +1 volt. This voltage is applied to the cell through an inverter and in the set mode this voltage can be set at rest potential of the WE. The potential DPM reads the set potential while the current DPM reads the rest potential so it is easy to set at required value. At the 'measure' mode the potentiostat is connected to the cell and starts controlling the potential.

For large current (greater than 100 mA) requirement one can use external power supply 40-0-40 volts , which can be connected to the instrument by changing the switch marked as 'POWER SUPPLY' to the 'EXT' mode. Otherwise the power supply mode has to be kept at 'INT' mode. Since main power consumption is only in the current booster, the internal power supply 15-0-15 Volts for the rest circuit remains same.

We have not done computer interfacing but we have connected one connector in the back panel, which may be useful for computer interfacing. Similarly IR compensation has not been connected but if requires it can be readily connected. One 10-k potentiostat has been mounted there for IR compensation, which is not connected in the circuitry.

4.2 Safety Precaution

1) The instrumentational amplifier has two-voltage follower CA3140 and if they are not connected in a loop or at fixed potential (i. e. hanging) they may burn out or damage due to the feedback. so there is 1-MΩ resistor connected across the two inputs of the instrumentational amplifier, to avoid the damage. Since 1 MΩ is very large resistance for our experimental purpose , the error introduce is negligible.

2) The current booster has high supply voltage (±40 Volts) . If by any means the output oscillates at high voltage then the instrumentational amplifier at first burns out. To

avoid this 2 Zener diode(each of 10 Volts) along with 2 general diodes have been used between current range resistor to ground in a manner such that if potential in the output is larger than ±10.7 Volts, then the current passes through the zener , letting the point at same potential.

4.3 Some suggestion for handling

1. Always switch on the device at the dummy mode

2. Switch on the device after proper connection with the cell , this reduces the noise.

3. If noninverting input has not to be given, then ground it before switching on . If non-inverting input has to be given then connect with the input first and then switch on. (For the inverting input it is not compulsory)

4. Set the rest potential at set mode.

5. What ever the potential is shown by DPM apply the potential at the set mode. (i.e. if positive 0.5 volts is shown then apply positive 0.5 volts)

6. In the measure mode the sign of potential will be reversed because of inverter and current reads in opposite sign to the potential

7. If purely Capacitive cell is under study then prefer the higher current sensitivity multiplication factor (× 100 mA).The current sensitivity for lower frequency may be at lower multiplication factor but as the frequency increases change it to higher one. This is due to the less impedance between RE and WE at higher frequency , which decreases the negative feedback factor. As the negative feedback decrease below certain level the error in potential control increase. As you increase the multiplication factor, the resistance between the control output and the counter electrode decreases letting the control output voltage go down(less amplification). In this way the performance will increase.

8. If high resistive system is under study then prefer lower multiplication factor of current sensitivity.

9. Put the current range at 'HI' in general, unless there is very high resistive system.

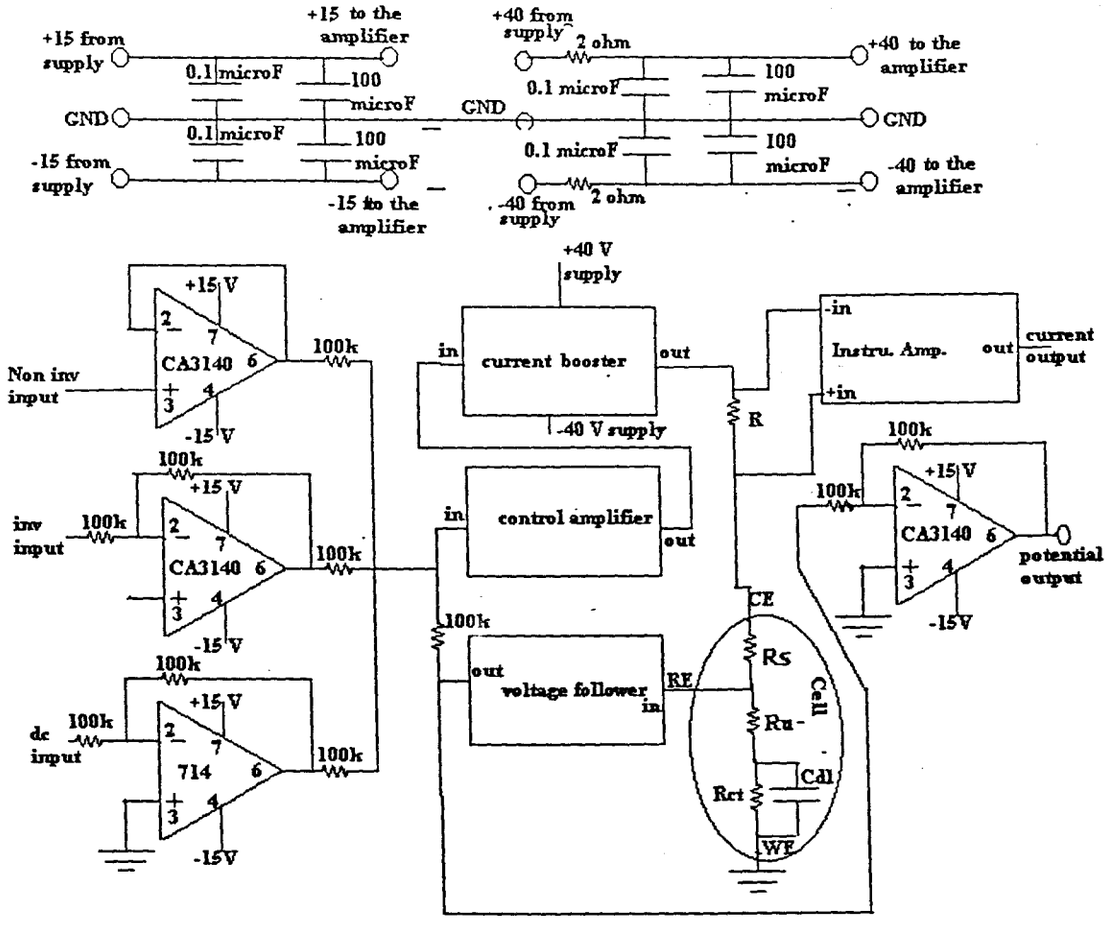


Fig 4.1 **Complete circuitary of the potentiostat**

5. ESI studies using potentiostat

After completing the fabrication we tested the instrument using one dummy cell and two real electrochemical cells. Lock-In amplifier SR830 DSP was used to give the signal and detect the output. The input signal was 4 mV for all the experiments.

1. Dummy cell

The dummy cell was Randles cell model with the following values of passive elements. (These are their actual values measured by standard instruments)

Cdl = 0.106 μF
Rct = 500 Ω
Ru = 22 Ω
Rs = 1000 Ω

The impedance of the cell is just the ratio of the potential to the current output. Since the Randles cell model has two time constants giving two corresponding frequencies,

$f_1 = \{2\pi C_{DL}(R_U+R_{CT})\}^{-1}$

$f_2 = \{2\pi C_{DL}R_U\}^{-1}$

The Bode plot of impedance | Z | Vs frequency f , of the dummy cell is given in fig 5.1 From the plot the first turnover frequency occurs at log f_1 =3.4484 and second turnover frequency occurs at log f_2 = 4.86111 with corresponding log | Z_1| = 2.719047 and log | Z_2 | = 1.3625397

$Z_1 = R_U+R_{CT}$ and $Z_2 = R_U$

By these data

R_U+R_{CT} = 523.657852 Ω , R_U = 23.3482 Ω and C_{DL} = 0.1081 μF

The result for R_{CT} is less than 0.01% error. The error for R_U is with in 5% and the error for C_{DL} is with in 2%.

2. Electrochemical cell 1

In this cell we used Silver modified with octadecanethiol (Ag, $CH_3(CH_2)SH$) as working electrode , saturated calomel reference electrode, Platinum counter electrode with 0.1 normal NaOH solution. The area of the WE was 0.5 square c.m.

The Bode plot of the impedance Vs frequency is shown in fig 5.2

From the plot the first turnover frequency occurs at log f_1 =0.106066 and second turnover frequency occurs at log f_2 = 4.638528 with corresponding log | Z_1| = 4.5210084 and log | Z_2 | = 1.24369748

$Z_1 = R_U+R_{CT}$ and $Z_2 = R_U$

By these data

R_U+R_{CT} = 33190.1 Ω , R_U =26.53Ω and C_{DL} = 3.75μF

Hence we concluded that the double layer capacitances in this case is 7.51 μF per square c.m.

3. Electrochemical cell 2

In this cell we used Armco Iron as working electrode , sulphate (Hg/Hg_2SO_4) reference electrode, Platinum counter electrode with 1 normal H_2SO_4 solution. The area of the WE was 1.17 square c.m.

The Bode plot of the impedance Vs frequency is shown in fig 5.3

From the plot the first turnover frequency occurs at log f_1 =1.21212121 and second turnover frequency occurs at log f_2 = 3.3080808 with corresponding log | Z_1| = 1.90966387 and log | Z_2 | = 0.24789916

$Z_1 = R_U+R_{CT}$ and $Z_2 = R_U$

By these data

R_U+R_{CT} = 81.22 Ω , R_U =1.05 Ω and C_{DL} = 120.2 μF

Hence we concluded that the double layer capacitances in this case is 103 μF per square c.m.

This cell configuration has very high capacitance and very low charge transfer resistance. After the upper turning frequency the negative feedback became so small that the potential started to increase. To minimise the error, the current sensitivity must keep at higher multiplication factor as already mentioned. We can see the sudden rise in the impedance in the plot , it is due to rise in the potential after negative feedback became very small.

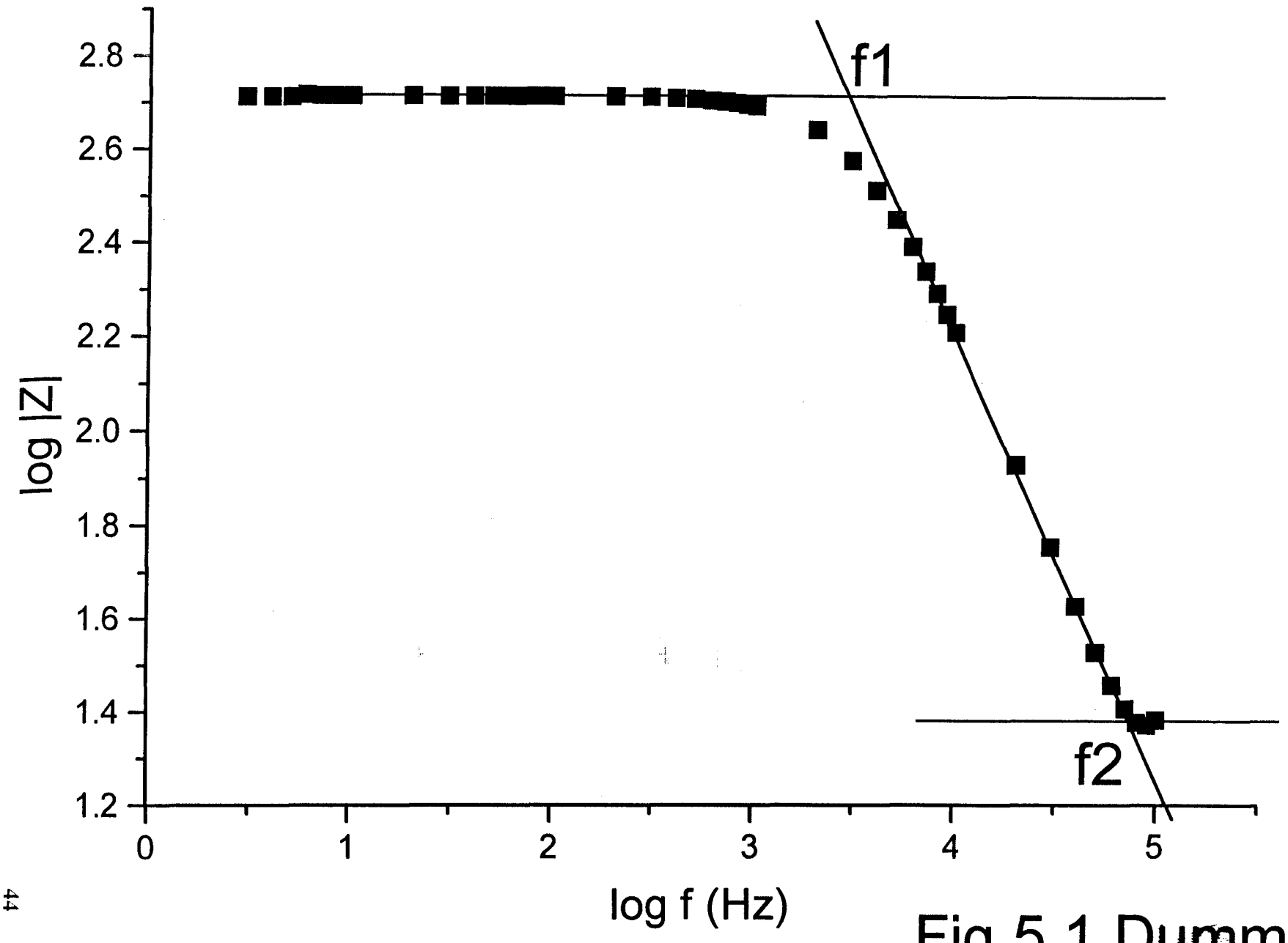


Fig 5.1 Dummy

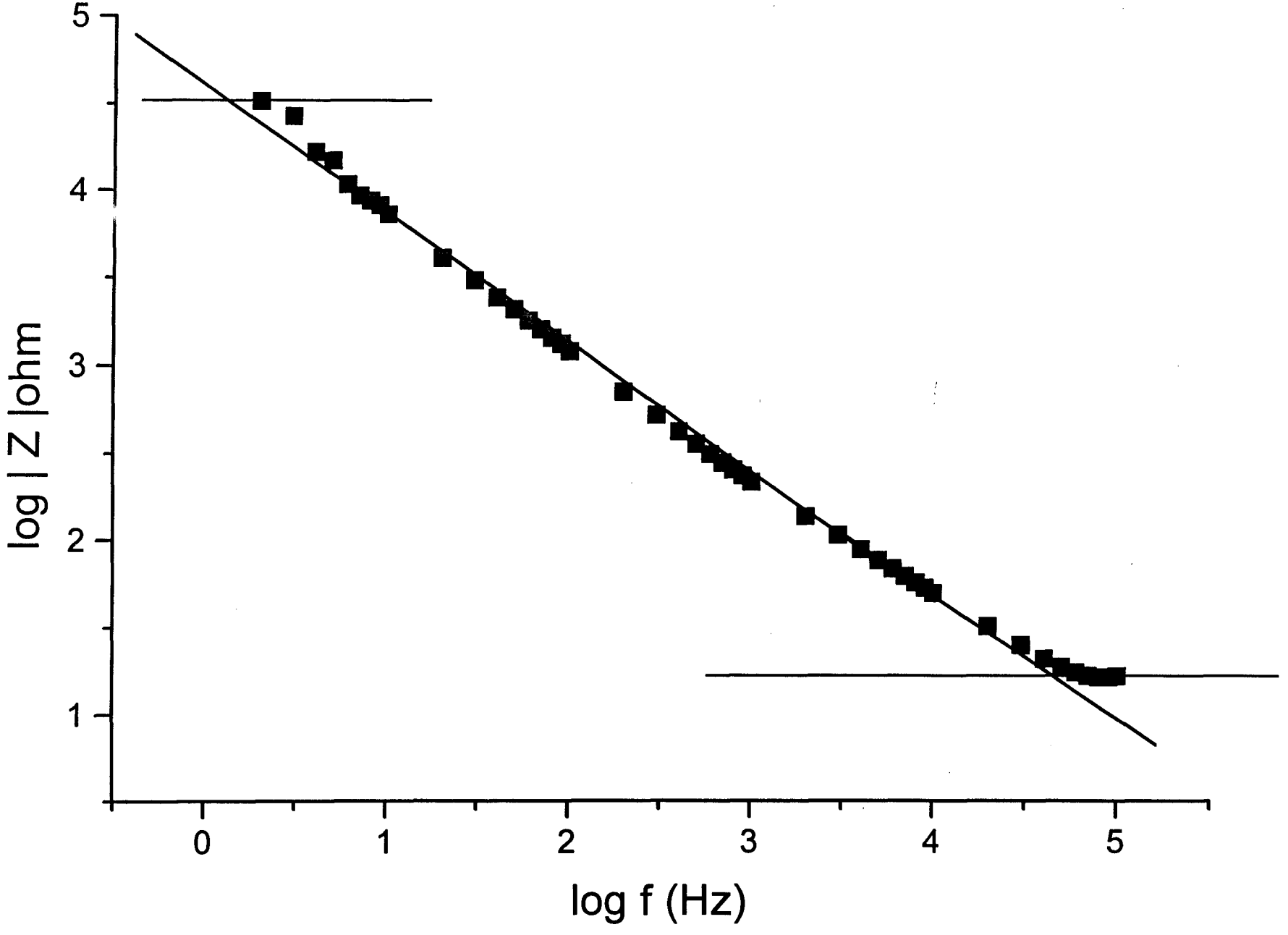


Fig 5.2 Plot of the EIS data for Octadecanethiol modified silver in 0.1N NaOH

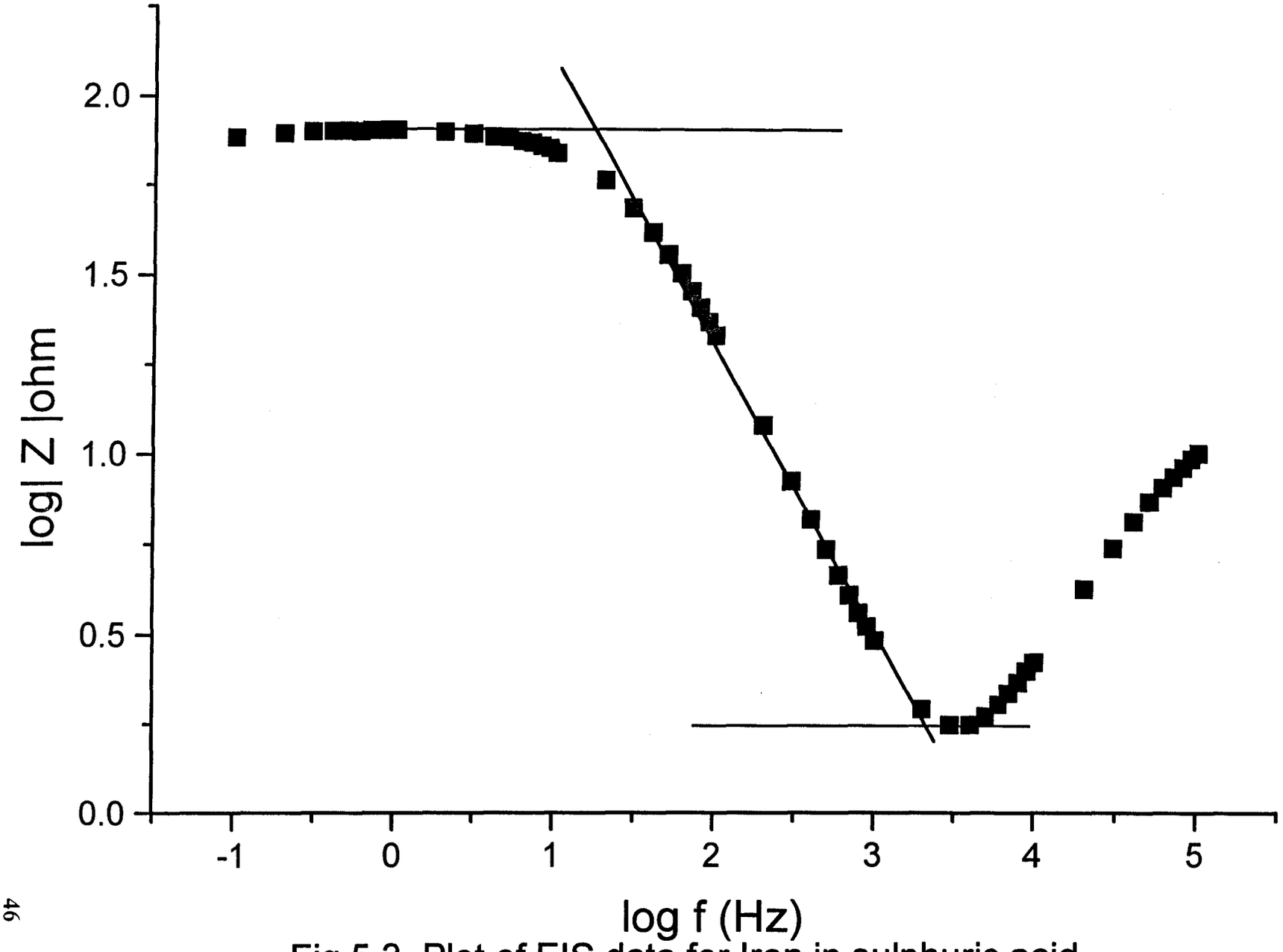


Fig 5.3 Plot of EIS data for Iron in sulphuric acid

CONCLUSION

The main aims of the project were;

1. **To design the high bandwidth potentiostat and galvanostat**
2. **To fabricate it.**
3. **To study the feasibility of using this device for electrochemical systems.**

Designing

Many potentiostats that are available have poor high frequency response. Commercially available potentiostats, having good high bandwidth, are very expensive. So we intended to design high bandwidth potentiostat and galvanostat to study electrochemical systems. We started testing different possible configuration choosing high frequency operational amplifiers, which are heart of this instrument. By matching the characteristics of op-amp, which are available in local market, we designed the potentiostats that can operate within 6 decades of frequency band. We found there is no phase shift and attenuation of input signal even at 100kHz. Nowadays many research experiments are computer controlled and this is true for commercially available potentiostats. The instrument can also interfaced to a PC.

Fabricating

The main PCB has been designed using ORCAD PCB II software. Power supply PCB is handmade one. The whole circuitry has been fitted inside a box of dimension 16"×10"×8". The front panel was properly drilled in the RRI workshop. The proper marking of the switches has been done. The picture of the instrument is given in Appendix 2.

Feasibility in electrochemical experiments

By using this instrument with lock-in amplifier for applying input and detecting output, we have made some impedance measurement. We tested it with dummy cell with known impedances and compared with the value obtained from it using known EIS method. The results were very good in the sense that errors were negligible. We used Randles cell model as dummy cell with Cdl =0.106 μF, Rct = 500 Ω and Ru = 22 Ω and the values obtained from experiment were Cdl = 0.108 μF, Rct = 500.3 Ω and Ru = 23.3 Ω.

Similarly we tested it in potentiostatic mode with electrochemical cells. One with silver as WE in 0.1 normal NaOH solution and found the double layer capacitance 7.509

μF per square c.m. Another with Armco Iron WE in 1 normal sulphuric acid and found double layer capacitance 103 μF per square centimetre. These results show that the instrument can be used in various electrochemical control system with practical accuracy.

References

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Donald T. Sawyer and Julian L. Roberts, JR. , John Wiley & Sons , Inc. 1974

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Allen J. Bard and Larry R Faulkner, John Wiley & Sons , Inc. 1980

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6) Robert Greef, J. Phys E: Sci. Instrum. Vol.11, p.1 (1978)

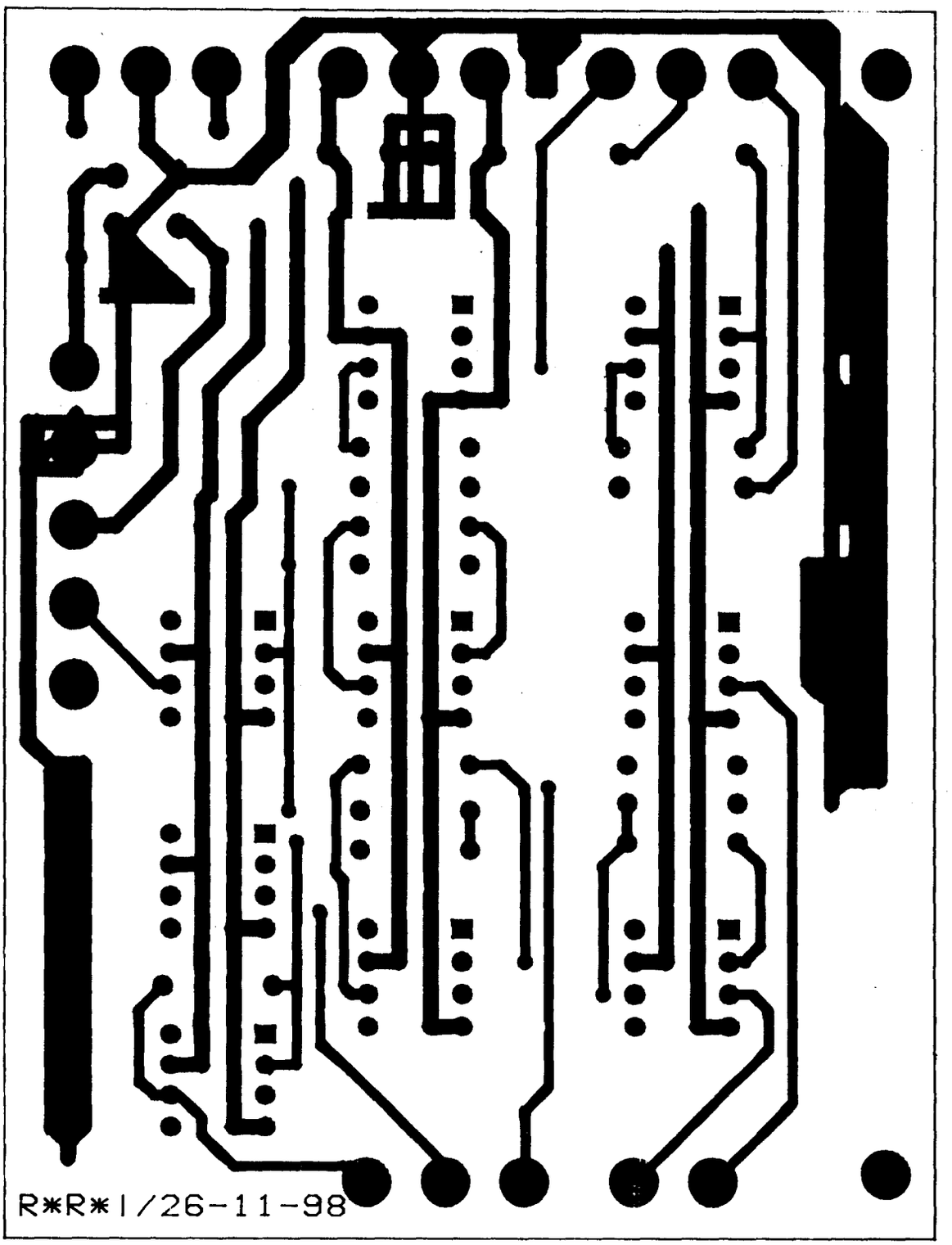
7) J. Lecoeur, C. Koehler & J. P. Bellier, Vol. 69 p.3031 (1998)

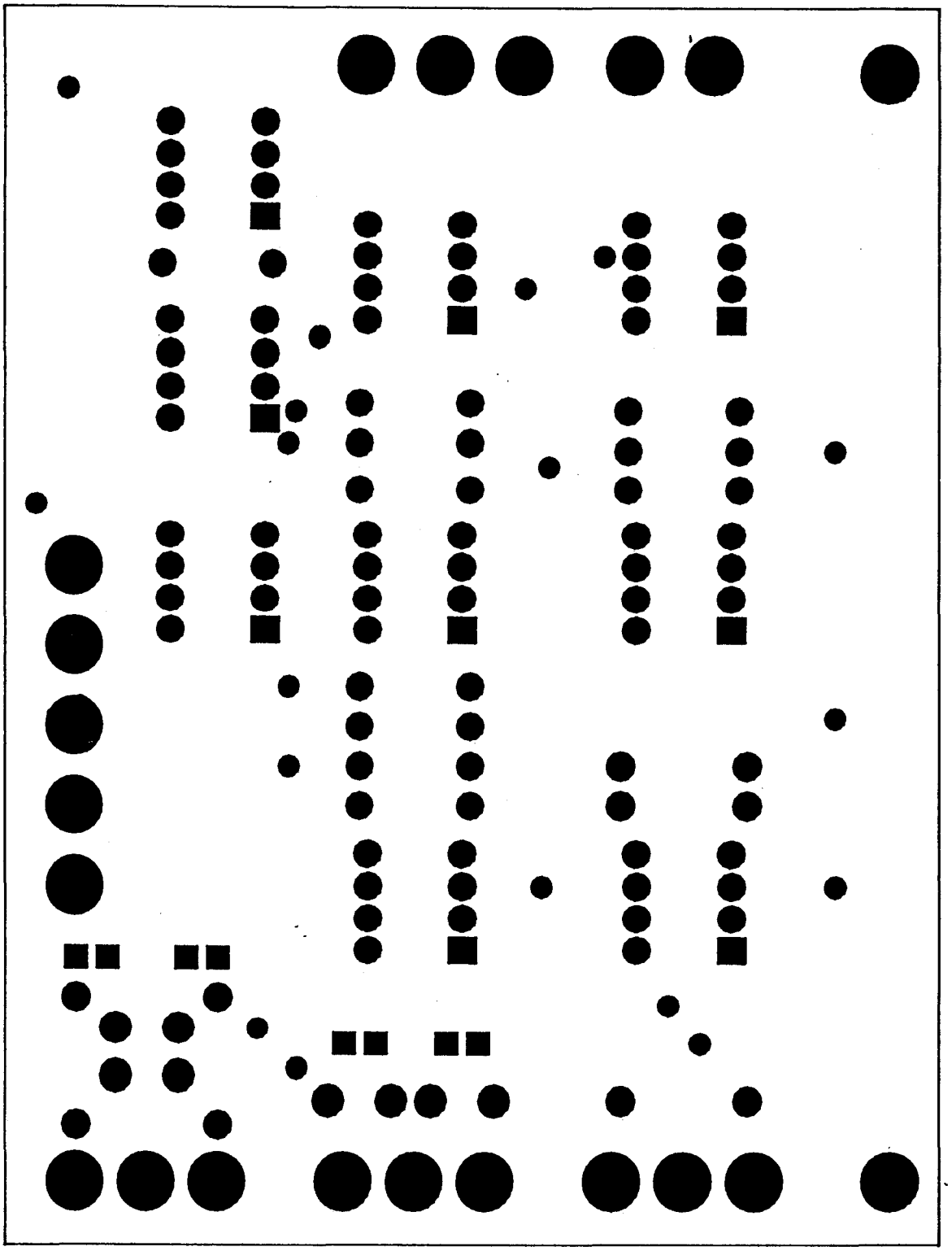
8) L. Kirkup, J. M. Bell, D. C. Green, G. B. Smith & K. A. MacDonald, Rev. Sci. Instrum. Vol 63 No 4 p.2328(1992)

9) M. S. Harrington, L. B. Anderson, J. A. Robbins & D. H. Karweik Rev. Sci. Instrum. Vol 60 No 10 p.3323(1989)

10) O. R. Brown, J. Phys E: Sci. Instrum. Vol.5, p.365 (1972)

Appendix 1

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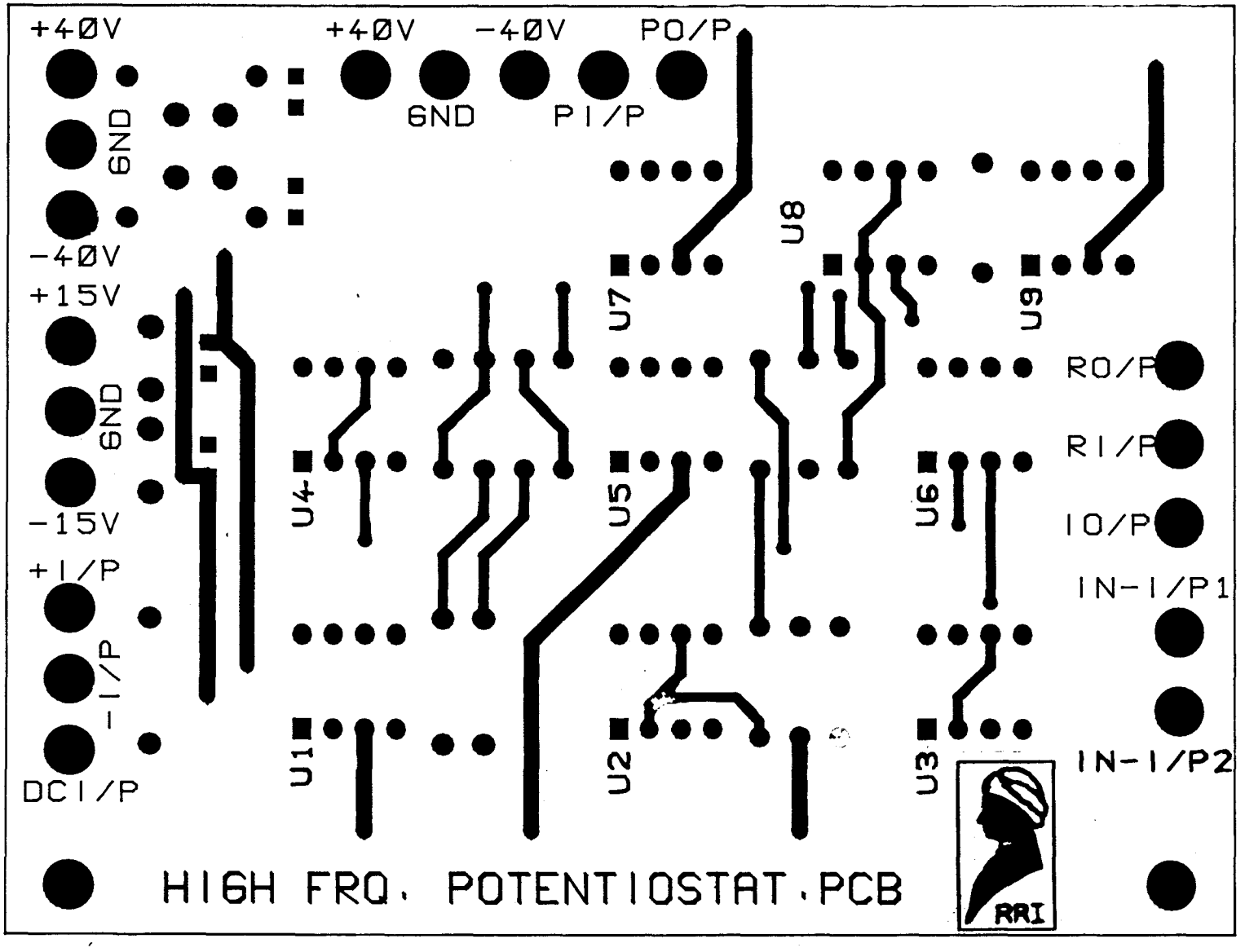
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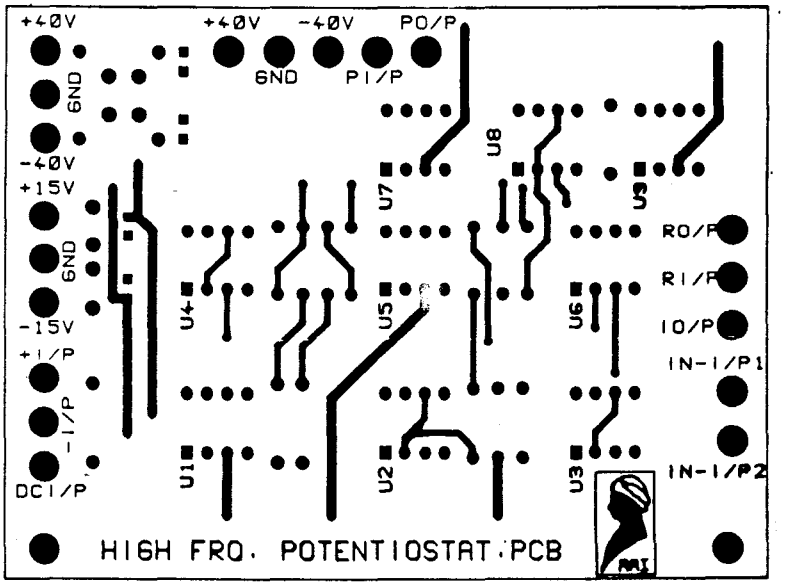
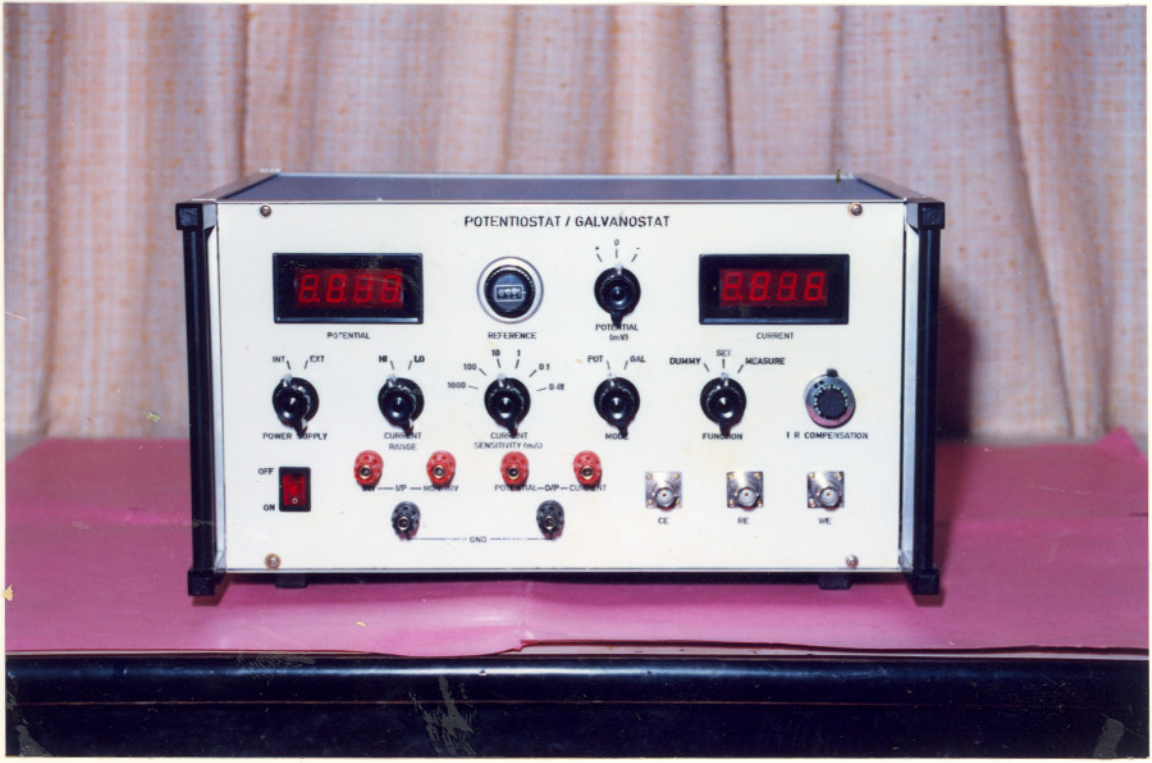
+40V
-40V
PO/P
GND
PI/P
GND
-40V
+15V
GND
-15V
+I/P
-I/P
DCI/P
U1
U2
U3
U4
U5
U6
U7
U8
U9
RO/P
RI/P
IO/P
IN-I/P1
IN-I/P2
HIGH FRQ. POTENTIOSTAT.PCB
RRI


+40V
+40V
-40V
PO/P
GND
P1/P
-40V
+15V
GND
-15V
+I/P
-I/P
DCI/P
U1
U2
U3
U4
U5
U6
U7
U8
S
RO/P
RI/P
IO/P
IN-I/P1
IN-I/P2
HIGH FRQ. POTENTIOSTAT PCB

Appendix 2


POTENTIOSTAT / GALVANOSTAT
POTENTIAL
REFERENCE
POTENTIAL (mV)
CURRENT
INT
EXT
POWER SUPPLY
HI
LO
CURRENT RANGE
100
10
1
0.1
1000
0.01
CURRENT SENSITIVITY (mA)
POT
GAL
MODE
DUMMY
SET
MEASURE
FUNCTION
I R COMPENSATION
OFF
ON
UP
POTENTIAL
O/P
CURRENT
GND
CE
RE
WE

ANALOG DEVICES

60 MHz, 2000 V/μs Monolithic Op Amp

AD844

FEATURES

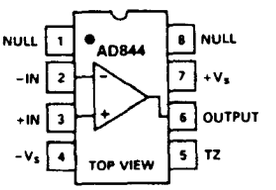
Wide Bandwidth: 60 MHz at Gain of –1
33 MHz at Gain of –10
Very High Output Slew Rate: Up to 2000 V/μs
20 MHz Full Power Bandwidth, 20 V pk-pk, R_L = 500 Ω
Fast Settling: 100 ns to 0.1% (10 V Step)
Differential Gain Error: 0.03% at 4.4 MHz
Differential Phase Error: 0.15° at 4.4 MHz
High Output Drive: ±50 mA into 50 Ω Load
Low Offset Voltage: 150 μV max (B Grade)
Low Quiescent Current: 6.5 mA
Available in Tape and Reel in Accordance with EIA-481A Standard

APPLICATIONS

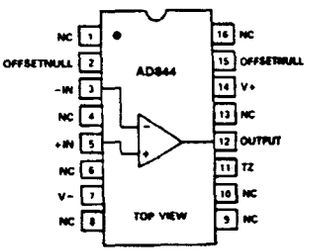
Flash ADC Input Amplifiers
High Speed Current DAC Interfaces
Video Buffers and Cable Drivers
Pulse Amplifiers

CONNECTION DIAGRAMS

8-Pin Plastic (N), and Cerdip (Q) Packages



16-Pin SOIC (R) Package



PRODUCT DESCRIPTION

The AD844 is a high speed monolithic operational amplifier fabricated using Analog Devices' junction isolated complementary bipolar (CB) process. It combines high bandwidth and very fast large signal response with excellent dc performance. Although optimized for use in current to voltage applications and as an inverting mode amplifier, it is also suitable for use in many noninverting applications.

The AD844 can be used in place of traditional op amps, but its current feedback architecture results in much better ac performance, high linearity and an exceptionally clean pulse response.

This type of op amp provides a closed-loop bandwidth which is determined primarily by the feedback resistor and is almost independent of the closed-loop gain. The AD844 is free from the slew rate limitations inherent in traditional op amps and other current-feedback op amps. Peak output rate of change can be over 2000 V/μs for a full 20 V output step. Settling time is typically 100 ns to 0.1%, and essentially independent of gain. The AD844 can drive 50 Ω loads to ±2.5 V with low distortion and is short circuit protected to 80 mA.

The AD844 is available in four performance grades and three package options. In the 16-pin SOIC (R) package, the AD844J is specified for the commercial temperature range of 0°C to +70°C. The AD844A and AD844B are specified for the industrial temperature range of –40°C to +85°C and are available in the cerdip (Q) package. The AD844A is also available in an 8-pin plastic mini-DIP (N). The AD844S is specified over the military temperature range of –55°C to +125°C. It is available in the 8-pin cerdip (Q) package. "A" and "S" grade chips and devices processed to MIL-STD-883B, REV. C are also available.

PRODUCT HIGHLIGHTS

1. The AD844 is a versatile, low cost component providing an excellent combination of ac and dc performance. It may be used as an alternative to the EL2020 and CLC400/1.
2. It is essentially free from slew rate limitations. Rise and fall times are essentially independent of output level.
3. The AD844 can be operated from ±4.5 V to ±18 V power supplies and is capable of driving loads down to 50 Ω, as well as driving very large capacitive loads using an external network.
4. The offset voltage and input bias currents of the AD844 are laser trimmed to minimize dc errors; V_{OS} drift is typically 1 μV/°C and bias current drift is typically 9 nA/°C.
5. The AD844 exhibits excellent differential gain and differential phase characteristics, making it suitable for a variety of video applications with bandwidths up to 60 MHz.
6. The AD844 combines low distortion, low noise and low drift with wide bandwidth, making it outstanding as an input amplifier for flash A/D converters.

REV. C

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703

AD844—SPECIFICATIONS (@ T_A = +25°C and V_S = ±15 V dc, unless otherwise noted)

Model	Conditions	AD844J/A Min	AD844J/A Typ	AD844J/A Max	AD844B Min	AD844B Typ	AD844B Max	AD844S Min	AD844S Typ	AD844S Max	Units
INPUT OFFSET VOLTAGE[1]			50	300		50	150		50	300	μV
T_{MIN}–T_{MAX}			75	500		75	200		125	500	μV
vs. Temperature			1			1	5		1	5	μV/°C
vs. Supply	5 V–18 V										
Initial			4	20		4	10		4	20	μV/V
T_{MIN}–T_{MAX}			4			4	10		4	20	μV/V
vs. Common Mode	V_{CM} = ±10 V										
Initial			10	35		10	20		10	35	μV/V
T_{MIN}–T_{MAX}			10			10	20		10	35	μV/V
INPUT BIAS CURRENT											
–Input Bias Current[1]			200	450		150	250		200	450	nA
T_{MIN}–T_{MAX}			800	1500		750	1100		1900	2500	nA
vs. Temperature			9			9	15		20	30	nA/°C
vs. Supply	5 V–18 V										
Initial			175	250		175	200		175	250	nA/V
T_{MIN}–T_{MAX}			220			220	240		220	300	nA/V
vs. Common Mode	V_{CM} = ±10 V										
Initial			90	160		90	110		90	160	nA/V
T_{MIN}–T_{MAX}			110			110	150		120	200	nA/V
+Input Bias Current[1]			150	400		100	200		100	400	nA
T_{MIN}–T_{MAX}			350	700		300	500		800	1300	nA
vs. Temperature			3			3	7		7	15	nA/°C
vs. Supply	5 V–18 V										
Initial			80	150		80	100		80	150	nA/V
T_{MIN}–T_{MAX}			100			100	120		120	200	nA/V
vs. Common Mode	V_{CM} = ±10 V										
Initial			90	150		90	120		90	150	nA/V
T_{MIN}–T_{MAX}			130			130	190		140	200	nA/V
INPUT CHARACTERISTICS											
Input Resistance											
–Input			50	65		50	65		50	65	Ω
+Input		7	10		7	10		7	10		MΩ
Input Capacitance											
–Input			2			2			2		pF
+Input			2			2			2		pF
Input Voltage Range											
Common Mode		±10			±10			±10			V
INPUT VOLTAGE NOISE	f ≥ 1 kHz		2			2			2		nV/√Hz
INPUT CURRENT NOISE											
–Input	f ≥ 1 kHz		10			10			10		pA/√Hz
+Input	f ≥ 1 kHz		12			12			12		pA/√Hz
OPEN LOOP TRANSRESISTANCE	V_{OUT} = ±10 V										
	R_{LOAD} = 500 Ω	2.2	3.0		2.8	3.0		2.2	3.0		MΩ
T_{MIN}–T_{MAX}		1.3	2.0		1.6	2.0		1.3	1.6		MΩ
Transcapacitance			4.5			4.5			4.5		pF
DIFFERENTIAL GAIN ERROR[2]	f = 4.4 MHz		0.03			0.03			0.03		%
DIFFERENTIAL PHASE ERROR[2]	f = 4.4 MHz		0.15			0.15			0.15		Degree
FREQUENCY RESPONSE											
Small Signal Bandwidth											
[3]Gain = –1			60			60			60		MHz
[4]Gain = –10			33			33			33		MHz
TOTAL HARMOMIC DISTORTION	f = 100 kHz, 2 V rms[5]		0.005			0.005			0.005		%
SETTLING TIME											
10 V Output Step	±15 V Supplies										
Gain = –1, to 0.1%[5]			100			100			100		ns
Gain = –10, to 0.1%[6]			100			100			100		ns
2 V Output Step	±5 V Supplies										
Gain = –1, to 0.1%[5]			110			110			110		ns
Gain = –10, to 0.1%[6]			100			100			100		ns

Model	Conditions	AD844J/A Min	AD844J/A Typ	AD844J/A Max	AD844B Min	AD844B Typ	AD844B Max	AD844S Min	AD844S Typ	AD844S Max	Units
OUTPUT SLEW RATE	Overdriven Input	1200	2000		1200	2000		1200	2000		V/μs
FULL POWER BANDWIDTH											
V_{OUT} = 20 V p-p[5]	V_S = ±15 V		20			20			20		MHz
V_{OUT} = 2 V p-p[5]	V_S = ±5 V THD = 3%		20			20			20		MHz
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD} = 500 Ω	**10**	11		**10**	11		**10**	11		±V
Short Circuit Current			80			80			80		mA
T_{MIN}–T_{MAX}			60			60			60		mA
Output Resistance	Open Loop		15			15			15		Ω
POWER SUPPLY											
Operating Range		±4.5		±18	±4.5		±18	+4.5		±18	V
Quiescent Current			6.5	7.5		6.5	7.5		6.5	7.5	mA
T_{MIN}–T_{MAX}			7.5	8.5		7.5	8.5		8.5	9.5	mA

NOTES
[1]Rated performance after a 5 minute warmup at T_A = 25°C.
[2]Input signal 285 mV p-p carrier (40 IRE) riding on 0 mV to 642 mV (90 IRE) ramp. R_L= 100 Ω; R1, R2 = 300 Ω.
[3]Input signal 0 dBm, C_L = 10 pF, R_L = 500 Ω, R1 = 500 Ω, R2 = 500 Ω in Figure 26.
[4]Input signal 0 dBm, C_L =10 pF, R_L = 500 Ω, R1 = 500 Ω, R2 = 50 Ω in Figure 26.
[5]C_L = 10 pF, R_L = 500 Ω, R1 = 1 kΩ, R2 = 1 kΩ in Figure 26.
[6]C_L = 10 pF, R_L = 500 Ω, R1 = 500 Ω, R2 = 50 Ω in Figure 26.

Specifications subject to change without notice. All min and max specifications are guaranteed.
Specifications shown in **boldface** are tested on all production units at final electrical test.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ..... ±18 V
Power Dissipation[2] ..... 1.1 W
Output Short Circuit Duration ..... Indefinite
Common-Mode Input Voltage ..... $\pm V_S$
Differential Input Voltage ..... 6 V
Inverting Input Current
  Continuous ..... 5 mA
  Transient ..... 10 mA
Storage Temperature Range (Q) .....–65°C to +150°C
  (N, R) .....–65°C to +125°C
Lead Temperature Range (Soldering 60 sec) ..... +300°C
ESD Rating ..... 1000 V

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]28-Pin Plastic Package: θ_{JA} = 100°C/Watt
8-Pin Cerdip Package: θ_{JA} = 110°C/Watt
16-Pin SOIC Package: θ_{JA} = 100°C/Watt

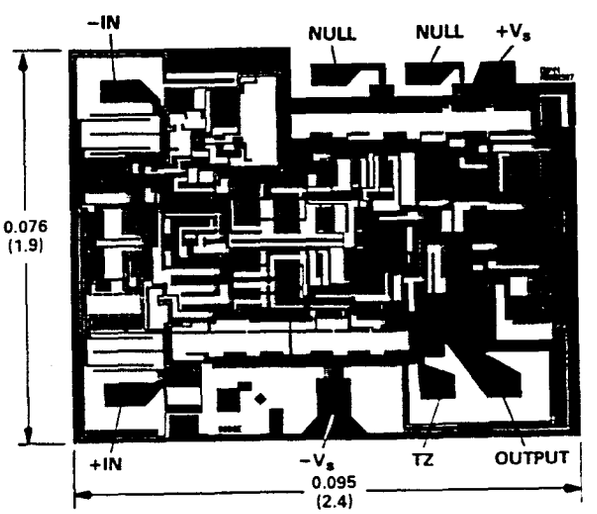
ORDERING GUIDE

Model	Temperature Range	Package Option*
AD844JR	0°C to +70°C	R-16
AD844JR-REEL	0°C to +70°C	Tape and Reel
AD844AN	–40°C to +85°C	N-8
AD844AQ	–40°C to +85°C	Q-8
AD844BQ	–40°C to +85°C	Q-8
AD844SQ	–55°C to +125°C	Q-8
AD844SQ/883B	–55°C to +125°C	Q-8
5962-8964401PA	–55°C to +125°C	Q-8
AD844A Chips	–40°C to +85°C	Die
AD844S Chips	–55°C to +125°C	Die

*N = Plastic DIP; Q = Cerdip; R = Small Outline IC (SOIC).

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimension shown in inches and (mm).



SUBTRATE CONNECTED TO $+V_S$

AD844–Typical Characteristics (T_A = +25°C and V_S = ±15 V, unless otherwise noted)

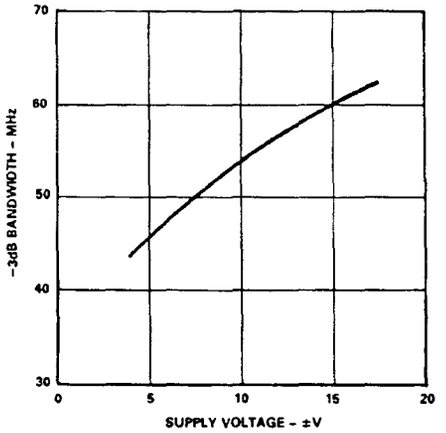


Figure 1. –3 dB Bandwidth vs. Supply Voltage R1 = R2 = 500Ω

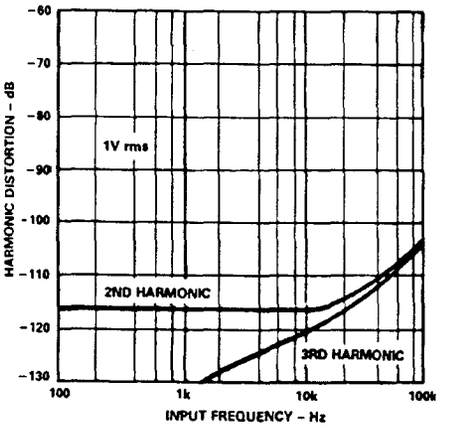


Figure 2. Harmonic Distortion vs. Frequency, R1 = R2 = 1 kΩ

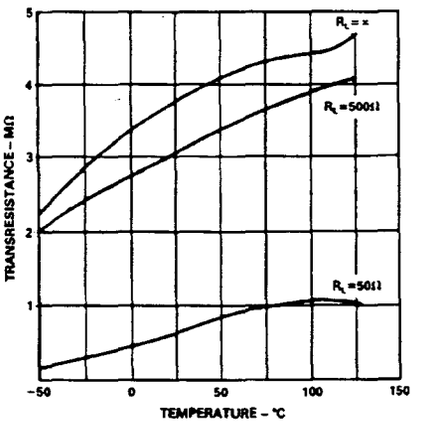


Figure 3. Transresistance vs. Temperature

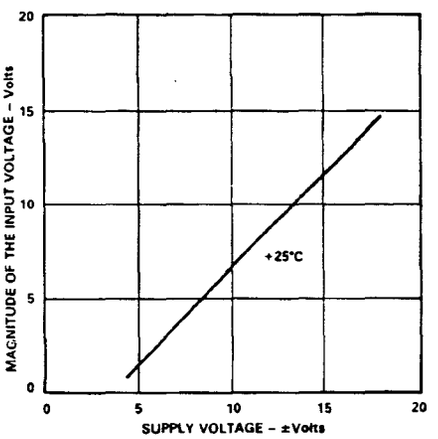


Figure 4. Noninverting Input Voltage Swing vs. Supply Voltage

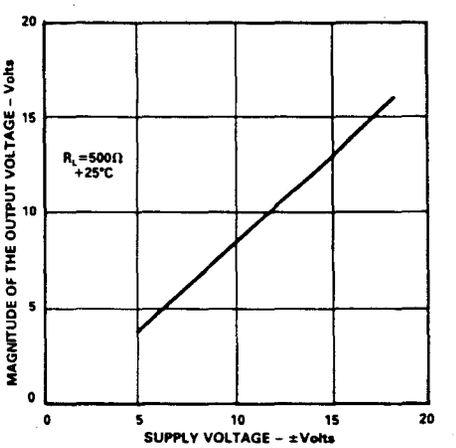


Figure 5. Output Voltage Swing vs. Supply Voltage

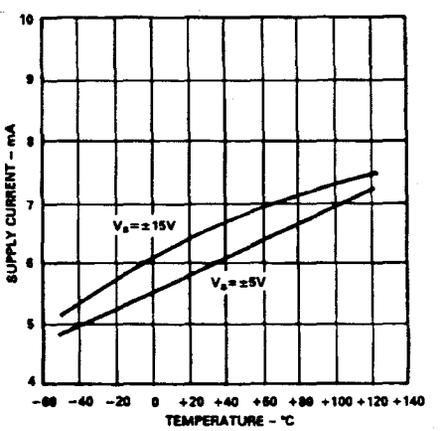


Figure 6. Quiescent Supply Current vs. Temperature and Supply Voltage

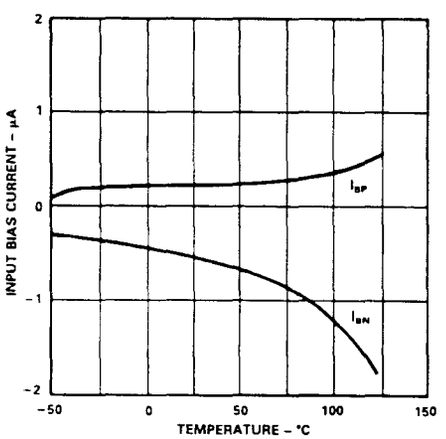


Figure 7. Inverting Input Bias Current (I_{BN}) and Noninverting Input Bias Current (I_{BP}) vs. Temperature

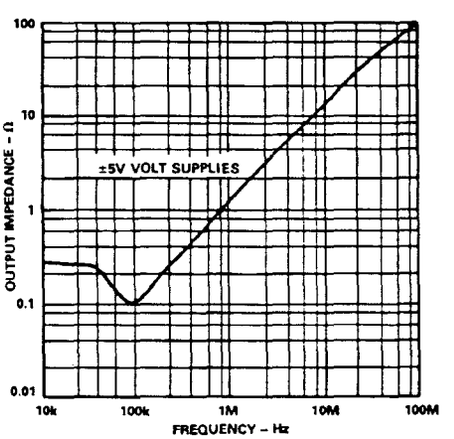


Figure 8. Output Impedance vs. Frequency, Gain = –1, R1 = R2 = 1 kΩ

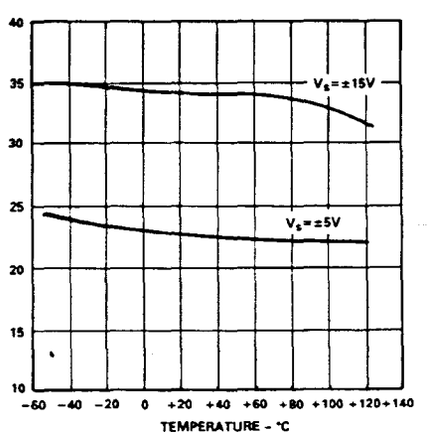


Figure 9. –3 dB Bandwidth vs. Temperature, Gain = –1, R1 = R2 = 1 kΩ

Inverting Gain of 1 AC Characteristics

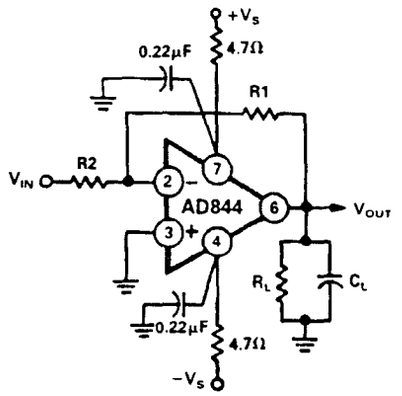


Figure 10. Inverting Amplifier, Gain of −1 (R1 = R2)

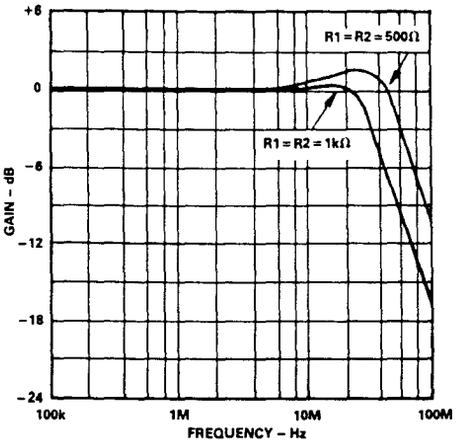


Figure 11. Gain vs. Frequency for Gain = −1, R_L = 500Ω, C_L = 0 pF

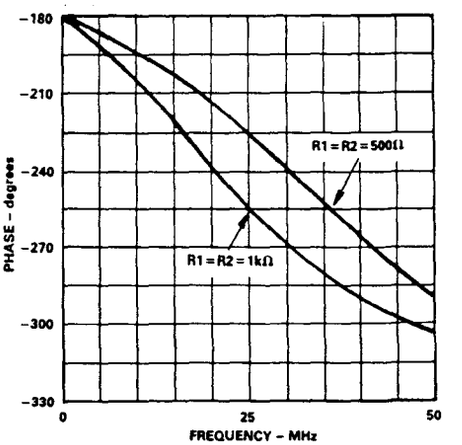


Figure 12. Phase vs. Frequency Gain = −1, R_L = 500Ω, C_L = 0 pF

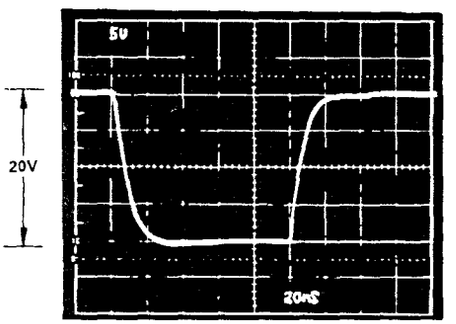


Figure 13. Large Signal Pulse Response, Gain = −1, R1 = R2 = 1 kΩ

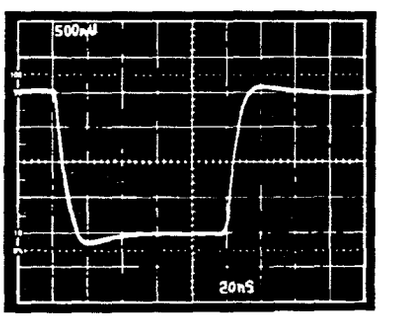


Figure 14. Small Signal Pulse Response, Gain = −1, R1 = R2 = 1 kΩ

Inverting Gain of 10 AC Characteristics

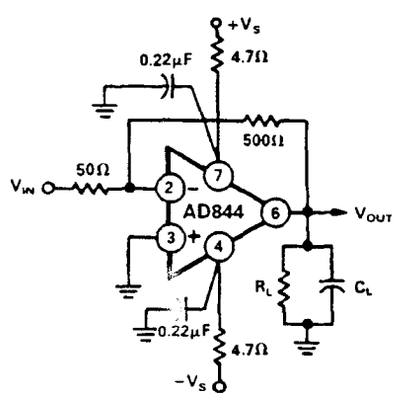


Figure 15. Gain of −10 Amplifier

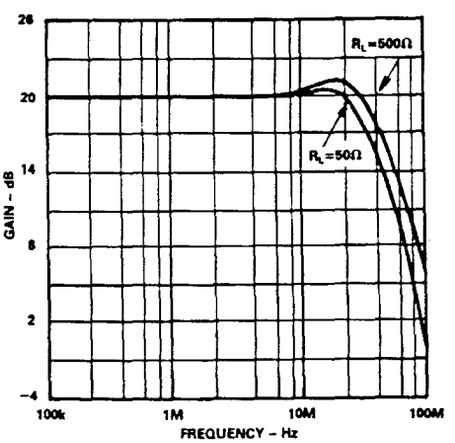


Figure 16. Gain vs. Frequency, Gain = −10

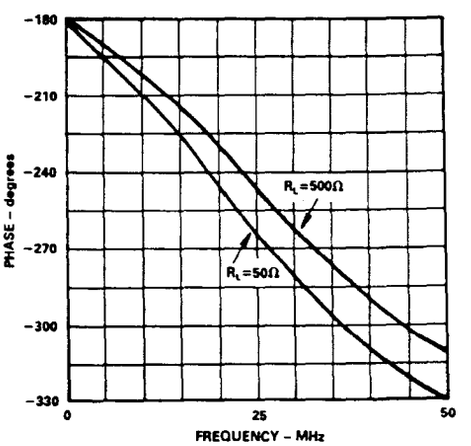


Figure 17. Phase vs. Frequency, Gain = −10

Inverting Gain of 10 Pulse Response

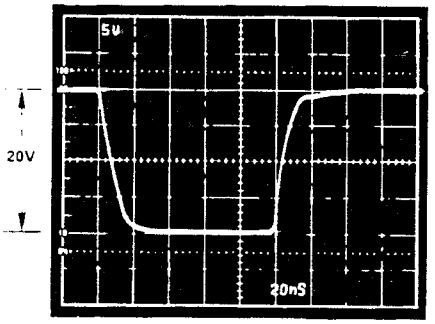


Figure 18. Large Signal Pulse Response, Gain = −10, R_L = 500Ω

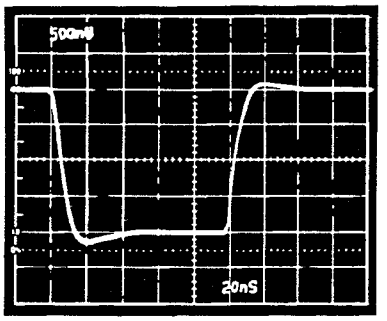


Figure 19. Small Signal Pulse Response, Gain = −10, R_L = 500Ω

Noninverting Gain of 10 AC Characteristics

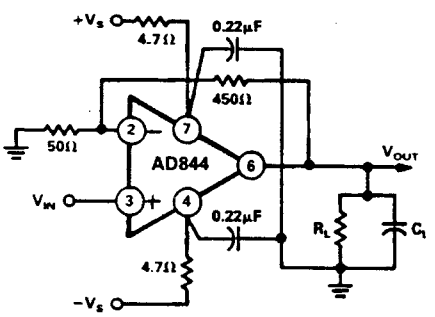


Figure 20. Noninverting Gain of +10 Amplifier

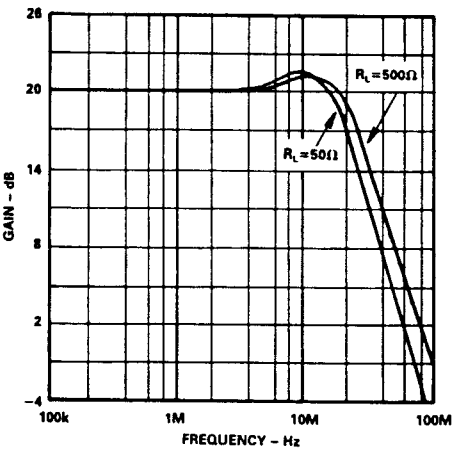


Figure 21. Gain vs. Frequency, Gain = +10

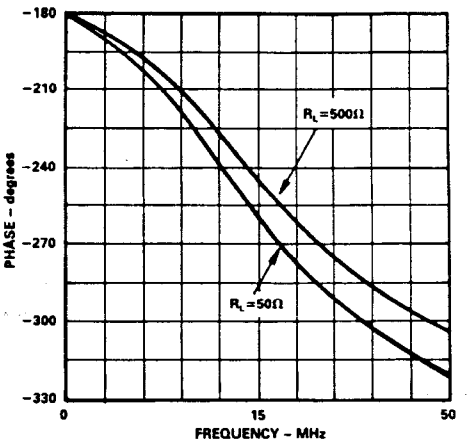


Figure 22. Phase vs. Frequency, Gain = +10

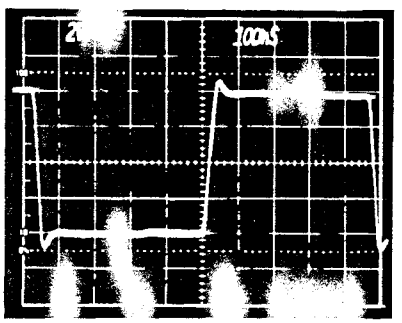


Figure 23. Noninverting Amplifier Large Signal Pulse Response, Gain = +10, R_L = 500Ω

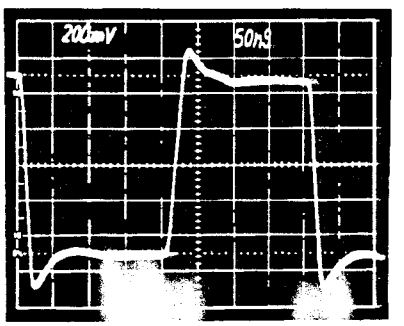


Figure 24. Small Signal Pulse Response, Gain = +10, R_L = 500Ω

UNDERSTANDING THE AD844

The AD844 can be used in ways similar to a conventional op amp while providing performance advantages in wideband applications. However, there are important differences in the internal structure which need to be understood in order to optimize the performance of the AD844 op amp.

Open Loop Behavior

Figure 25 shows a current feedback amplifier reduced to essentials. Sources of fixed dc errors such as the inverting node bias current and the offset voltage are excluded from this model and are discussed later. The most important parameter limiting the dc gain is the transresistance, Rt, which is ideally infinite. A finite value of Rt is analogous to the finite open loop voltage gain in a conventional op amp.

The current applied to the inverting input node is replicated by the current conveyor so as to flow in resistor Rt. The voltage developed across Rt is buffered by the unity gain voltage follower. Voltage gain is the ratio Rt/ R_{IN}. With typical values of Rt = 3 MΩ and R_{IN} = 50 Ω, the voltage gain is about 60,000. The open loop current gain is another measure of gain and is determined by the beta product of the transistors in the voltage follower stage (see Figure 28); it is typically 40,000.

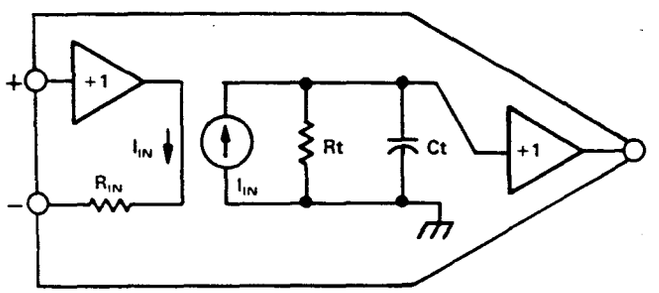


Figure 25. Equivalent Schematic

The important parameters defining ac behavior are the transcapacitance, Ct, and the external feedback resistor (not shown). The time constant formed by these components is analogous to the dominant pole of a conventional op amp, and thus cannot be reduced below a critical value if the closed loop system is to be stable. In practice, Ct is held to as low a value as possible (typically 4.5 pF) so that the feedback resistor can be maximized while maintaining a fast response. The finite R_{IN} also affects the closed loop response in some applications as will be shown.

The open loop ac gain is also best understood in terms of the transimpedance rather than as an open loop voltage gain. The open loop pole is formed by Rt in parallel with Ct. Since Ct is typically 4.5 pF, the open loop corner frequency occurs at about 12 kHz. However, this parameter is of little value in determining the closed loop response.

Response as an Inverting Amplifier

Figure 26 shows the connections for an inverting amplifier. Unlike a conventional amplifier the transient response and the small signal bandwidth are determined primarily by the value of the external feedback resistor, R1, rather than by the ratio of R1/R2 as is customarily the case in an op amp application. This is a direct result of the low impedance at the inverting input. As with conventional op amps, the closed loop gain is −R1/R2.

The closed loop transresistance is simply the parallel sum of R1 and Rt. Since R1 will generally be in the range 500 Ω to 2 kΩ and Rt is about 3 MΩ the closed loop transresistance will be only 0.02% to 0.07% lower than R1. This small error will often be less than the resistor tolerance.

When R1 is fairly large (above 5 kΩ) but still much less than Rt, the closed loop HF response is dominated by the time constant R1Ct. Under such conditions the AD844 is over-damped and will provide only a fraction of its bandwidth potential. Because of the absence of slew rate limitations under these conditions, the circuit will exhibit a simple single pole response even under large signal conditions.

In Figure 26, R3 is used to properly terminate the input if desired. R3 in parallel with R2 gives the terminated resistance. As R1 is lowered, the signal bandwidth increases, but the time constant R1Ct becomes comparable to higher order poles in the closed loop response. Therefore, the closed loop response becomes complex, and the pulse response shows overshoot. When R2 is much larger than the input resistance, R_{IN}, at Pin 2, most of the feedback current in R1 is delivered to this input; but as R2 becomes comparable to R_{IN}, less of the feedback is absorbed at Pin 2, resulting in a more heavily damped response. Consequently, for low values of R2 it is possible to lower R1 without causing instability in the closed loop response. Table I lists combinations of R1 and R2 and the resulting frequency response for the circuit of Figure 26. Figure 13 shows the very clean and fast ±10 V pulse response of the AD844.

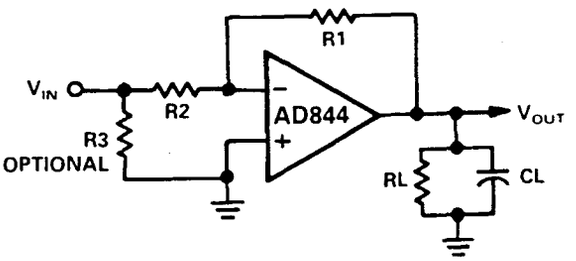


Figure 26. Inverting Amplifier

Table I.

Gain	R1	R2	BW (MHz)	GBW (MHz)
−1	1 kΩ	1 kΩ	35	35
−1	500 Ω	500 Ω	60	60
−2	2 kΩ	1 kΩ	15	30
−2	1 kΩ	500 Ω	30	60
−5	5 kΩ	1 kΩ	5.2	26
−5	500 Ω	100 Ω	49	245
−10	1 kΩ	100 Ω	23	230
−10	500 Ω	50 Ω	33	330
−20	1 kΩ	50 Ω	21	420
−100	5 kΩ	50 Ω	3.2	320
+100	5 kΩ	50 Ω	9	900

Response as an I-V Converter

The AD844 works well as the active element in an operational current to voltage converter, used in conjunction with an external scaling resistor, R1, in Figure 27. This analysis includes the stray capacitance, C_S, of the current source, which might be a high speed DAC. Using a conventional op amp, this capacitance forms a "nuisance pole" with R1 which destabilizes the closed loop response of the system. Most op amps are internally compensated for the fastest response at unity gain, so the pole due to R1 and C_S reduces the already narrow phase margin of the system. For example, if R1 were 2.5 kΩ a C_S of 15 pF would place this pole at a frequency of about 4 MHz, well within the response range of even a medium speed operational amplifier. In a current feedback amp this nuisance pole is no longer determined by R1 but by the input resistance, R_{IN}. Since this is about 50 Ω for the AD844, the same 15 pF forms a pole 212 MHz and causes little trouble. It can be shown that the response of this system is:

$$V_{OUT} = -Isig\frac{K\,R1}{(1+sTd)(1+sTn)}$$

where K is a factor very close to unity and represents the finite dc gain of the amplifier, Td is the dominant pole and Tn is the nuisance pole:

$$K = \frac{Rt}{Rt + R1}$$

$$Td = KR1Ct$$

$$Tn = R_{IN}C_S \qquad (assuming\ R_{IN} << R1)$$

Using typical values of R1 = 1 kΩ and Rt = 3 MΩ, K is 0.9997; in other words, the "gain error" is only 0.03%. This is much less than the scaling error of virtually all DACs and can be absorbed, if necessary, by the trim needed in a precise system.

In the AD844, Rt is fairly stable with temperature and supply voltages, and consequently the effect of finite "gain" is negligible unless high value feedback resistors are used. Since that would result in slower response times than are possible, the relatively low value of Rt in the AD844 will rarely be a significant source of error.

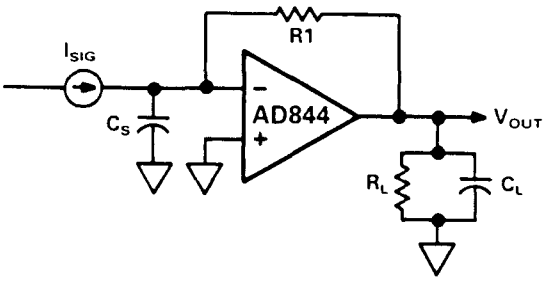


Figure 27. Current to Voltage Converter

Circuit Description of the AD844

A simplified schematic is shown in Figure 28. The AD844 differs from a conventional op amp in that the signal inputs have radically different impedance. The noninverting input (Pin 3) presents the usual high impedance. The voltage on this input is transferred to the inverting input (Pin 2) with a low offset voltage, ensured by the close matching of like polarity transistors operating under essentially identical bias conditions. Laser trimming nulls the residual offset voltage, down to a few tens of microvolts. The inverting input is the common emitter node of a complementary pair of grounded base stages and behaves as a current summing node. In an ideal current feedback op amp the input resistance would be zero. In the AD844 it is about 50 Ω.

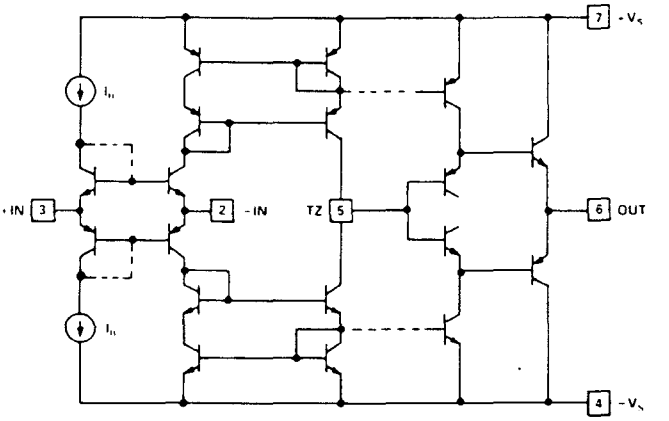


Figure 28. Simplified Schematic

A current applied to the inverting input is transferred to a complementary pair of unity-gain current mirrors which deliver the same current to an internal node (Pin 5) at which the full output voltage is generated. The unity-gain complementary voltage follower then buffers this voltage and provides the load driving power. This buffer is designed to drive low impedance loads such as terminated cables, and can deliver ±50 mA into a 50 Ω load while maintaining low distortion, even when operating at supply voltages of only ±6 V. Current limiting (not shown) ensures safe operation under short circuited conditions.

It is important to understand that the low input impedance at the inverting input is locally generated, and does not depend on feedback. This is very different from the "virtual ground" of a conventional operational amplifier used in the current summing mode which is essentially an open circuit until the loop settles. In the AD844, transient current at the input does not cause voltage spikes at the summing node while the amplifier is settling. Furthermore, all of the transient current is delivered to the slewing (TZ) node (Pin 5) via a short signal path (the grounded base stages and the wideband current mirrors).

The current available to charge the capacitance (about 4.5 pF) at TZ node, is *always proportional to the input error current,* and the slew rate limitations associated with the large signal response of op amps do not occur. For this reason, the rise and fall times are almost independent of signal level. In practice, the input current will eventually cause the mirrors to saturate. When using ±15 V supplies, this occurs at about 10 mA (or ±2200 V/μs). Since signal currents are rarely this large, classical "slew rate" limitations are absent.

This inherent advantage would be lost if the voltage follower used to buffer the output were to have slew rate limitations. The AD844 has been designed to avoid this problem, and as a result the output buffer exhibits a clean large signal transient response, free from anomalous effects arising from internal saturation.

Response as a Noninverting Amplifier

Since current feedback amplifiers are asymmetrical with regard to their two inputs, performance will differ markedly in noninverting and inverting modes. In noninverting modes, the large signal high speed behavior of the AD844 deteriorates at low gains because the biasing circuitry for the input system (not shown in Figure 28) is not designed to provide high input voltage slew rates.

However, good results can be obtained with some care. The noninverting input will not tolerate a large transient input; it must be kept below ±1 V for best results. Consequently this mode is better suited to high gain applications (greater than ×10). Figure 20 shows a noninverting amplifier with a gain of 10 and a bandwidth of 30 MHz. The transient response is shown in Figures 23 and 24. To increase the bandwidth at higher gains, a capacitor can be added across R2 whose value is approximately the ratio of R1 and R2 times Ct.

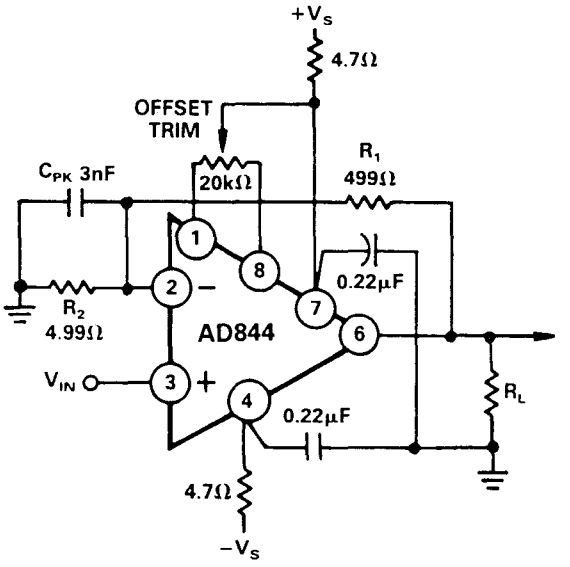


Figure 29. Noninverting Amplifier Gain = 100, Optional Offset Trim Is Shown

Noninverting Gain of 100

The AD844 provides very clean pulse response at high noninverting gains. Figure 29 shows a typical configuration providing a gain of 100 with high input resistance. The feedback resistor is kept as low as practicable to maximize bandwidth, and a peaking capacitor (C_{PK}) can optionally be added to further extend the bandwidth. Figure 30 shows the small signal response with C_{PK} = 3 nF, R_L = 500 Ω and supply voltages of either ±5 V or ±15 V. *Gain bandwidth products of up to 900 MHz can be achieved in this way.*

The offset voltage of the AD844 is laser trimmed to the 50 μV level and exhibits very low drift. In practice, there is an additional offset term due to the bias current at the inverting input (I_{BN}) which flows in the feedback resistor (R1). This can optionally be nulled by the trimming potentiometer shown in Figure 29.

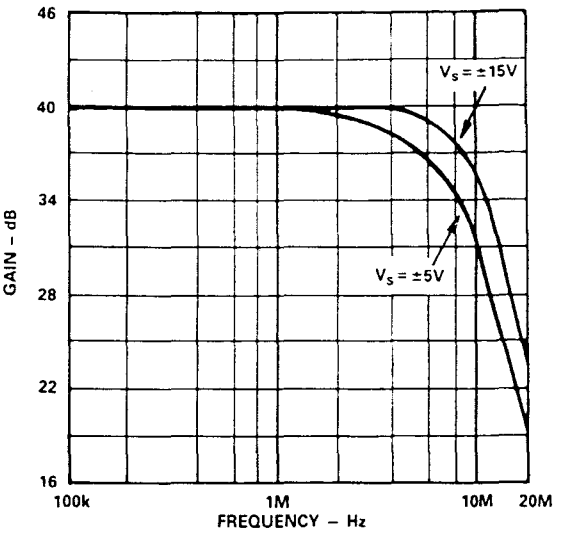


Figure 30. AC Response for Gain = 100, Configuration Shown in Figure 29

USING THE AD844

Board Layout

As with all high frequency circuits considerable care must be used in the layout of the components surrounding the AD844. A ground plane, to which the power supply decoupling capacitors are connected by the shortest possible leads, is essential to achieving clean pulse response. Even a continuous ground plane will exhibit finite voltage drops between points on the plane, and this must be kept in mind in selecting the grounding points. Generally speaking, decoupling capacitors should be taken to a point close to the load (or output connector) since the load currents flow in these capacitors at high frequencies. The +In and –In circuits (for example, a termination resistor and Pin 3) must be taken to a common point on the ground plane close to the amplifier package.

Use low impedance capacitors (AVX SR305C224KAA or equivalent) of 0.22 μF wherever ac coupling is required. Include either ferrite beads and/or a small series resistance (approximately 4.7 Ω) in each supply line.

Input Impedance

At low frequencies, negative feedback keeps the resistance at the inverting input close to zero. As the frequency increases, the impedance looking into this input will increase from near zero to the open loop input resistance, due to bandwidth limitations, making the input seem inductive. If it is desired to keep the input impedance flatter, a series RC network can be inserted across the input. The resistor is chosen so that the parallel sum of it and R2 equals the desired termination resistance. The capacitance is set so that the pole determined by this RC network is about half the bandwidth of the op amp. This network is not important if the input resistor is much larger than the termination used, or if frequencies are relatively low. In some cases, the small peaking that occurs without the network can be of use in extending the –3 dB bandwidth.

Driving Large Capacitive Loads

Capacitive drive capability is 100 pF without an external network. With the addition of the network shown in Figure 31, the capacitive drive can be extended to over 10,000 pF, limited by internal power dissipation. With capacitive loads, the output speed becomes a function of the overdriven output current limit. Since this is roughly ±100 mA, under these conditions, the maximum slew rate into a 1000 pF load is ±100 V/μs. Figure 32 shows the transient response of an inverting amplifier (R1 = R2 = 1 kΩ) using the feed forward network shown in Figure 31, driving a load of 1000 pF.

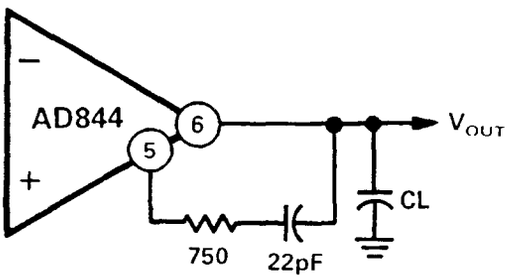


Figure 31. Feed Forward Network for Large Capacitive Loads

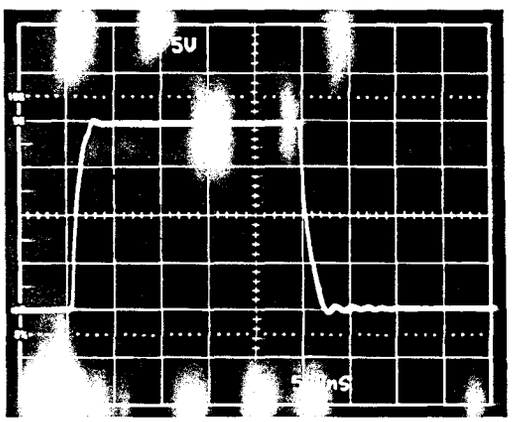


Figure 32. Driving 1000 pF C_L with Feed Forward Network of Figure 31

Settling Time

Settling time is measured with the circuit of Figure 33. This circuit employs a false summing node, clamped by the two Schottky diodes, to create the error signal and limit the input signal to the oscilloscope. For measuring settling time, the ratio of R6/R5 is equal to R1/R2. For unity gain, R6 = R5 = 1 kΩ, and R_L = 500 Ω. For the gain of –10, R5 = 50 Ω, R6 = 500 Ω and R_L was not used since the summing network loads the output with approximately 275 Ω. Using this network in a unity-gain configuration, settling time is 100 ns to 0.1% for a –5 V to +5 V step with C_L = 10 pF.

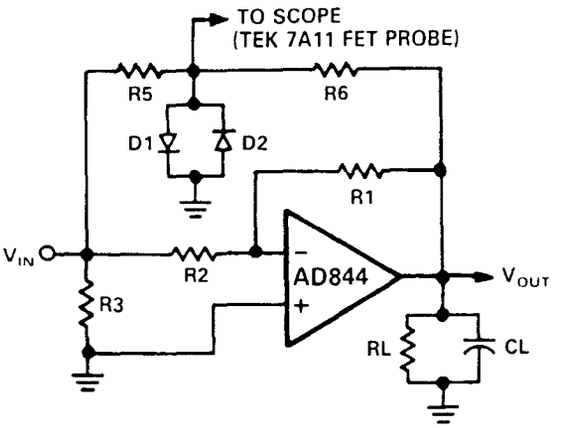


Figure 33. Settling Time Test Fixture

DC Error Calculation

Figure 34 shows a model of the dc error and noise sources for the AD844. The inverting input bias current, I_{BN}, flows in the feedback resistor. I_{BP}, the noninverting input bias current, flows in the resistance at Pin 3 (R_P), and the resulting voltage (plus any offset voltage) will appear at the inverting input. The total error, V_O, at the output is:

$$V_O = (I_{BP}\ R_P + V_{OS} + I_{BN}\ R_{IN})\left(1+\frac{R1}{R2}\right) + I_{BN}\ R1$$

Since I_{BN} and I_{BP} are unrelated both in sign and magnitude, inserting a resistor in series with the noninverting input will not necessarily reduce dc error and may actually increase it.

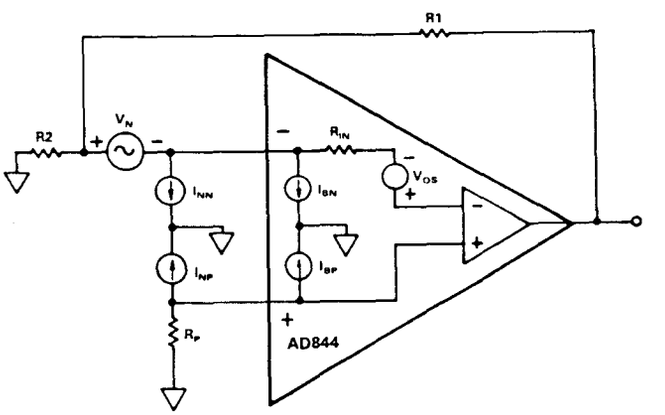


Figure 34. Offset Voltage and Noise Model for the AD844

Noise

Noise sources can be modeled in a manner similar to the dc bias currents, but the noise sources are Inn, Inp, Vn, and the amplifier induced noise at the output, V_{ON}, is:

$$V_{ON} = \sqrt{((Inp\ R_P)^2 + Vn^2)\left(1+\frac{R1}{R2}\right)^2 + (Inn\ R1)^2}$$

Overall noise can be reduced by keeping all resistor values to a minimum. With typical numbers, R1 = R2 = 1k, R_P = 0, Vn = 2 nV/$\sqrt{Hz}$, Inp = 10 pA/$\sqrt{Hz}$, Inn = 12 pA/$\sqrt{Hz}$, V_{ON} calculates to 12 nV/$\sqrt{Hz}$. The current noise is dominant in this case, as it will be in most low gain applications.

Video Cable Driver Using ±5 Volt Supplies

The AD844 can be used to drive low impedance cables. Using ±5 V supplies, a 100 Ω load can be driven to ±2.5 V with low distortion. Figure 35a shows an illustrative application which provides a noninverting gain of 2, allowing the cable to be reverse-terminated while delivering an overall gain of +1 to the load. The –3 dB bandwidth of this circuit is typically 30 MHz. Figure 35b shows a differential gain and phase test setup. In video applications, differential-phase and differential-gain characteristics are often important. Figure 35c shows the variation in phase as the load voltage varies. Figure 35d shows the gain variation.

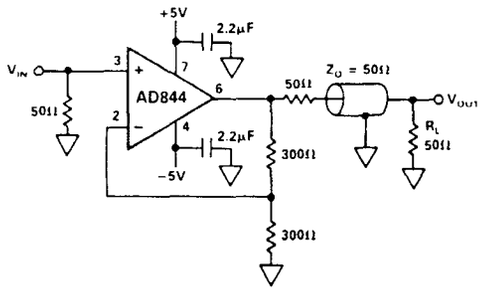


Figure 35a. The AD844 as a Cable Driver

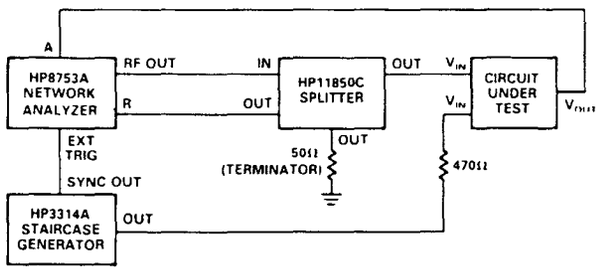


Figure 35b. Differential Gain/Phase Test Setup

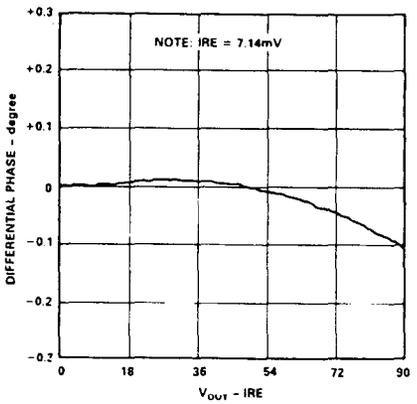


Figure 35c. Differential Phase for the Circuit of Figure 35a

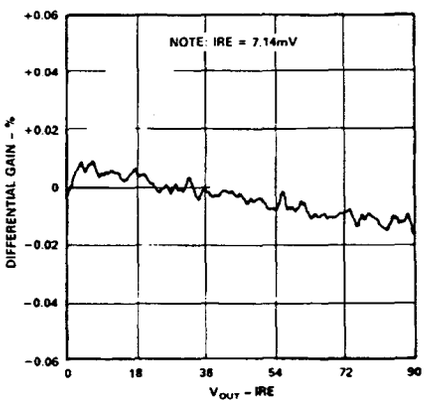


Figure 35d. Differential Gain for the Circuit of Figure 35a

High Speed DAC Buffer

The AD844 performs very well in applications requiring current-to-voltage conversion. Figure 36 shows connections for use with the AD568 current output DAC. In this application the bipolar offset is used so that the full-scale current is ±5.12 mA, which generates an output of ±5.12 V using the 1 kΩ application resistor on the AD568. Figure 37 shows the full-scale transient response. Care is needed in power supply decoupling and grounding techniques to achieve the full 12-bit accuracy and realize the fast settling capabilities of the system. The unmarked capacitors in this figure are 0.1 μF ceramic (for example, AVX Type SR305C104KAA), and the ferrite inductors should be about 2.5 μH (for example, Fair-Rite Type 2743002122). The AD568 data sheet should be consulted for more complete details about its use.

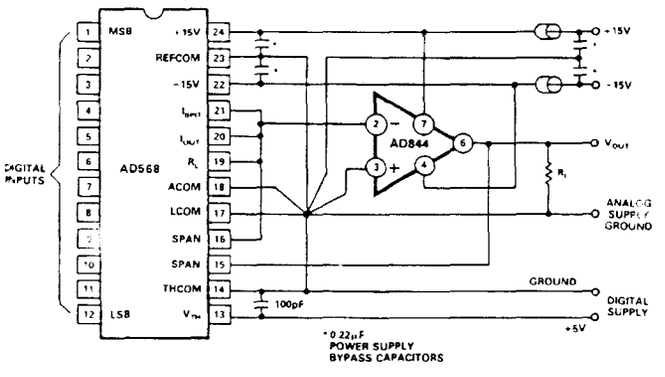


Figure 36. High Speed DAC Amplifier

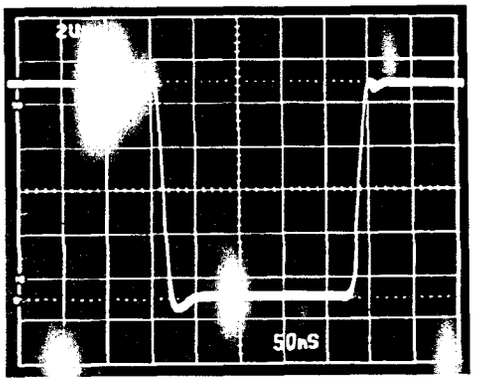


Figure 37. DAC Amplifier Full-Scale Transient Response

20 MHz Variable Gain Amplifier

The AD844 is an excellent choice as an output amplifier for the AD539 multiplier, in all of its connection modes. (See AD539 data sheet for full details.) Figure 38 shows a simple multiplier providing the output:

$$V_W = -\frac{V_X V_Y}{2V}$$

where V_X is the "gain control" input, a positive voltage of from 0 V to +3.2 V (max) and V_Y is the "signal voltage", nominally ±2 V FS but capable of operation up to ±4.2 V. The peak output in this configuration is thus ±6.7 V. Using all four of the internal application resistors provided on the AD539 in parallel results in a feedback resistance of 1.5 kΩ, at which value the bandwidth of the AD844 is about 22 MHz, and is essentially independent of V_X. The gain at V_X = 3.16 V is +4 dB.

Figure 39 shows the small signal response for a 50 dB gain control range (V_X = +10 mV to +3.16 V). At small values of V_X, capacitive feedthrough on the PC board becomes troublesome, and very careful layout techniques are needed to minimize this problem. A ground strip between the pins of the AD539 will be helpful in this regard. Figure 40 shows the response to a 2 V pulse on V_Y for V_X = +1 V, +2 V and +3 V. For these results, a load resistor of 500 Ω was used and the supplies were ±9 V. The multiplier will operate from supplies between ±4.5 V and ±16.5 V.

Disconnecting Pins 9 and 16 on the AD539 alters the denominator in the above expression to 1 V, and the bandwidth will be approximately 10 MHz, with a maximum gain of 10 dB. Using only Pin 9 or Pin 16 results in a denominator of 0.5 V, a bandwidth of 5 MHz and a maximum gain of 16 dB.

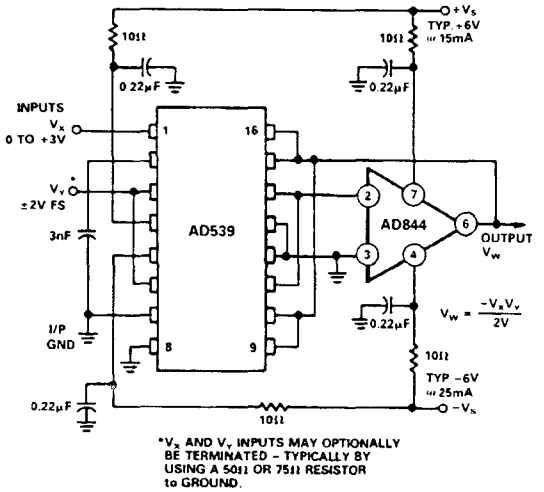


Figure 38. 20 MHz VGA Using the AD539

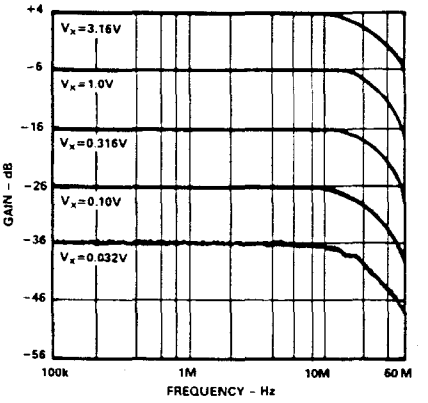


Figure 39. VGA AC Response

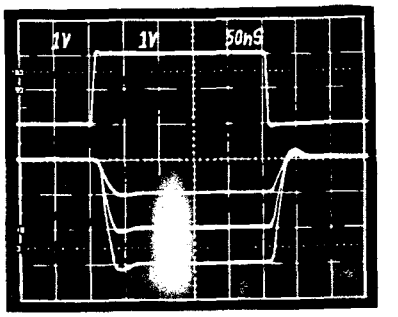
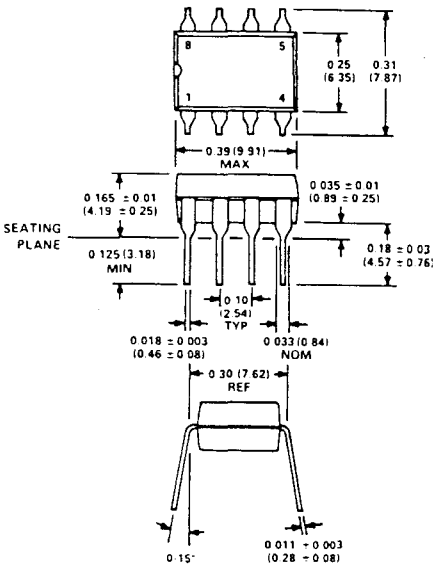


Figure 40. VGA Transient Response with V_X = 1 V, 2 V, and 3 V

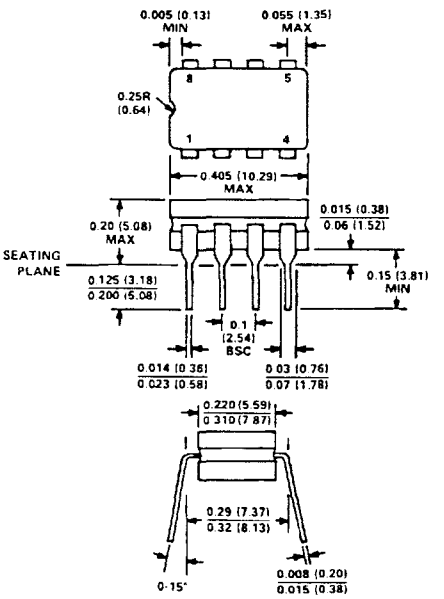
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

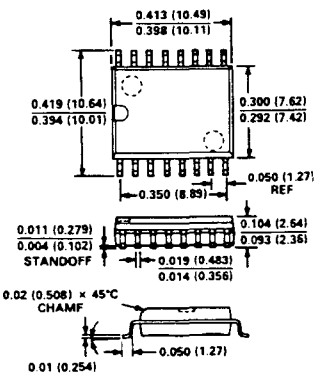
Mini-DIP (N) Package



Cerdip (Q) Package



16-Pin SOIC (R) Package



September 1998 File Number 957.4

4.5MHz, BiMOS Operational Amplifier with MOSFET Input/Bipolar Output

The CA3140A and CA3140 are integrated circuit operational amplifiers that combine the advantages of high voltage PMOS transistors with high voltage bipolar transistors on a single monolithic chip.

The CA3140A and CA3140 BiMOS operational amplifiers feature gate protected MOSFET (PMOS) transistors in the input circuit to provide very high input impedance, very low input current, and high speed performance. The CA3140A and CA3140 operate at supply voltage from 4V to 36V (either single or dual supply). These operational amplifiers are internally phase compensated to achieve stable operation in unity gain follower operation, and additionally, have access terminal for a supplementary external capacitor if additional frequency roll-off is desired. Terminals are also provided for use in applications requiring input offset voltage nulling. The use of PMOS field effect transistors in the input stage results in common mode input voltage capability down to 0.5V below the negative supply terminal, an important attribute for single supply applications. The output stage uses bipolar transistors and includes built-in protection against damage from load terminal short circuiting to either supply rail or to ground.

The CA3140 Series has the same 8-lead pinout used for the "741" and other industry standard op amps. The CA3140A and CA3140 are intended for operation at supply voltages up to 36V (±18V).

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
CA3140AE	-55 to 125	8 Ld PDIP	E8.3
CA3140AM (3140A)	-55 to 125	8 Ld SOIC	M8.15
CA3140AS	-55 to 125	8 Pin Metal Can	T8.C
CA3140AT	-55 to 125	8 Pin Metal Can	T8.C
CA3140E	-55 to 125	8 Ld PDIP	E8.3
CA3140M (3140)	-55 to 125	8 Ld SOIC	M8.15
CA3140M96 (3140)	-55 to 125	8 Ld SOIC Tape and Reel	
CA3140T	-55 to 125	8 Pin Metal Can	T8.C

Features

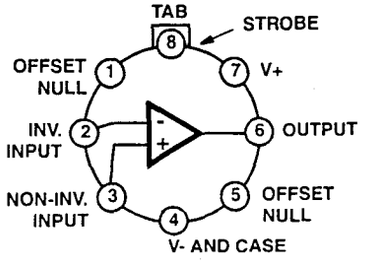
- MOSFET Input Stage
  - Very High Input Impedance (Z_{IN}) -1.5TΩ (Typ)
  - Very Low Input Current (I_I) -10pA (Typ) at ±15V
  - Wide Common Mode Input Voltage Range (V_{ICR}) - Can be Swung 0.5V Below Negative Supply Voltage Rail
  - Output Swing Complements Input Common Mode Range
- Directly Replaces Industry Type 741 in Most Applications

Applications

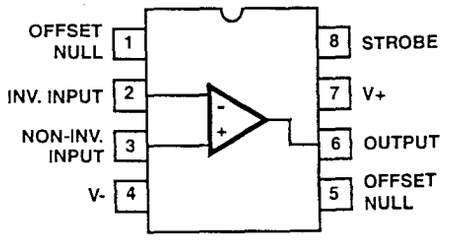
- Ground-Referenced Single Supply Amplifiers in Automobile and Portable Instrumentation
- Sample and Hold Amplifiers
- Long Duration Timers/Multivibrators (μseconds-Minutes-Hours)
- Photocurrent Instrumentation
- Peak Detectors
- Active Filters
- Comparators
- Interface in 5V TTL Systems and Other Low Supply Voltage Systems
- All Standard Operational Amplifier Applications
- Function Generators
- Tone Controls
- Power Supplies
- Portable Instruments
- Intrusion Alarm Systems

Pinouts

CA3140 (METAL CAN)
TOP VIEW



CA3140 (PDIP, SOIC)
TOP VIEW



Absolute Maximum Ratings

DC Supply Voltage (Between V+ and V- Terminals) 36V
Differential Mode Input Voltage 8V
DC Input Voltage . . . . . (V+ +8V) To (V- -0.5V)
Input Terminal Current 1mA
Output Short Circuit Duration (Note 2) . . . . . Indefinite

Operating Conditions

Temperature Range . . . . . $-55^{o}C$ to $125^{o}C$

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^{o}C/W$)	θ_{JC} ($^{o}C/W$)
PDIP Package	100	N/A
SOIC Package	160	N/A
Metal Can Package	170	85

Maximum Junction Temperature (Metal Can Package) . . . . . $175^{o}C$
Maximum Junction Temperature (Plastic Package) . . . . . $150^{o}C$
Maximum Storage Temperature Range . . . . . $-65^{o}C$ to $150^{o}C$
Maximum Lead Temperature (Soldering 10s) . . . . . $300^{o}C$
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
2. Short circuit may be applied to ground or to either supply.

Electrical Specifications $V_{SUPPLY} = \pm15V$, $T_A = 25^{o}C$

PARAMETER	SYMBOL	TEST CONDITIONS		TYPICAL VALUES CA3140	TYPICAL VALUES CA3140A	UNITS
Input Offset Voltage Adjustment Resistor		Typical Value of Resistor Between Terminals 4 and 5 or 4 and 1 to Adjust Max V_{IO}		4.7	18	kΩ
Input Resistance	R_I			1.5	1.5	TΩ
Input Capacitance	C_I			4	4	pF
Output Resistance	R_O			60	60	Ω
Equivalent Wideband Input Noise Voltage (See Figure 27)	e_N	BW = 140kHz, R_S = 1MΩ		48	48	μV
Equivalent Input Noise Voltage (See Figure 35)	e_N	R_S = 100Ω	f = 1kHz	40	40	$nV/\sqrt{Hz}$
			f = 10kHz	12	12	$nV/\sqrt{Hz}$
Short Circuit Current to Opposite Supply	I_{OM+}		Source	40	40	mA
	I_{OM-}		Sink	18	18	mA
Gain-Bandwidth Product, (See Figures 6, 30)	f_T			4.5	4.5	MHz
Slew Rate, (See Figure 31)	SR			9	9	V/μs
Sink Current From Terminal 8 To Terminal 4 to Swing Output Low				220	220	μA
Transient Response (See Figure 28)	t_r	R_L = 2kΩ, C_L = 100pF	Rise Time	0.08	0.08	μs
	OS		Overshoot	10	10	%
Settling Time at $10V_{P-P}$, (See Figure 5)	t_S	R_L = 2kΩ, C_L = 100pF, Voltage Follower	To 1mV	4.5	4.5	μs
			To 10mV	1.4	1.4	μs

Electrical Specifications For Equipment Design, at $V_{SUPPLY} = \pm15V$, $T_A = 25^{o}C$, Unless Otherwise Specified

PARAMETER	SYMBOL	CA3140 MIN	CA3140 TYP	CA3140 MAX	CA3140A MIN	CA3140A TYP	CA3140A MAX	UNITS
Input Offset Voltage	$\lvert V_{IO}\rvert$	-	5	15	-	2	5	mV
Input Offset Current	$\lvert I_{IO}\rvert$	-	0.5	30	-	0.5	20	pA
Input Current	I_I	-	10	50	-	10	40	pA
Large Signal Voltage Gain (Note 3) (See Figures 6, 29)	A_{OL}	20	100	-	20	100	-	kV/V
		86	100	-	86	100	-	dB

Electrical Specifications For Equipment Design, at V_{SUPPLY} = ±15V, T_A = 25°C, Unless Otherwise Specified (Continued)

PARAMETER	SYMBOL	CA3140			CA3140A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Common Mode Rejection Ratio (See Figure 34)	CMRR	-	32	320	-	32	320	µV/V
		70	90	-	70	90	-	dB
Common Mode Input Voltage Range (See Figure 8)	V_{ICR}	-15	-15.5 to +12.5	11	-15	-15.5 to +12.5	12	V
Power-Supply Rejection Ratio, $\Delta V_{IO}/\Delta V_S$ (See Figure 36)	PSRR	-	100	150	-	100	150	µV/V
		76	80	-	76	80	-	dB
Max Output Voltage (Note 4) (See Figures 2, 8)	V_{OM}+	+12	13	-	+12	13	-	V
	V_{OM}-	-14	-14.4	-	-14	-14.4	-	V
Supply Current (See Figure 32)	I+	-	4	6	-	4	6	mA
Device Dissipation	P_D	-	120	180	-	120	180	mW
Input Offset Voltage Temperature Drift	$\Delta V_{IO}/\Delta T$	-	8	-	-	6	-	µV/°C

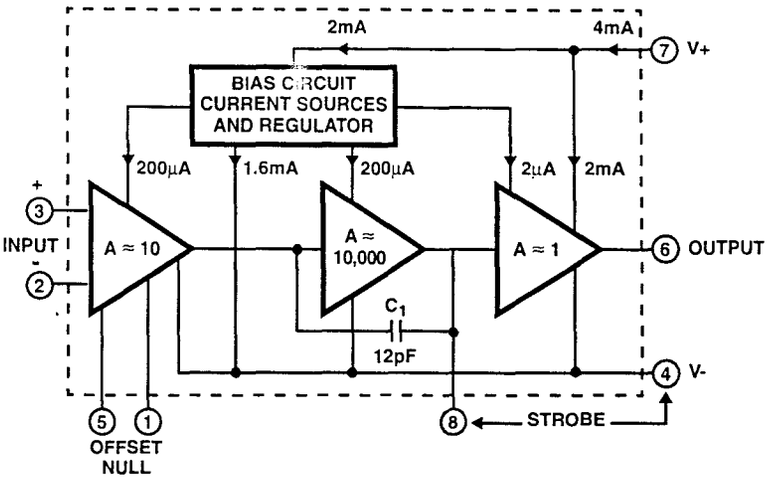
NOTES:

3. At V_O = 26V_{P-P}, +12V, -14V and R_L = 2kΩ.
4. At R_L = 2kΩ.

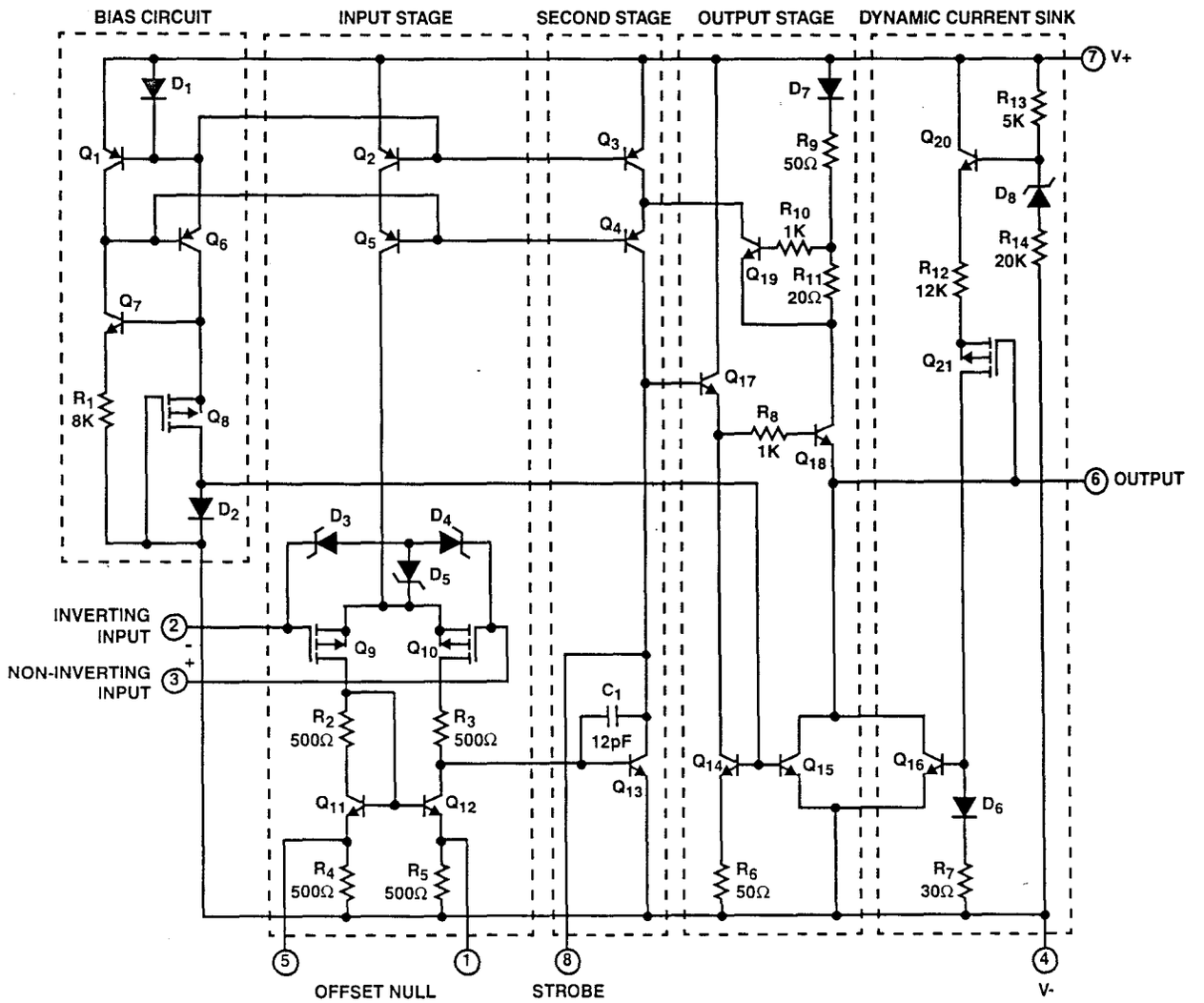
Electrical Specifications For Design Guidance At V+ = 5V, V- = 0V, T_A = 25°C

PARAMETER		SYMBOL	TYPICAL VALUES		UNITS
			CA3140	CA3140A	
Input Offset Voltage		$\|V_{IO}\|$	5	2	mV
Input Offset Current		$\|I_{IO}\|$	0.1	0.1	pA
Input Current		I_I	2	2	pA
Input Resistance		R_I	1	1	TΩ
Large Signal Voltage Gain (See Figures 6, 29)		A_{OL}	100	100	kV/V
			100	100	dB
Common Mode Rejection Ratio		CMRR	32	32	µV/V
			90	90	dB
Common Mode Input Voltage Range (See Figure 8)		V_{ICR}	-0.5	-0.5	V
			2.6	2.6	V
Power Supply Rejection Ratio		PSRR $\Delta V_{IO}/\Delta V_S$	100	100	µV/V
			80	80	dB
Maximum Output Voltage (See Figures 2, 8)		V_{OM}+	3	3	V
		V_{OM}-	0.13	0.13	V
Maximum Output Current:	Source	I_{OM}+	10	10	mA
	Sink	I_{OM}-	1	1	mA
Slew Rate (See Figure 31)		SR	7	7	V/µs
Gain-Bandwidth Product (See Figure 30)		f_T	3.7	3.7	MHz
Supply Current (See Figure 32)		I+	1.6	1.6	mA
Device Dissipation		P_D	8	8	mW
Sink Current from Terminal 8 to Terminal 4 to Swing Output Low			200	200	µA

Block Diagram



Schematic Diagram



NOTE: All resistance values are in ohms.

Application Information

Circuit Description

As shown in the block diagram, the input terminals may be operated down to 0.5V below the negative supply rail. Two class A amplifier stages provide the voltage gain, and a unique class AB amplifier stage provides the current gain necessary to drive low-impedance loads.

A biasing circuit provides control of cascoded constant current flow circuits in the first and second stages. The CA3140 includes an on chip phase compensating capacitor that is sufficient for the unity gain voltage follower configuration.

Input Stage

The schematic diagram consists of a differential input stage using PMOS field-effect transistors (Q_9, Q_{10}) working into a mirror pair of bipolar transistors (Q_{11}, Q_{12}) functioning as load resistors together with resistors R_2 through R_5. The mirror pair transistors also function as a differential-to-single-ended converter to provide base current drive to the second stage bipolar transistor (Q_{13}). Offset nulling, when desired, can be effected with a 10kΩ potentiometer connected across Terminals 1 and 5 and with its slider arm connected to Terminal 4. Cascode-connected bipolar transistors Q_2, Q_5 are the constant current source for the input stage. The base biasing circuit for the constant current source is described subsequently. The small diodes D_3, D_4, D_5 provide gate oxide protection against high voltage transients, e.g., static electricity.

Second Stage

Most of the voltage gain in the CA3140 is provided by the second amplifier stage, consisting of bipolar transistor Q_{13} and its cascode connected load resistance provided by bipolar transistors Q_3, Q_4. On-chip phase compensation, sufficient for a majority of the applications is provided by C_1. Additional Miller-Effect compensation (roll off) can be accomplished, when desired, by simply connecting a small capacitor between Terminals 1 and 8. Terminal 8 is also used to strobe the output stage into quiescence. When terminal 8 is tied to the negative supply rail (Terminal 4) by mechanical or electrical means, the output Terminal 6 swings low, i.e., approximately to Terminal 4 potential.

Output Stage

The CA3140 Series circuits employ a broad band output stage that can sink loads to the negative supply to complement the capability of the PMOS input stage when operating near the negative rail. Quiescent current in the emitter-follower cascade circuit (Q_{17}, Q_{18}) is established by transistors (Q_{14}, Q_{15}) whose base currents are "mirrored" to current flowing through diode D_2 in the bias circuit section. When the CA3140 is operating such that output Terminal 6 is sourcing current, transistor Q_{18} functions as an emitter-follower to source current from the V+ bus (Terminal 7), via D_7, R_9, and R_{11}. Under these conditions, the collector potential of Q_{13} is sufficiently high to permit the necessary flow of base current to emitter follower Q_{17} which, in turn, drives Q_{18}.

When the CA3140 is operating such that output Terminal 6 is sinking current to the V- bus, transistor Q_{16} is the current sinking element. Transistor Q_{16} is mirror connected to D_6, R_7, with current fed by way of Q_{21}, R_{12}, and Q_{20}. Transistor Q_{20}, in turn, is biased by current flow through R_{13}, zener D_8, and R_{14}. The dynamic current sink is controlled by voltage level sensing. For purposes of explanation, it is assumed that output Terminal 6 is quiescently established at the potential midpoint between the V+ and V- supply rails. When output current sinking mode operation is required, the collector potential of transistor Q_{13} is driven below its quiescent level, thereby causing Q_{17}, Q_{18} to decrease the output voltage at Terminal 6. Thus, the gate terminal of PMOS transistor Q_{21} is displaced toward the V- bus, thereby reducing the channel resistance of Q_{21}. As a consequence, there is an incremental increase in current flow through Q_{20}, R_{12}, Q_{21}, D_6, R_7, and the base of Q_{16}. As a result, Q_{16} sinks current from Terminal 6 in direct response to the incremental change in output voltage caused by Q_{18}. This sink current flows regardless of load; any excess current is internally supplied by the emitter-follower Q_{18}. Short circuit protection of the output circuit is provided by Q_{19}, which is driven into conduction by the high voltage drop developed across R_{11} under output short circuit conditions. Under these conditions, the collector of Q_{19} diverts current from Q_4 so as to reduce the base current drive from Q_{17}, thereby limiting current flow in Q_{18} to the short circuited load terminal.

Bias Circuit

Quiescent current in all stages (except the dynamic current sink) of the CA3140 is dependent upon bias current flow in R_1. The function of the bias circuit is to establish and maintain constant current flow through D_1, Q_6, Q_8 and D_2. D_1 is a diode connected transistor mirror connected in parallel with the base emitter junctions of Q_1, Q_2, and Q_3. D_1 may be considered as a current sampling diode that senses the emitter current of Q_6 and automatically adjusts the base current of Q_6 (via Q_1) to maintain a constant current through Q_6, Q_8, D_2. The base currents in Q_2, Q_3 are also determined by constant current flow D_1. Furthermore, current in diode connected transistor Q_2 establishes the currents in transistors Q_{14} and Q_{15}.

Typical Applications

Wide dynamic range of input and output characteristics with the most desirable high input impedance characteristics is achieved in the CA3140 by the use of an unique design based upon the PMOS Bipolar process. Input common mode voltage range and output swing capabilities are complementary, allowing operation with the single supply down to 4V.

The wide dynamic range of these parameters also means that this device is suitable for many single supply applications. such as, for example, where one input is driven below the potential of Terminal 4 and the phase sense of the output signal must be maintained – a most important consideration in comparator applications.

Output Circuit Considerations

Excellent interfacing with TTL circuitry is easily achieved with a single 6.2V zener diode connected to Terminal 8 as shown in Figure 1. This connection assures that the maximum output signal swing will not go more positive than the zener voltage minus two base-to-emitter voltage drops within the CA3140. These voltages are independent of the operating supply voltage.

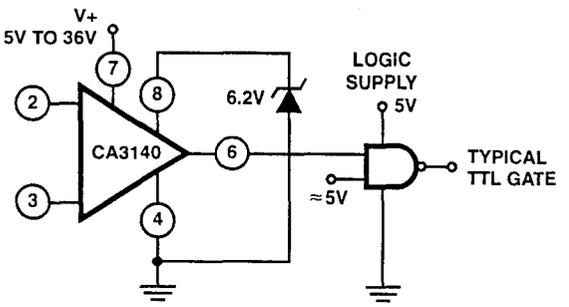


FIGURE 1. ZENER CLAMPING DIODE CONNECTED TO TERMINALS 8 AND 4 TO LIMIT CA3140 OUTPUT SWING TO TTL LEVELS

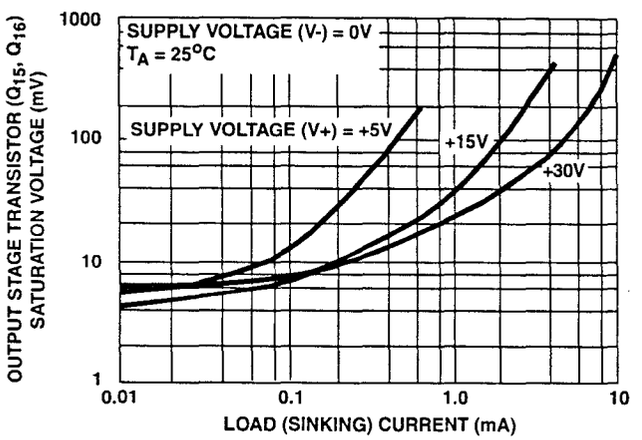


FIGURE 2. VOLTAGE ACROSS OUTPUT TRANSISTORS (Q_{15} AND Q_{16}) vs LOAD CURRENT

Figure 2 shows output current sinking capabilities of the CA3140 at various supply voltages. Output voltage swing to the negative supply rail permits this device to operate both power transistors and thyristors directly without the need for level shifting circuitry usually associated with the 741 series of operational amplifiers.

Figure 4 shows some typical configurations. Note that a series resistor, R_L, is used in both cases to limit the drive available to the driven device. Moreover, it is recommended that a series diode and shunt diode be used at the thyristor input to prevent large negative transient surges that can appear at the gate of thyristors, from damaging the integrated circuit.

Offset Voltage Nulling

The input offset voltage can be nulled by connecting a 10kΩ potentiometer between Terminals 1 and 5 and returning its wiper arm to terminal 4, see Figure 3A. This technique, however, gives more adjustment range than required and therefore, a considerable portion of the potentiometer rotation is not fully utilized. Typical values of series resistors (R) that may be placed at either end of the potentiometer, see Figure 3B, to optimize its utilization range are given in the Electrical Specifications table.

An alternate system is shown in Figure 3C. This circuit uses only one additional resistor of approximately the value shown in the table. For potentiometers, in which the resistance does not drop to 0Ω at either end of rotation, a value of resistance 10% lower than the values shown in the table should be used.

Low Voltage Operation

Operation at total supply voltages as low as 4V is possible with the CA3140. A current regulator based upon the PMOS threshold voltage maintains reasonable constant operating current and hence consistent performance down to these lower voltages.

The low voltage limitation occurs when the upper extreme of the input common mode voltage range extends down to the voltage at Terminal 4. This limit is reached at a total supply voltage just below 4V. The output voltage range also begins to extend down to the negative supply rail, but is slightly higher than that of the input. Figure 8 shows these characteristics and shows that with 2V dual supplies, the lower extreme of the input common mode voltage range is below ground potential.

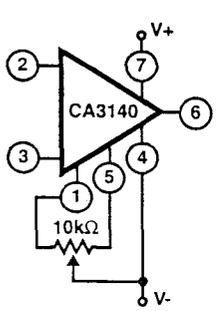


FIGURE 3A. BASIC

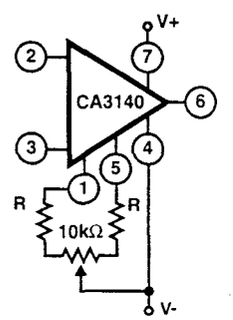


FIGURE 3B. IMPROVED RESOLUTION

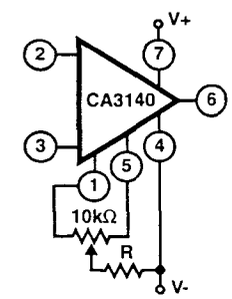
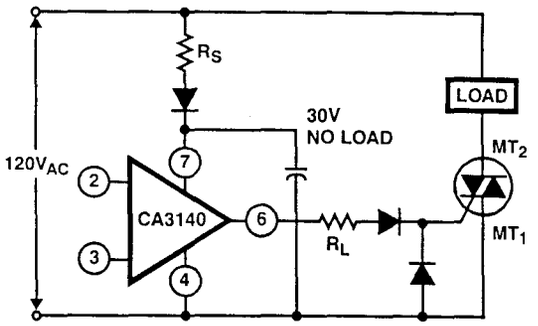


FIGURE 3C. SIMPLER IMPROVED RESOLUTION

FIGURE 3. THREE OFFSET VOLTAGE NULLING METHODS



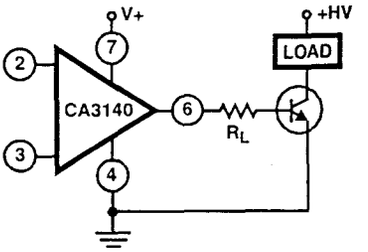


FIGURE 4. METHODS OF UTILIZING THE $V_{CE(SAT)}$ SINKING CURRENT CAPABILITY OF THE CA3140 SERIES

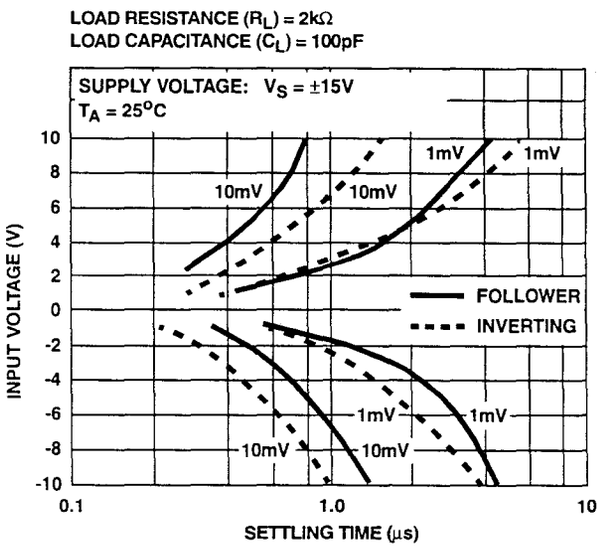


FIGURE 5A. WAVEFORM

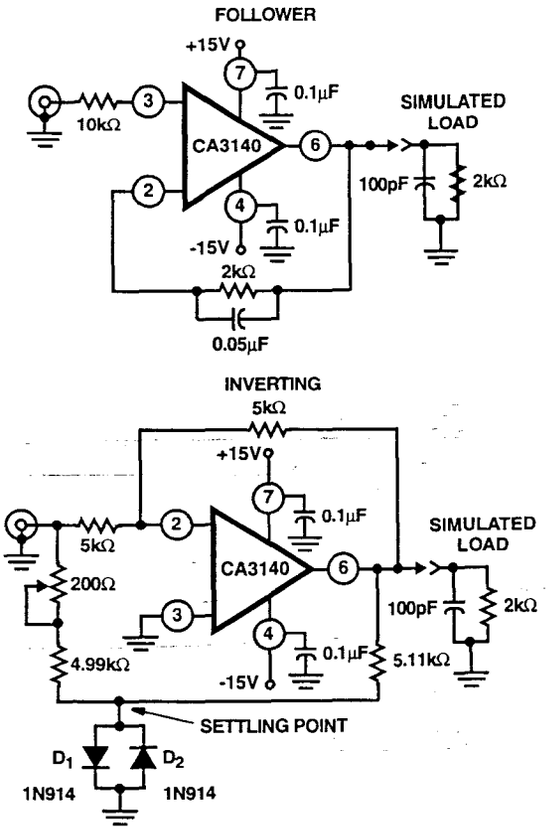


FIGURE 5B. TEST CIRCUITS

FIGURE 5. SETTLING TIME vs INPUT VOLTAGE

Bandwidth and Slew Rate

For those cases where bandwidth reduction is desired, for example, broadband noise reduction, an external capacitor connected between Terminals 1 and 8 can reduce the open loop -3dB bandwidth. The slew rate will, however, also be proportionally reduced by using this additional capacitor. Thus, a 20% reduction in bandwidth by this technique will also reduce the slew rate by about 20%.

Figure 5 shows the typical settling time required to reach 1mV or 10mV of the final value for various levels of large signal inputs for the voltage follower and inverting unity gain amplifiers. The exceptionally fast settling time characteristics are largely due to the high combination of high gain and wide bandwidth of the CA3140; as shown in Figure 6.

Input Circuit Considerations

As mentioned previously, the amplifier inputs can be driven below the Terminal 4 potential, but a series current limiting resistor is recommended to limit the maximum input terminal current to less than 1mA to prevent damage to the input protection circuitry.

Moreover, some current limiting resistance should be provided between the inverting input and the output when the CA3140 is used as a unity gain voltage follower. This resistance prevents the possibility of extremely large input

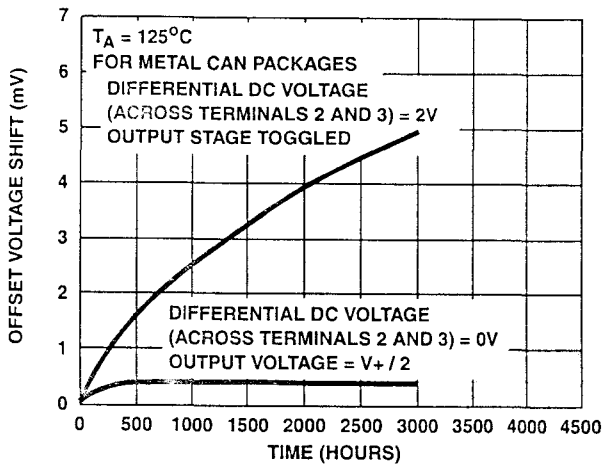


FIGURE 9. TYPICAL INCREMENTAL OFFSET VOLTAGE SHIFT vs OPERATING LIFE

Super Sweep Function Generator

A function generator having a wide tuning range is shown in Figure 10. The 1,000,000/1 adjustment range is accomplished by a single variable potentiometer or by an auxiliary sweeping signal. The CA3140 functions as a non-inverting readout amplifier of the triangular signal developed across the integrating capacitor network connected to the output of the CA3080A current source.

Buffered triangular output signals are then applied to a second CA3080 functioning as a high speed hysteresis switch. Output from the switch is returned directly back to the input of the CA3080A current source, thereby, completing the positive feedback loop

The triangular output level is determined by the four 1N914 level limiting diodes of the second CA3080 and the resistor divider network connected to Terminal No. 2 (input) of the CA3080. These diodes establish the input trip level to this switching stage and, therefore, indirectly determine the amplitude of the output triangle.

Compensation for propagation delays around the entire loop is provided by one adjustment on the input of the CA3080. This adjustment, which provides for a constant generator amplitude output, is most easily made while the generator is sweeping. High frequency ramp linearity is adjusted by the single 7pF to 60pF capacitor in the output of the CA3080A.

It must be emphasized that only the CA3080A is characterized for maximum output linearity in the current generator function.

Meter Driver and Buffer Amplifier

Figure 11 shows the CA3140 connected as a meter driver and buffer amplifier. Low driving impedance is required of the CA3080A current source to assure smooth operation of the Frequency Adjustment Control. This low-driving impedance requirement is easily met by using a CA3140 connected as a voltage follower. Moreover, a meter may be placed across the input to the CA3080A to give a logarithmic analog indication of the function generator's frequency.

Analog frequency readout is readily accomplished by the means described above because the output current of the CA3080A varies approximately one decade for each 60mV change in the applied voltage, V_{ABC} (voltage between Terminals 5 and 4 of the CA3080A of the function generator). Therefore, six decades represent 360mV change in V_{ABC}.

Now, only the reference voltage must be established to set the lower limit on the meter. The three remaining transistors from the CA3086 Array used in the sweep generator are used for this reference voltage. In addition, this reference generator arrangement tends to track ambient temperature variations, and thus compensates for the effects of the normal negative temperature coefficient of the CA3080A V_{ABC} terminal voltage.

Another output voltage from the reference generator is used to insure temperature tracking of the lower end of the Frequency Adjustment Potentiometer. A large series resistance simulates a current source, assuring similar temperature coefficients at both ends of the Frequency Adjustment Control.

To calibrate this circuit, set the Frequency Adjustment Potentiometer at its low end. Then adjust the Minimum Frequency Calibration Control for the lowest frequency. To establish the upper frequency limit, set the Frequency Adjustment Potentiometer to its upper end and then adjust the Maximum Frequency Calibration Control for the maximum frequency. Because there is interaction among these controls, repetition of the adjustment procedure may be necessary. Two adjustments are used for the meter. The meter sensitivity control sets the meter scale width of each decade, while the meter position control adjusts the pointer on the scale with negligible effect on the sensitivity adjustment. Thus, the meter sensitivity adjustment control calibrates the meter so that it deflects $^1/_6$ of full scale for each decade change in frequency.

Sine Wave Shaper

The circuit shown in Figure 12 uses a CA3140 as a voltage follower in combination with diodes from the CA3019 Array to convert the triangular signal from the function generator to a sine-wave output signal having typically less than 2% THD. The basic zero crossing slope is established by the 10kΩ potentiometer connected between Terminals 2 and 6 of the CA3140 and the 9.1kΩ resistor and 10kΩ potentiometer from Terminal 2 to ground. Two break points are established by diodes D_1 through D_4. Positive feedback via D_5 and D_6 establishes the zero slope at the maximum and minimum levels of the sine wave. This technique is necessary because the voltage follower configuration approaches unity gain rather than the zero gain required to shape the sine wave at the two extremes.

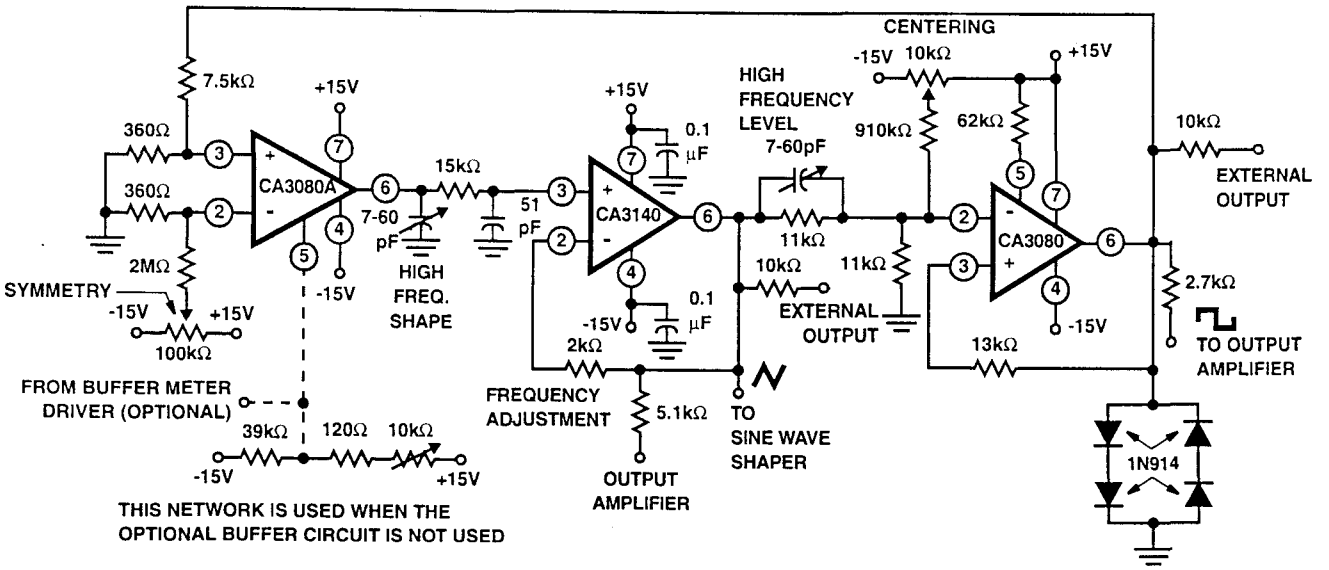
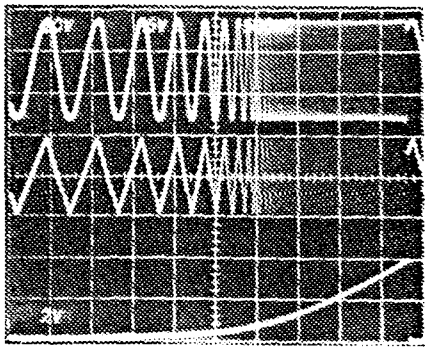


FIGURE 10A. CIRCUIT

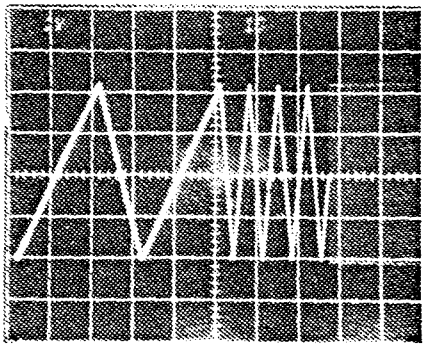


Top Trace: Output at junction of 2.7Ω and 51Ω resistors; 5V/Div., 500ms/Div.

Center Trace: External output of triangular function generator; 2V/Div., 500ms/Div.

Bottom Trace: Output of "Log" generator; 10V/Div., 500ms/Div.

FIGURE 10B. FIGURE FUNCTION GENERATOR SWEEPING



1V/Div., 1s/Div.

Three tone test signals, highest frequency ≥0.5MHz. Note the slight asymmetry at the three second/cycle signal. This asymmetry is due to slightly different positive and negative integration from the CA3080A and from the PC board and component leakages at the 100pA level.

FIGURE 10C. FUNCTION GENERATOR WITH FIXED FREQUENCIES

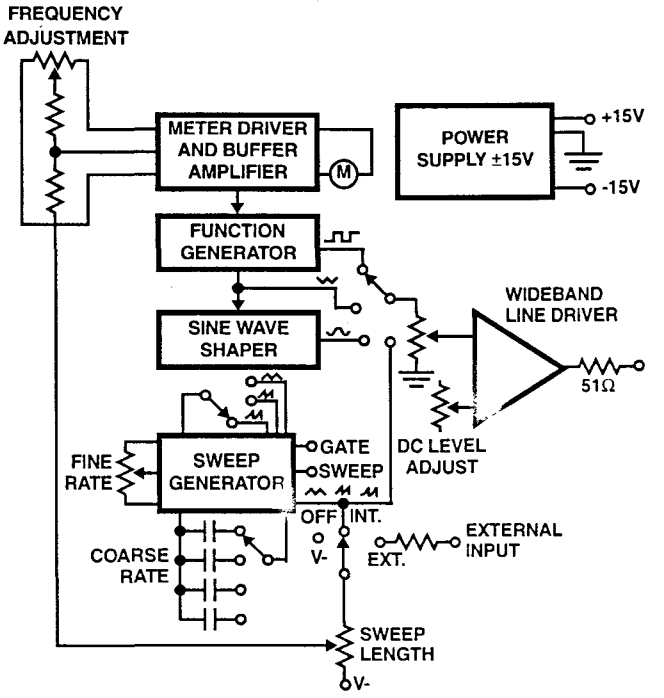


FIGURE 10D. INTERCONNECTIONS

FIGURE 10. FUNCTION GENERATOR

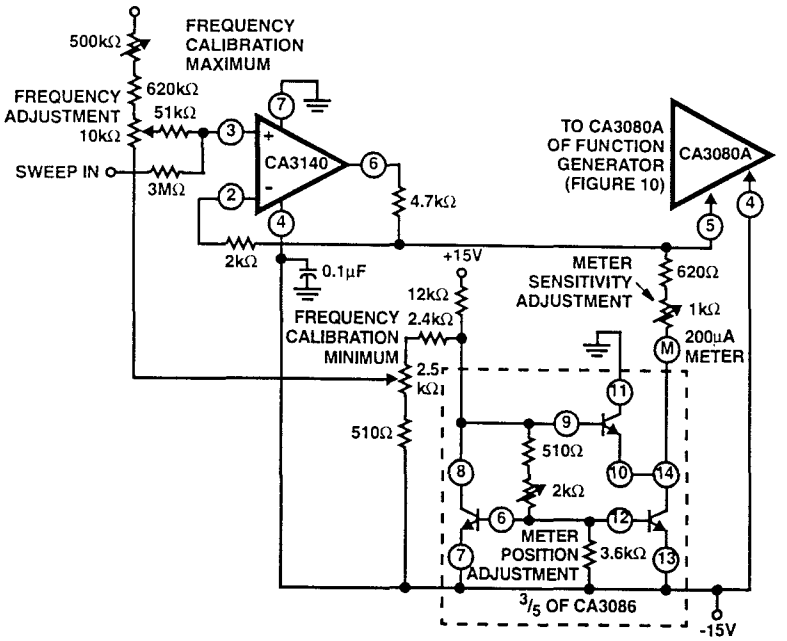


FIGURE 11. METER DRIVER AND BUFFER AMPLIFIER

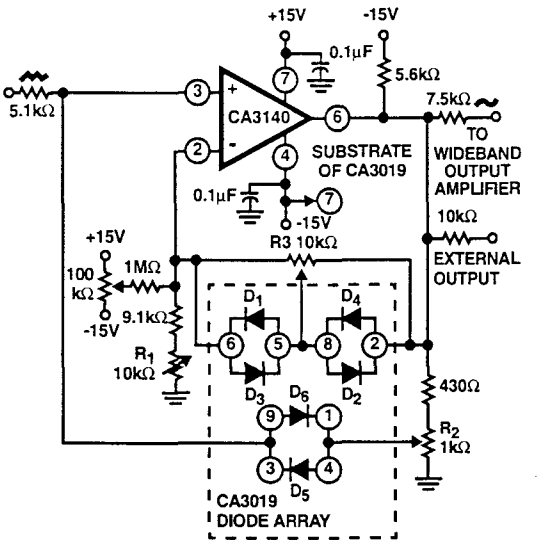


FIGURE 12. SINE WAVE SHAPER

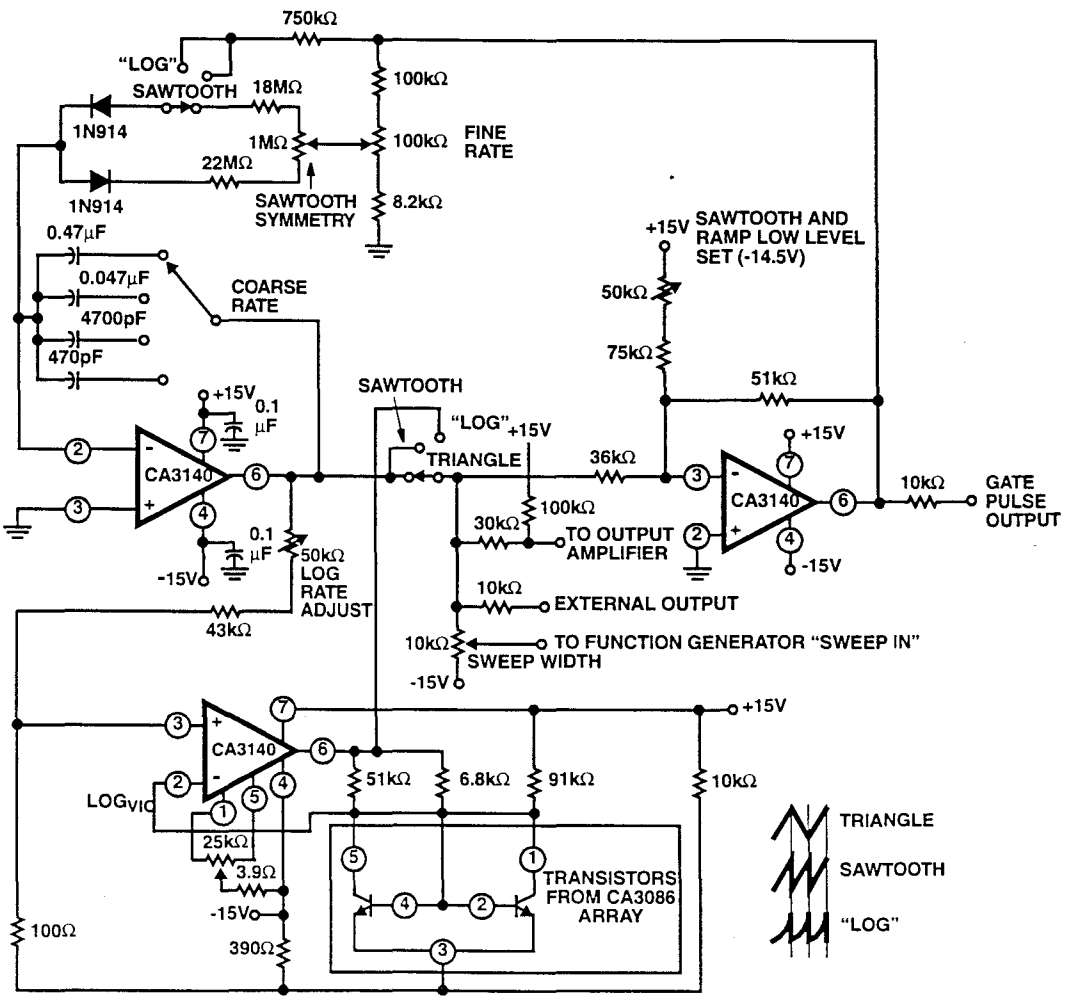


FIGURE 13. SWEEPING GENERATOR

This circuit can be adjusted most easily with a distortion analyzer, but a good first approximation can be made by comparing the output signal with that of a sine wave generator. The initial slope is adjusted with the potentiometer R_1, followed by an adjustment of R_2. The final slope is established by adjusting R_3, thereby adding additional segments that are contributed by these diodes. Because there is some interaction among these controls, repetition of the adjustment procedure may be necessary.

Sweeping Generator

Figure 13 shows a sweeping generator. Three CA3140s are used in this circuit. One CA3140 is used as an integrator, a second device is used as a hysteresis switch that determines the starting and stopping points of the sweep. A third CA3140 is used as a logarithmic shaping network for the log function. Rates and slopes, as well as sawtooth, triangle, and logarithmic sweeps are generated by this circuit.

Wideband Output Amplifier

Figure 14 shows a high slew rate, wideband amplifier suitable for use as a 50Ω transmission line driver. This circuit, when used in conjunction with the function generator and sine wave shaper circuits shown in Figures 10 and 12 provides $18V_{P-P}$ output open circuited, or $9V_{P-P}$ output when terminated in 50Ω. The slew rate required of this amplifier is 28V/μs ($18V_{P-P} \times \pi \times 0.5MHz$).

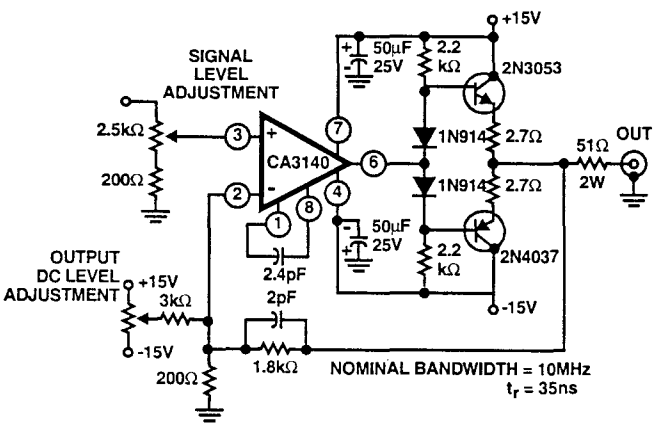


FIGURE 14. WIDEBAND OUTPUT AMPLIFIER

Power Supplies

High input impedance, common mode capability down to the negative supply and high output drive current capability are key factors in the design of wide range output voltage supplies that use a single input voltage to provide a regulated output voltage that can be adjusted from essentially 0V to 24V.

Unlike many regulator systems using comparators having a bipolar transistor input stage, a high impedance reference voltage divider from a single supply can be used in n with the CA3140 (see Figure 15).

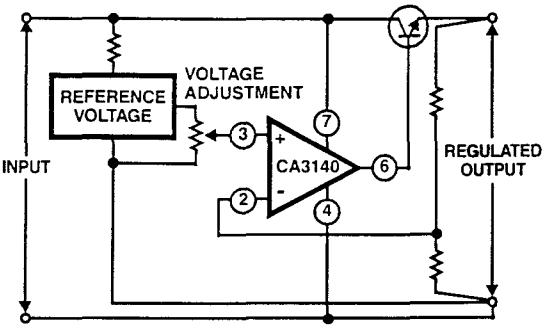


FIGURE 15. BASIC SINGLE SUPPLY VOLTAGE REGULATOR SHOWING VOLTAGE FOLLOWER CONFIGURATION

Essentially, the regulators, shown in Figures 16 and 17, are connected as non inverting power operational amplifiers with a gain of 3.2. An 8V reference input yields a maximum output voltage slightly greater than 25V. As a voltage follower, when the reference input goes to 0V the output will be 0V. Because the offset voltage is also multiplied by the 3.2 gain factor, a potentiometer is needed to null the offset voltage.

Series pass transistors with high I_{CBO} levels will also prevent the output voltage from reaching zero because there is a finite voltage drop (V_{CESAT}) across the output of the CA3140 (see Figure 2). This saturation voltage level may indeed set the lowest voltage obtainable.

The high impedance presented by Terminal 8 is advantageous in effecting current limiting. Thus, only a small signal transistor is required for the current-limit sensing amplifier. Resistive decoupling is provided for this transistor to minimize damage to it or the CA3140 in the event of unusual input or output transients on the supply rail.

Figures 16 and 17, show circuits in which a D2201 high speed diode is used for the current sensor. This diode was chosen for its slightly higher forward voltage drop characteristic, thus giving greater sensitivity. It must be emphasized that heat sinking of this diode is essential to minimize variation of the current trip point due to internal heating of the diode. That is, 1A at 1V forward drop represents one watt which can result in significant regenerative changes in the current trip point as the diode temperature rises. Placing the small signal reference amplifier in the proximity of the current sensing diode also helps minimize the variability in the trip level due to the negative temperature coefficient of the diode. In spite of those limitations, the current limiting point can easily be adjusted over the range from 10mA to 1A with a single adjustment potentiometer. If the temperature stability of the current limiting system is a serious consideration, the more usual current sampling resistor type of circuitry should be employed.

A power Darlington transistor (in a metal can with heatsink), is used as the series pass element for the conventional current limiting system. Figure 16, because high power Darlington dissipation will be encountered at low output voltage and high currents.

A small heat sink VERSAWATT transistor is used as the series pass element in the fold back current system, Figure 17, since dissipation levels will only approach 10W. In this system, the D2201 diode is used for current sampling. Foldback is provided by the 3kΩ and 100kΩ divider network connected to the base of the current sensing transistor.

Both regulators provide better than 0.02% load regulation. Because there is constant loop gain at all voltage settings, the regulation also remains constant. Line regulation is 0.1% per volt. Hum and noise voltage is less than 200μV as read with a meter having a 10MHz bandwidth.

Figure 18A shows the turn ON and turn OFF characteristics of both regulators. The slow turn on rise is due to the slow rate of rise of the reference voltage. Figure 18B shows the transient response of the regulator with the switching of a 20Ω load at 20V output.

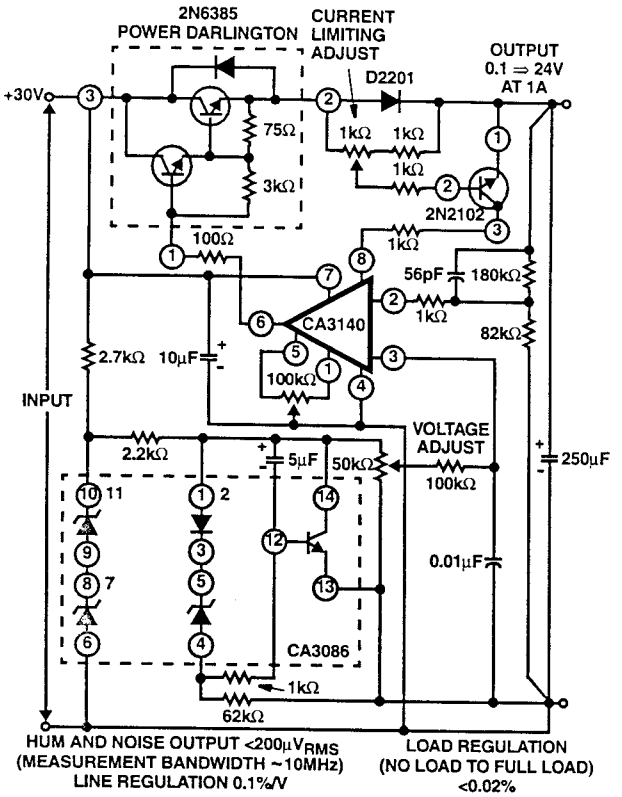


FIGURE 16. REGULATED POWER SUPPLY

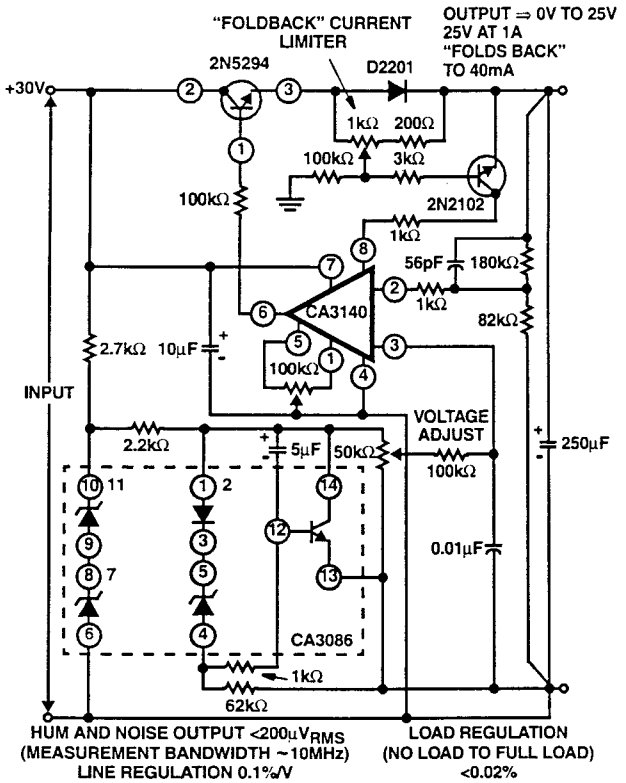
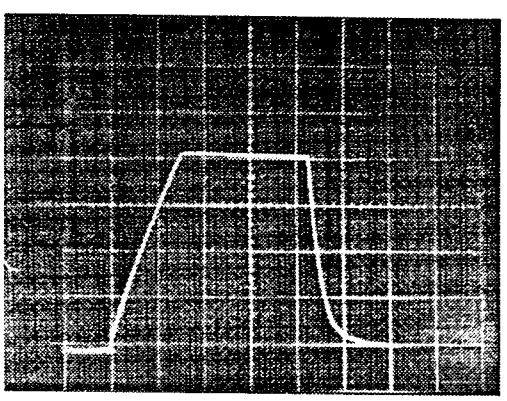
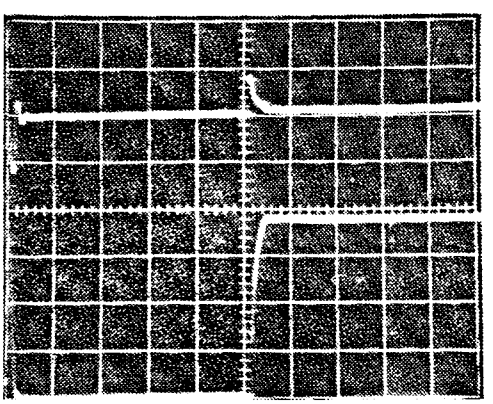


FIGURE 17. REGULATED POWER SUPPLY WITH "FOLDBACK" CURRENT LIMITING



5V/Div., 1s/Div.

FIGURE 18A. SUPPLY TURN-ON AND TURNOFF CHARACTERISTICS



Top Trace: Output Voltage; 200mV/Div., 5μs/Div.

Bottom Trace: Collector of load switching transistor, load = 1A; 5V/Div., 5μs/Div.

FIGURE 18B. TRANSIENT RESPONSE

FIGURE 18. WAVEFORMS OF DYNAMIC CHARACTERISTICS OF POWER SUPPLY CURRENTS SHOWN IN FIGURES 16 AND 17

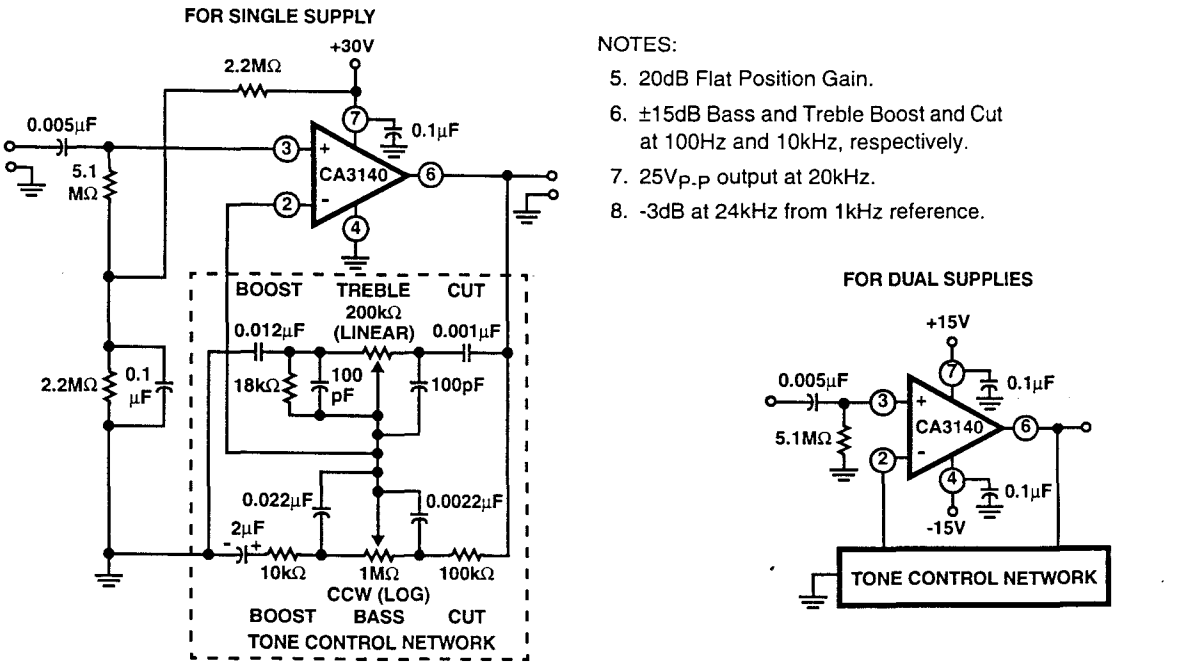
Tone Control Circuits

High slew rate, wide bandwidth, high output voltage capability and high input impedance are all characteristics required of tone control amplifiers. Two tone control circuits that exploit these characteristics of the CA3140 are shown in Figures 19 and 20.

The first circuit, shown in Figure 20, is the Baxandall tone control circuit which provides unity gain at midband and uses standard linear potentiometers. The high input impedance of the CA3140 makes possible the use of low-cost, low-value, small size capacitors, as well as reduced load of the driving stage.

Bass treble boost and cut are ±15dB at 100Hz and 10kHz, respectively. Full peak-to-peak output is available up to at least 20kHz due to the high slew rate of the CA3140. The amplifier gain is 3dB down from its "flat" position at 70kHz.

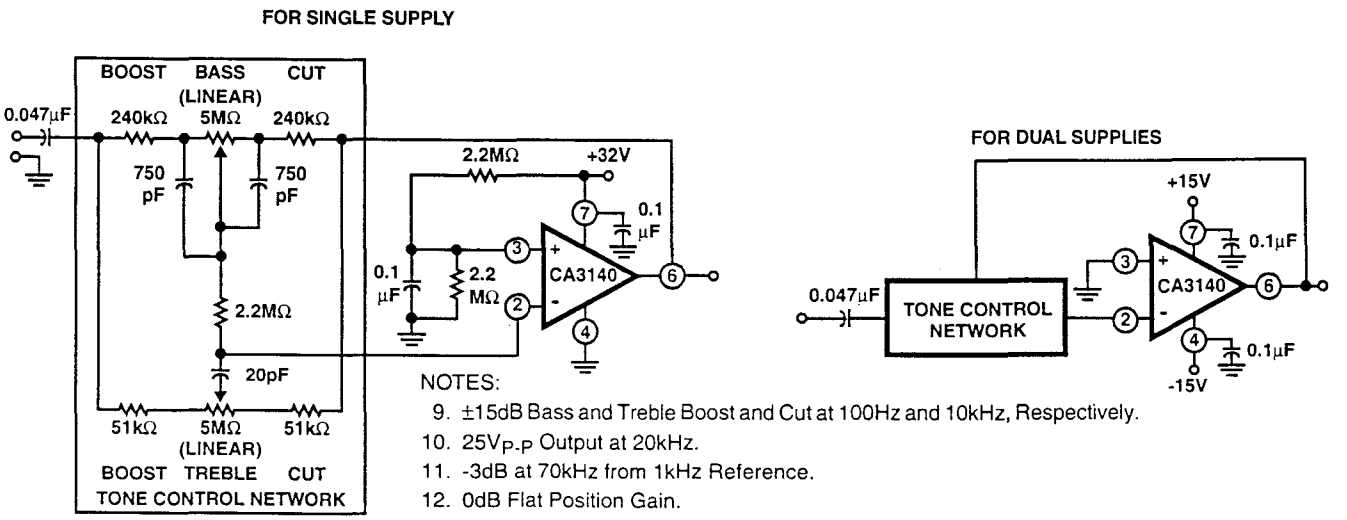
Figure 19 shows another tone control circuit with similar boost and cut specifications. The wideband gain of this circuit is equal to the ultimate boost or cut plus one, which in this case is a gain of eleven. For 20dB boost and cut, the input loading of this circuit is essentially equal to the value of the resistance from Terminal No. 3 to ground. A detailed analysis of this circuit is given in "An IC Operational Transconductance Amplifier (OTA) With Power Capability" by L. Kaplan and H. Wittlinger, IEEE Transactions on Broadcast and Television Receivers, Vol. BTR-18, No. 3, August, 1972.



NOTES:

5. 20dB Flat Position Gain.
6. ±15dB Bass and Treble Boost and Cut at 100Hz and 10kHz, respectively.
7. $25V_{P-P}$ output at 20kHz.
8. -3dB at 24kHz from 1kHz reference.

FIGURE 19. TONE CONTROL CIRCUIT USING CA3130 SERIES (20dB MIDBAND GAIN)



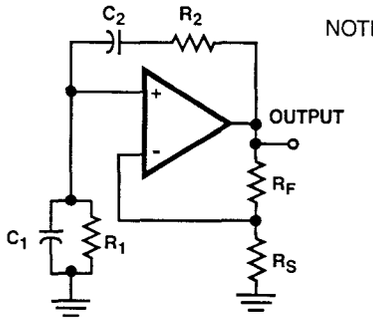
NOTES:

9. ±15dB Bass and Treble Boost and Cut at 100Hz and 10kHz, Respectively.
10. $25V_{P-P}$ Output at 20kHz.
11. -3dB at 70kHz from 1kHz Reference.
12. 0dB Flat Position Gain.

FIGURE 20. BAXANDALL TONE CONTROL CIRCUIT USING CA3140 SERIES

Wien Bridge Oscillator

Another application of the CA3140 that makes excellent use of its high input impedance, high slew rate, and high voltage qualities is the Wien Bridge sine wave oscillator. A basic Wien Bridge oscillator is shown in Figure 21. When $R_1 = R_2 = R$ and $C_1 = C_2 = C$, the frequency equation reduces to the familiar $f = 1/(2\pi RC)$ and the gain required for oscillation, A_{OSC} is equal to 3. Note that if C_2 is increased by a factor of four and R_2 is reduced by a factor of four, the gain required for oscillation becomes 1.5, thus permitting a potentially higher operating frequency closer to the gain bandwidth product of the CA3140.



NOTES:

$$f = \frac{1}{2\pi\sqrt{R_1 C_1 R_2 C_2}}$$

$$A_{OSC} = 1 + \frac{C_1}{C_2} + \frac{R_2}{R_1}$$

$$A_{CL} = 1 + \frac{R_F}{R_S}$$

FIGURE 21. BASIC WIEN BRIDGE OSCILLATOR CIRCUIT USING AN OPERATIONAL AMPLIFIER

Oscillator stabilization takes on many forms. It must be precisely set, otherwise the amplitude will either diminish or reach some form of limiting with high levels of distortion. The element, R_S, is commonly replaced with some variable resistance element. Thus, through some control means, the value of R_S is adjusted to maintain constant oscillator output. A FET channel resistance, a thermistor, a lamp bulb, or other device whose resistance increases as the output amplitude is increased are a few of the elements often utilized.

Figure 22 shows another means of stabilizing the oscillator with a zener diode shunting the feedback resistor (R_F of Figure 21). As the output signal amplitude increases, the zener diode impedance decreases resulting in more feedback with consequent reduction in gain; thus stabilizing the amplitude of the output signal. Furthermore, this combination of a monolithic zener diode and bridge rectifier circuit tends to provide a zero temperature coefficient for this regulating system. Because this bridge rectifier system has no time constant, i.e., thermal time constant for the lamp bulb, and RC time constant for filters often used in detector networks, there is no lower frequency limit. For example, with 1µF polycarbonate capacitors and 22MΩ for the frequency determining network, the operating frequency is 0.007Hz.

As the frequency is increased, the output amplitude must be reduced to prevent the output signal from becoming slew-rate limited. An output frequency of 180kHz will reach a slew rate [illegible]oximately 9V/µs when its amplitude is $16V_{P-P}$.

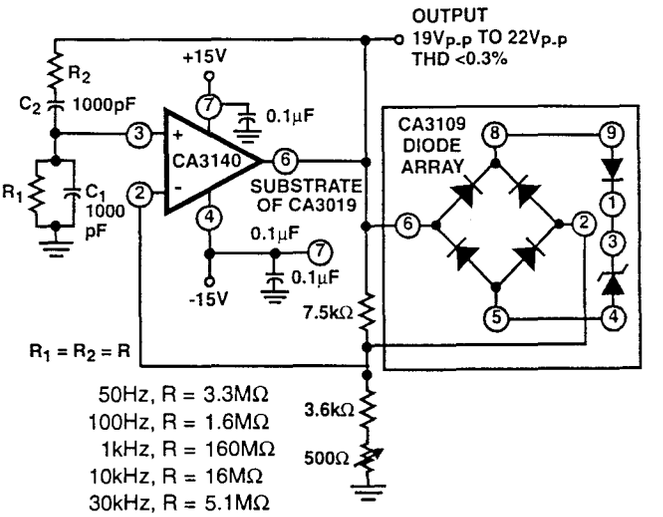


FIGURE 22. WIEN BRIDGE OSCILLATOR CIRCUIT USING CA3140

Simple Sample-and-Hold System

Figure 23 shows a very simple sample-and-hold system using the CA3140 as the readout amplifier for the storage capacitor. The CA3080A serves as both input buffer amplifier and low feed-through transmission switch (see Note 13). System offset nulling is accomplished with the CA3140 via its offset nulling terminals. A typical simulated load of 2kΩ and 30pF is shown in the schematic.

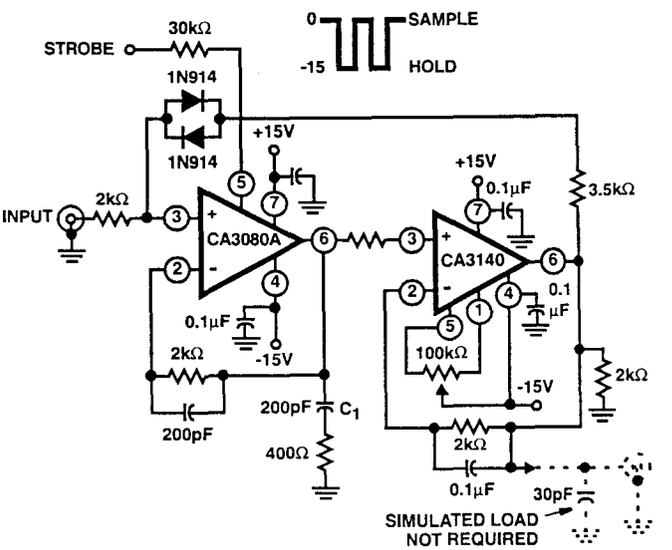


FIGURE 23. SAMPLE AND HOLD CIRCUIT

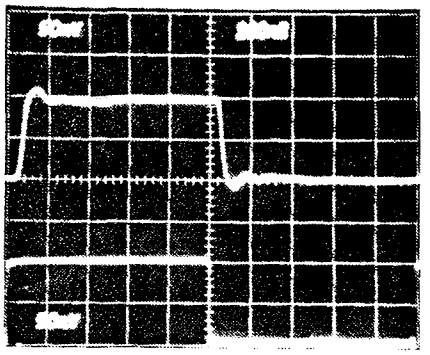
In this circuit, the storage compensation capacitance (C_1) is only 200pF. Larger value capacitors provide longer "hold" periods but with slower slew rates. The slew rate is:

$$\frac{dv}{dt} = \frac{I}{C} = 0.5mA/200pF = 2.5V/\mu s$$

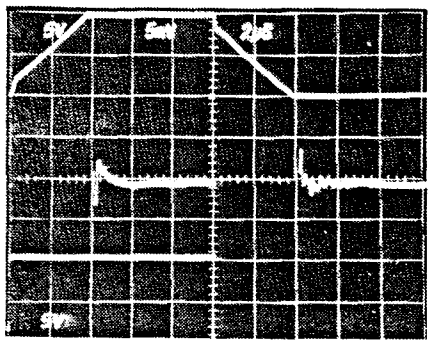
NOTE:

13. AN6668 "Applications of the CA3080 and CA 3080A High Performance Operational Transconductance Amplifiers".

Pulse "droop" during the hold interval is 170pA/200pF which is 0.85μV/μs; (i.e., 170pA/200pF). In this case, 170pA represents the typical leakage current of the CA3080A when strobed off. If C_1 were increased to 2000pF, the "hold-droop" rate will decrease to 0.085μV/μs, but the slew rate would decrease to 0.25V/μs. The parallel diode network connected between Terminal 3 of the CA3080A and Terminal 6 of the CA3140 prevents large input signal feedthrough across the input terminals of the CA3080A to the 200pF storage capacitor when the CA3080A is strobed off. Figure 24 shows dynamic characteristic waveforms of this sample-and-hold system.

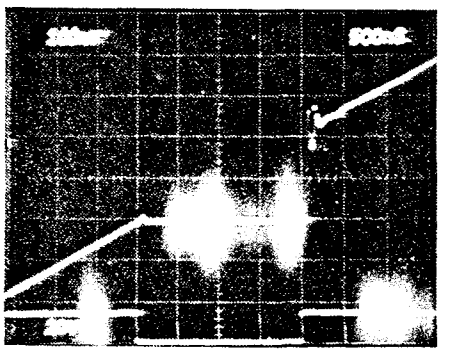


Top Trace: Output; 50mV/Div., 200ns/Div.
Bottom Trace: Input; 50mV/Div., 200ns/Div.



Top Trace: Output Signal; 5V/Div, 2μs/Div.
Center Trace: Difference of Input and Output Signals through Tektronix Amplifier 7A13; 5mV/Div., 2μs/Div.
Bottom Trace: Input Signal; 5V/Div., 2μs/Div.

LARGE SIGNAL RESPONSE AND SETTLING TIME



SAMPLING RESPONSE

Top Trace: Output; 100mV/Div., 500ns/Div.
Bottom Trace: Input; 20V/Div., 500ns/Div.

FIGURE 24. SAMPLE AND HOLD SYSTEM DYNAMIC CHARACTERISTICS WAVEFORMS

Current Amplifier

The low input terminal current needed to drive the CA3140 makes it ideal for use in current amplifier applications such as the one shown in Figure 25 (see Note 14). In this circuit, low current is supplied at the input potential as the power supply to load resistor R_L. This load current is increased by the multiplication factor R_2/R_1, when the load current is monitored by the power supply meter M. Thus, if the load current is 100nA, with values shown, the load current presented to the supply will be 100μA; a much easier current to measure in many systems.

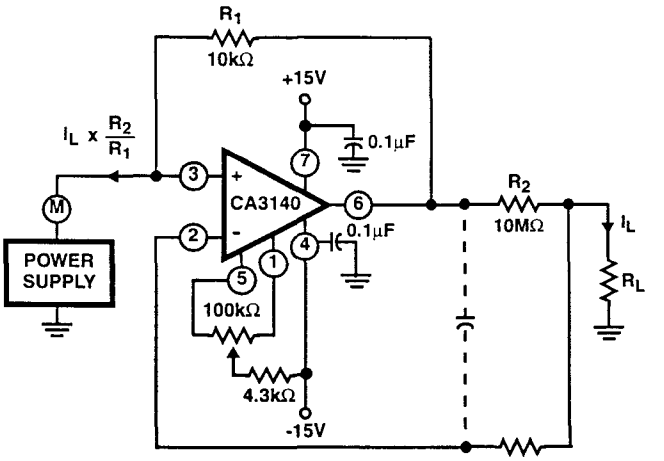


FIGURE 25. BASIC CURRENT AMPLIFIER FOR LOW CURRENT MEASUREMENT SYSTEMS

Note that the input and output voltages are transferred at the same potential and only the output current is multiplied by the scale factor.

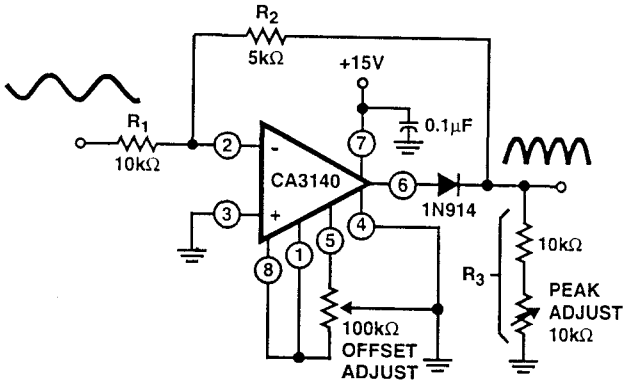
The dotted components show a method of decoupling the circuit from the effects of high output load capacitance and the potential oscillation in this situation. Essentially, the necessary high frequency feedback is provided by the capacitor with the dotted series resistor providing load decoupling.

Full Wave Rectifier

Figure 26 shows a single supply, absolute value, ideal full-wave rectifier with associated waveforms. During positive excursions, the input signal is fed through the feedback network directly to the output. Simultaneously, the positive excursion of the input signal also drives the output terminal (No. 6) of the inverting amplifier in a negative going excursion such that the 1N914 diode effectively disconnects the amplifier from the signal path. During a negative going excursion of the input signal, the CA3140 functions as a normal inverting amplifier with a gain equal to $-R_2/R_1$. When the equality of the two equations shown in Figure 26 is satisfied, the full wave output is symmetrical.

NOTE:

14. "Operational Amplifiers Design and Applications", J. G. Graeme, McGraw-Hill Book Company, page 308, "Negative Immittance Converter Circuits".



$$GAIN = \frac{R_2}{R_1} = X = \frac{R_3}{R_1R_2 + R_3}$$

$$R_3 = \left(\frac{X + X^2}{1 - X}\right)R_1$$

$$\text{FOR } X = 0.5 \quad \frac{5k\Omega}{10k\Omega} = \frac{R_2}{R_1}$$

$$R_3 = 10k\Omega\left(\frac{0.75}{0.5}\right) = 15k\Omega$$

$20V_{P-P}$ Input BW (-3dB) = 290kHz, DC Output (Avg) = 3.2V

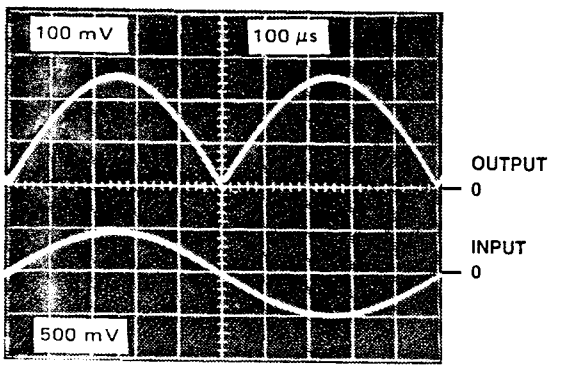


FIGURE 26. SINGLE SUPPLY, ABSOLUTE VALUE, IDEAL FULL WAVE RECTIFIER WITH ASSOCIATED WAVEFORMS

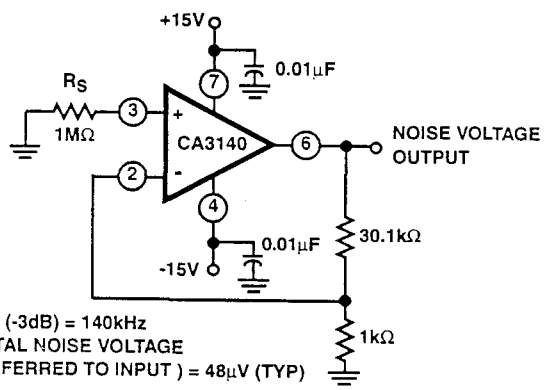


FIGURE 27. TEST CIRCUIT AMPLIFIER (30dB GAIN) USED FOR WIDEBAND NOISE MEASUREMENT

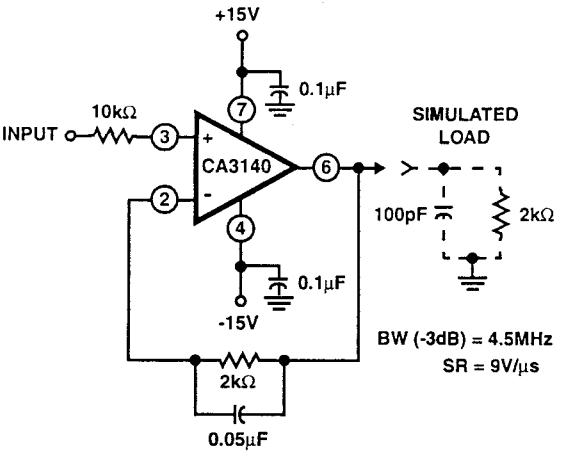
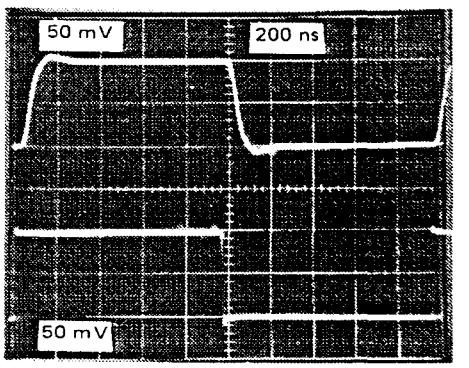
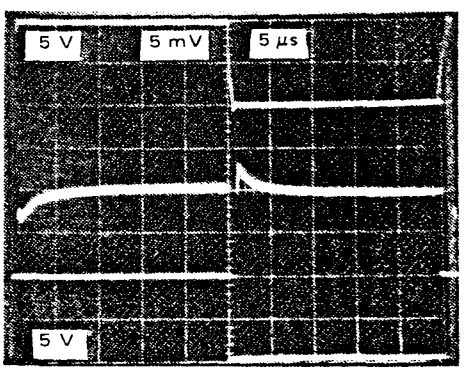


FIGURE 28A. TEST CIRCUIT



Top Trace: Output; 50mV/Div., 200ns/Div.
Bottom Trace: Input; 50mV/Div., 200ns/Div.

FIGURE 28B. SMALL SIGNAL RESPONSE



(Measurement made with Tektronix 7A13 differential amplifier.)

Top Trace: Output Signal; 5V/Div., 5µs/Div.
Center Trace: Difference Signal; 5mV/Div., 5µs/Div.
Bottom Trace: Input Signal; 5V/Div., 5µs/Div.

FIGURE 28C. INPUT-OUTPUT DIFFERENCE SIGNAL SHOWING SETTLING TIME

FIGURE 28. SPLIT SUPPLY VOLTAGE FOLLOWER TEST CIRCUIT AND ASSOCIATED WAVEFORMS

Typical Performance Curves

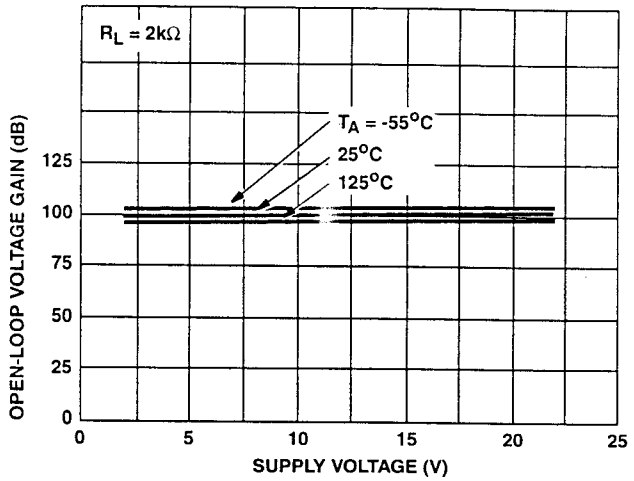


FIGURE 29. OPEN-LOOP VOLTAGE GAIN vs SUPPLY VOLTAGE AND TEMPERATURE

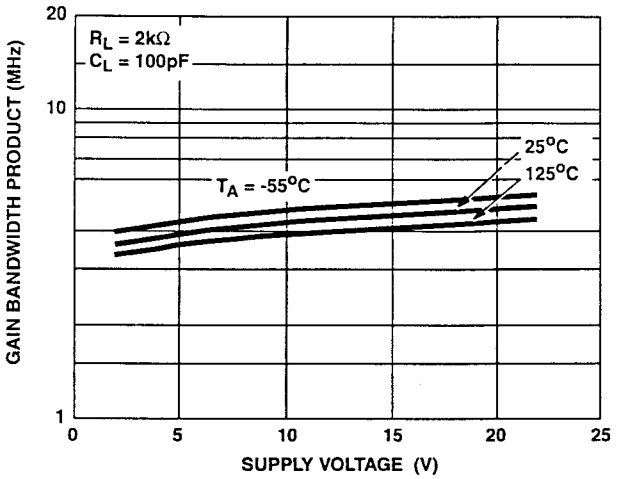


FIGURE 30. GAIN BANDWIDTH PRODUCT vs SUPPLY VOLTAGE AND TEMPERATURE

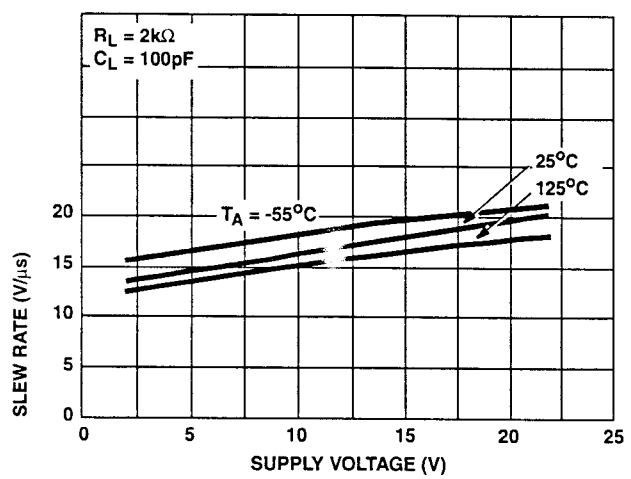


FIGURE 31. SLEW RATE vs SUPPLY VOLTAGE AND TEMPERATURE

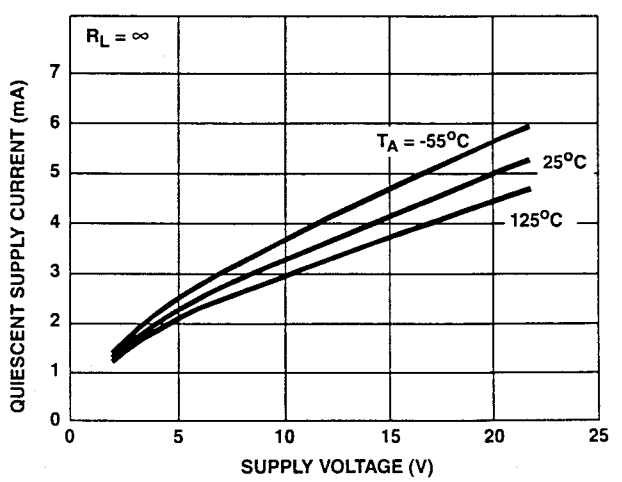


FIGURE 32. QUIESCENT SUPPLY CURRENT vs SUPPLY VOLTAGE AND TEMPERATURE

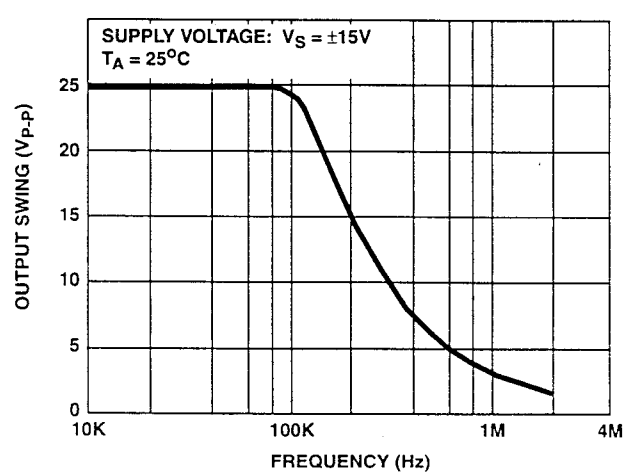


FIGURE 33. MAXIMUM OUTPUT VOLTAGE SWING vs FREQUENCY

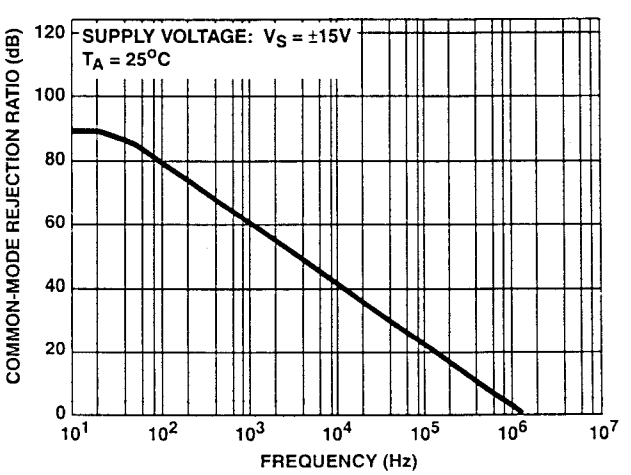


FIGURE 34. COMMON MODE REJECTION RATIO vs FREQUENCY

Typical Performance Curves (Continued)

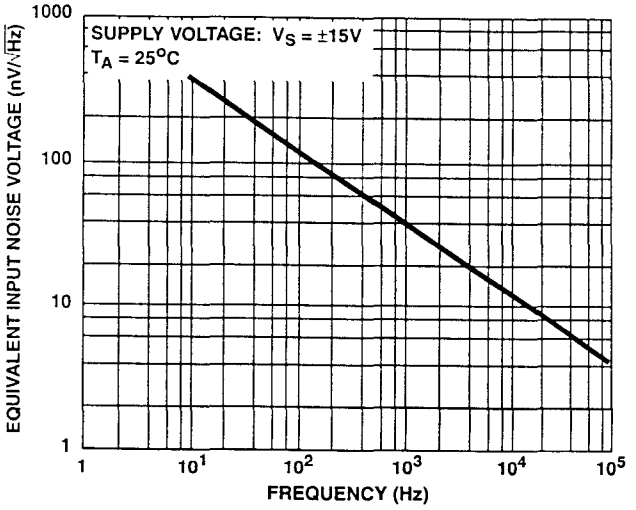


FIGURE 35. EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

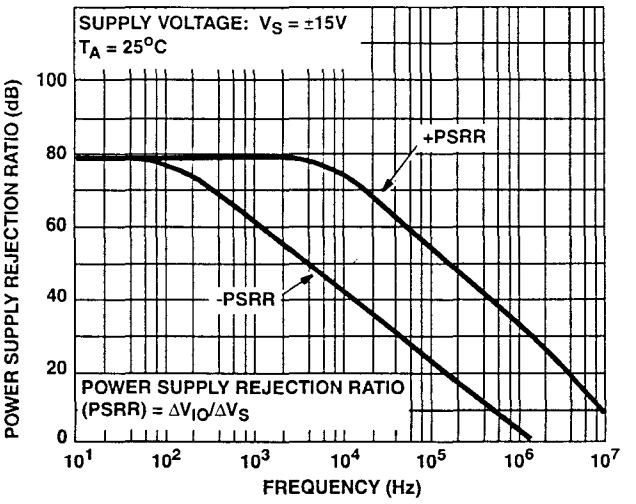
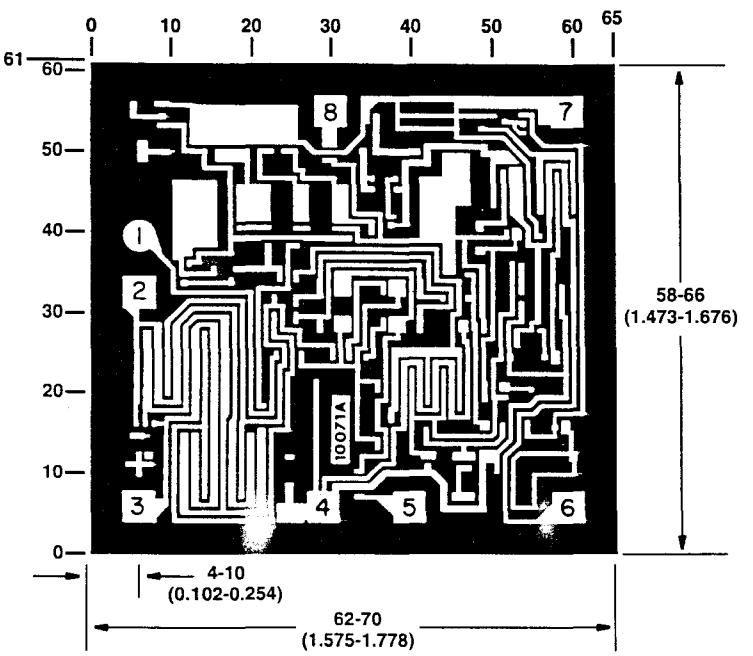


FIGURE 36. POWER SUPPLY REJECTION RATIO vs FREQUENCY

Metallization Mask Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17mm) larger in both dimensions.

APEX MICROTECHNOLOGY

POWER BOOSTER AMPLIFIERS

PB58 • PB58A

HTTP://WWW.APEXMICROTECH.COM (800) 546-APEX (800) 546-2739

FEATURES

- WIDE SUPPLY RANGE — ±15V to ±150V
- HIGH OUTPUT CURRENT —
  - 1.5A Continuous (PB58)
  - 2.0A Continuous (PB58A)
- VOLTAGE AND CURRENT GAIN
- HIGH SLEW — 50V/µs Minimum (PB58)
  75V/µs Minimum (PB58A)
- PROGRAMMABLE OUTPUT CURRENT LIMIT
- HIGH POWER BANDWIDTH — 320 kHz Minimum
- LOW QUIESCENT CURRENT — 12mA Typical
- EVALUATION KIT — See EK50

APPLICATIONS

- HIGH VOLTAGE INSTRUMENTATION
- Electrostatic TRANSDUCERS & DEFLECTION
- Programmable Power Supplies Up to 280V p-p

DESCRIPTION

The PB58 is a high voltage, high current amplifier designed to provide voltage and current gain for a small signal, general purpose op amp. Including the power booster within the feedback loop of the driver amplifier results in a composite amplifier with the accuracy of the driver and the extended output voltage range and current capability of the booster. The PB58 can also be used without a driver in some applications, requiring only an external current limit resistor to function properly.

The output stage utilizes complementary MOSFETs, providing symmetrical output impedance and eliminating second breakdown limitations imposed by Bipolar Transistors. Internal feedback and gainset resistors are provided for a pin-strapable gain of 3. Additional gain can be achieved with a single external resistor. Compensation is not required for most driver/gain configurations, but can be accomplished with a single external capacitor. Enormous flexibility is provided through the choice of driver amplifier, current limit, supply voltage, voltage gain, and compensation.

This hybrid circuit utilizes a beryllia (BeO) substrate, thick film resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is electrically isolated and hermetically sealed using one-shot resistance welding. The use of compressible isolation washers voids the warranty.

TYPICAL APPLICATION

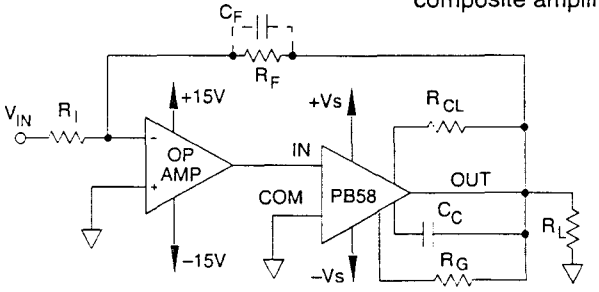
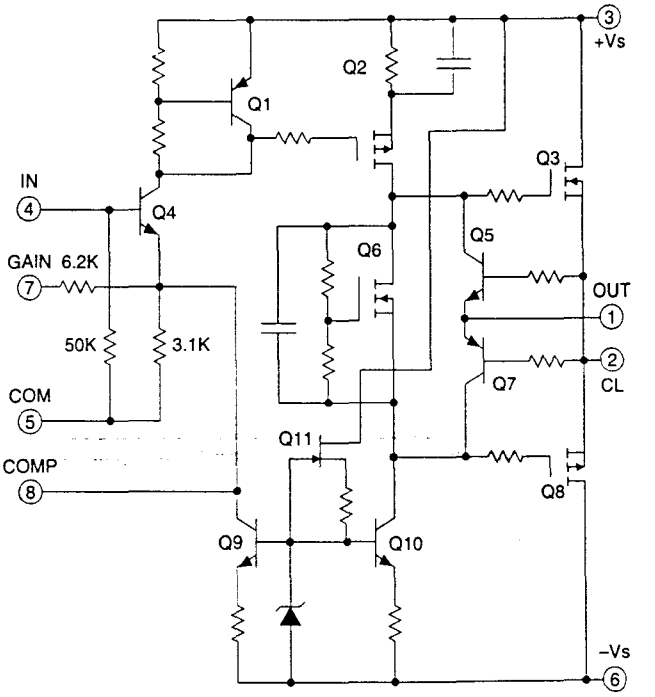
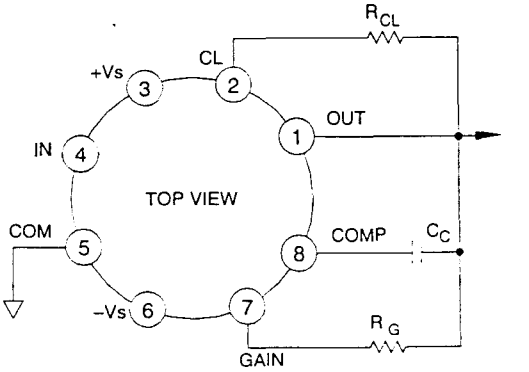


Figure 1. Inverting composite amplifier.

EQUIVALENT SCHEMATIC



EXTERNAL CONNECTIONS



PB58 • PB58A

ABSOLUTE MAXIMUM RATINGS
SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	300V
OUTPUT CURRENT, within SOA	2.0A
POWER DISSIPATION, internal at T_C = 25°C[1]	83W
INPUT VOLTAGE, referred to COM	±15V
TEMPERATURE, pin solder—10 sec max	300°C
TEMPERATURE, junction[1]	175°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

SPECIFICATIONS

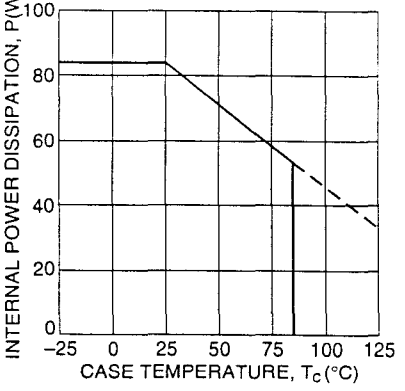
PARAMETER	TEST CONDITIONS[2]	PB58 MIN	PB58 TYP	PB58 MAX	PB58A MIN	PB58A TYP	PB58A MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial			±.75	±1.75		*	±1.0	V
OFFSET VOLTAGE, vs. temperature	Full temperature range[3]		–4.5	–7		*	*	mV/°C
INPUT IMPEDANCE, DC		25	50		*	*		kΩ
INPUT CAPACITANCE			3			*		pF
CLOSED LOOP GAIN RANGE		3	10	25	*	*	*	V/V
GAIN ACCURACY, internal Rg, Rf	A_V = 3		±10	±15		*	*	%
GAIN ACCURACY, external Rf	A_V = 10		±15	±25		*	*	%
PHASE SHIFT	f = 10kHz, AV_{CL} = 10, C_C = 22pF		10			*		°
	f = 200kHz, AV_{CL} = 10, C_C = 22pF		60			*		°
OUTPUT								
VOLTAGE SWING	Io = 1.5A (PB58), 2A (PB58A)	V_S–11	V_S –8		V_S–15	V_S–11		V
VOLTAGE SWING	Io = 1A	V_S–10	V_S –7		*	*		V
VOLTAGE SWING	Io = .1A	V_S–8	V_S –5		*	*		V
CURRENT, continuous		1.5			2.0			A
SLEW RATE	Full temperature range	50	100		75	*		V/µs
CAPACITIVE LOAD	Full temperature range		2200			*		pF
SETTLING TIME to .1%	R_L = 100Ω, 2V step		2			*		µs
POWER BANDWIDTH	V_C = 100 Vpp	160	320		240	*		kHz
SMALL SIGNAL BANDWIDTH	C_C = 22pF, A_V = 25, Vcc = ±100		100			*		kHz
SMALL SIGNAL BANDWIDTH	C_C = 22pF, A_V = 3, Vcc = ±30		1			*		MHz
POWER SUPPLY								
VOLTAGE, $\pm V_S$[4]	Full temperature range	±15[6]	±60	±150	*	*	*	V
CURRENT, quiescent	V_S = ±15		11			*		mA
	V_S = ±60		12			*		mA
	V_S = ±150		14	18		*	*	mA
THERMAL								
RESISTANCE, AC junction to case[5]	Full temp. range, f > 60Hz		1.2	1.3		*	*	°C/W
RESISTANCE, DC junction to case	Full temp. range, f < 60Hz		1.6	1.8		*	*	°C/W
RESISTANCE, junction to air	Full temperature range		30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25	25	85	*	*	*	°C

NOTES: * The specification of PB58A is identical to the specification for PB58 in applicable column to the left.
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF (Mean Time to Failure).
2. The power supply voltage specified under typical (TYP) applies, T_C = 25°C unless otherwise noted.
3. Guaranteed by design but not tested.
4. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively.
5. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
6. $+V_S/-V_S$ must be at least 15V above/below COM.

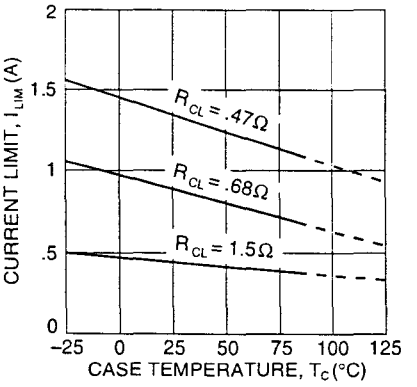
CAUTION The PB58 is constructed from MOSFET transistors. ESD handling procedures must be observed.

The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

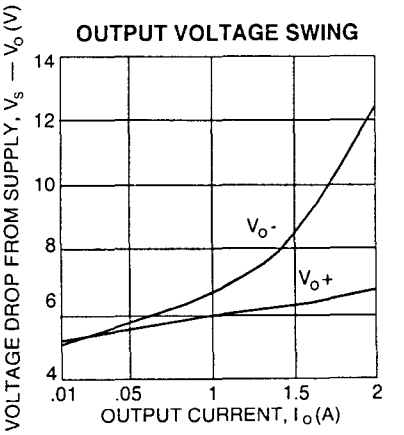
POWER DERATING



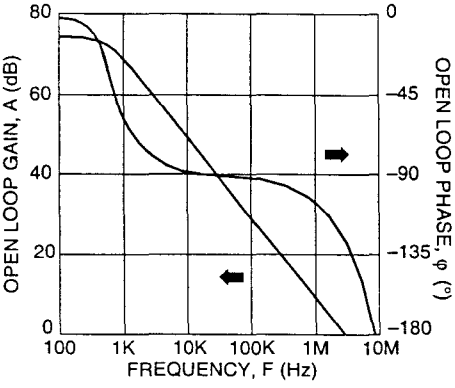
CURRENT LIMIT



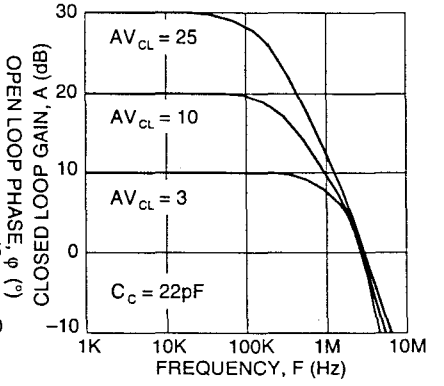
OUTPUT VOLTAGE SWING



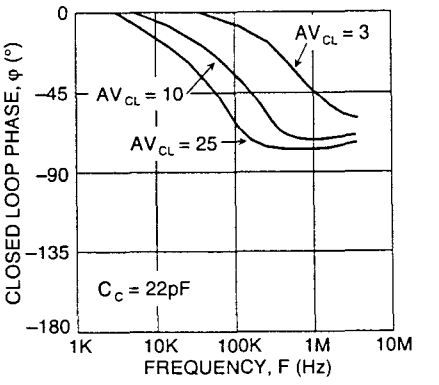
SMALL SIGNAL RESPONSE



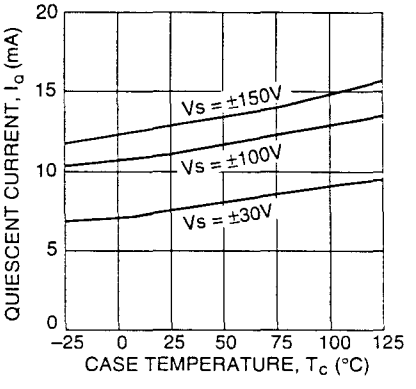
SMALL SIGNAL RESPONSE



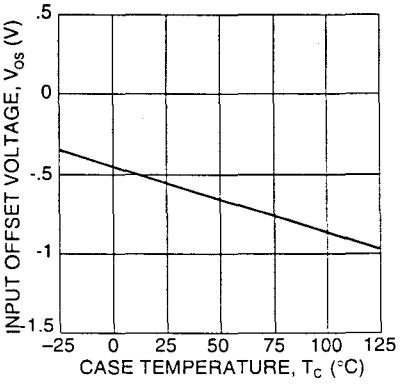
SMALL SIGNAL RESPONSE



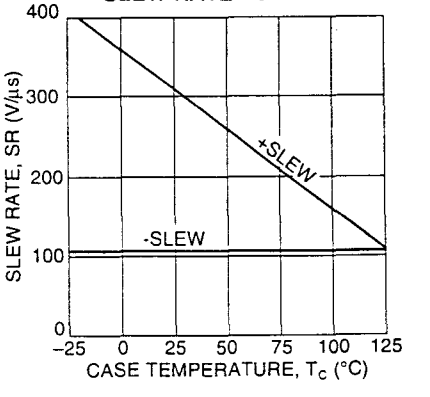
QUIESCENT CURRENT



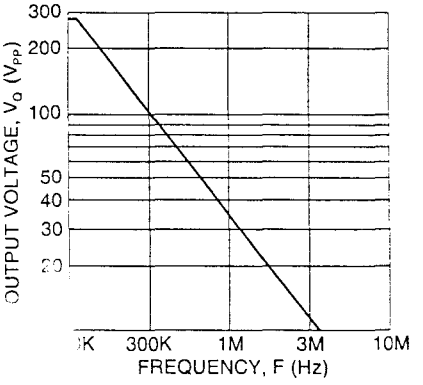
INPUT OFFSET VOLTAGE



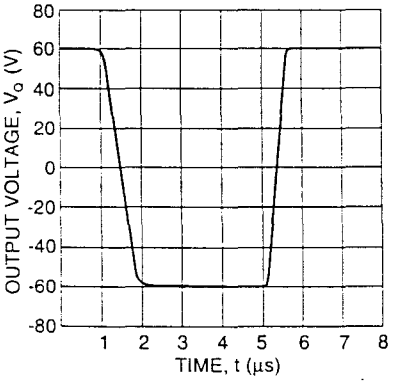
SLEW RATE VS. TEMP.



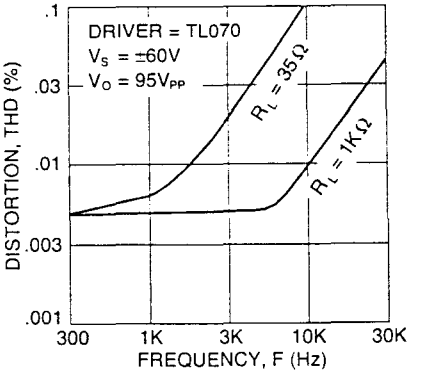
POWER RESPONSE



PULSE RESPONSE



HARMONIC DISTORTION



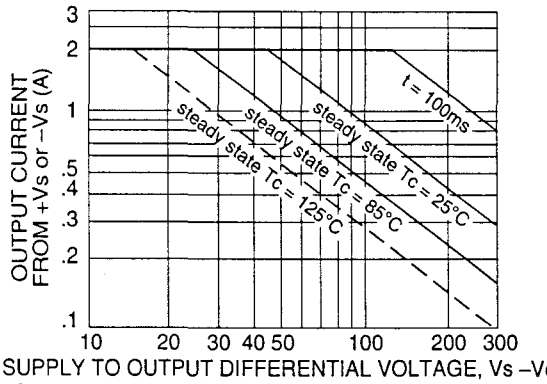
GENERAL

Please read the "General Operating Considerations" section, which covers stability, supplies, heatsinking, mounting, current limit, SOA interpretation, and specification interpretation. Additional information can be found in the application notes. For information on the package outline, heatsinks, and mounting hardware, consult the "Accessory and Package Mechanical Data" section of the handbook.

CURRENT LIMIT

For proper operation, the current limit resistor (R_{CL}) must be connected as shown in the external connection diagram. The minimum value is 0.33Ω with a maximum practical value of 47Ω. For optimum reliability the resistor value should be set as high as possible. The value is calculated as follows: $+I_L = .65/R_{CL} + .010$, $-I_L = .65/R_{CL}$.

SAFE OPERATING AREA (SOA)



NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

COMPOSITE AMPLIFIER CONSIDERATIONS

Cascading two amplifiers within a feedback loop has many advantages, but also requires careful consideration of several amplifier and system parameters. The most important of these are gain, stability, slew rate, and output swing of the driver. Operating the booster amplifier in higher gains results in a higher slew rate and lower output swing requirement for the driver, but makes stability more difficult to achieve.

GAIN SET

$$R_G = [(Av\text{-}1) * 3.1K] - 6.2K$$

$$Av = \frac{R_G + 6.2K}{3.1K} + 1$$

The booster's closed-loop gain is given by the equation above. The composite amplifier's closed loop gain is determined by the feedback network, that is: –Rf/Ri (inverting) or 1+Rf/Ri (non-inverting). The driver amplifier's "effective gain" is equal to the composite gain divided by the booster gain.

Example: Inverting configuration (figure 1) with

R i = 2K, R f = 60K, R g = 0 :

Av (booster) = (6.2K/3.1K) + 1 = 3

Av (composite) = 60K/2K = – 30

Av (driver) = – 30/3 = –10

STABILITY

Stability can be maximized by observing the following guidelines:

1. Operate the booster in the lowest practical gain.
2. Operate the driver amplifier in the highest practical effective gain.
3. Keep gain-bandwidth product of the driver lower than the closed loop bandwidth of the booster.
4. Minimize phase shift within the loop.

A good compromise for (1) and (2) is to set booster gain from 3 to 10 with total (composite) gain at least a factor of 3 times booster gain. Guideline (3) implies compensating the driver as required in low composite gain configurations. Phase shift within the loop (4) is minimized through use of booster and loop compensation capacitors Cc and Cf when required. Typical values are 5pF to 33pF.

Stability is the most difficult to achieve in a configuration where driver effective gain is unity (ie; total gain = booster gain). For this situation, Table 1 gives compensation values for optimum square wave response with the op amp drivers listed.

DRIVER	C_{CH}	C_F	C_C	FPBW	SR
OP07	-	22p	22p	4kHz	1.5
741	-	18p	10p	20kHz	7
LF155	-	4.7p	10p	60kHz	>60
LF156	-	4.7p	10p	80kHz	>60
TL070	22p	15p	10p	80kHz	>60
For: R_F = 33K, R_I = 3.3K, R_G = 22K					

Table 1: Typical values for case where op amp effective gain = 1.

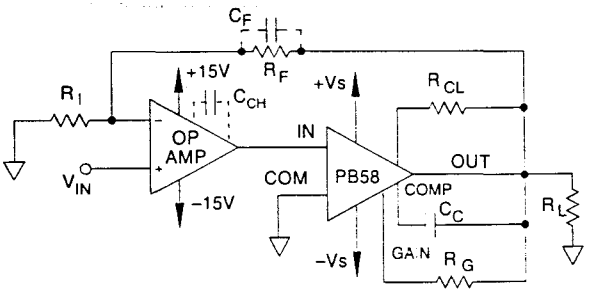


Figure 2. Non-inverting composite amplifier.

SLEW RATE

The slew rate of the composite amplifier is equal to the slew rate of the driver times the booster gain, with a maximum value equal to the booster slew rate.

OUTPUT SWING

The maximum output voltage swing required from the driver op amp is equal to the maximum output swing from the booster divided by the booster gain. The Vos of the booster must also be supplied by the driver, and should be subtracted from the available swing range of the driver. Note also that effects of Vos drift and booster gain accuracy should be considered when calculating maximum available driver swing.

