PROJECT REPORT

"DISPLAYING GRAY SHADES IN PASSIVE MATRIX LCDs USING AMPLITUDE MODULATION"

submitted in partial fulfillment of the requirements of
Visveswaraiah Technological University for the award of degree
of Bachelor of Engineering in Electronics and Communication

2002

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June 15, 2002

Certificate

This is to certify that the project entitled

"Displaying Gray Shades in Passive Matrix LCDs Using Amplitude Modulation"

is a bona fide work of

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Carried out under my guidance at the

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during the period March to June 2002.

This project is in partial fulfillment of the requirement for the award of Bachelor's Degree in Electronics & Communication Engineering for the Visveshwaraiah Technological University during the academic year 2001-2002.

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CERTIFICATE

Certified that the project work entitled "**DISPLAYING GRAY SHADES IN PASSIVE MATRIX LCDs USING AMPLITUDE MODULATION**" is a bonafide work carried out by

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in partial fulfillment for the award of degree of Bachelor of Engineering in of the Visveswaraiah Technological University, Belgaum during the year 20002. It is certified that all corrections/suggestions indicated for Internal Assessment have been incorporated in the Report deposited in the department library. The project report has been approved as it satisfies the academic requirements in respect of Project work prescribed for the Bachelor of Engineering Degree.

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ACKNOWLEDGEMENT

The satisfaction and happiness that accompanies the successful completion of this project would be incomplete without the expression of gratitude and appreciation to the people who made this project possible.

I would like to sincerely thank **Dr.T.N.Ruckmongathan,** Associate Professor, Raman Research Institute for introducing me to the world of LCDs and giving me the opportunity to work on this project. His suggestions and guidance at every stage of implementation were invaluable.

As a grateful beneficiary of the personalized guidance, prompt help and encouragement of my Internal Guide, **Prof. Madhusudhan Rao**, Department of E & C Engineering, M.S.R.I.T., I would like to thank him immensely.

I also humbly thank **Prof.M.S.Sudhi**, Head of the Department, E&C Engineering, M.S.R.I.T for providing me the opportunity to undertake my project at RRI.

I am grateful **to Mr.Panikumar**, **Mr.A.R.Shashidhara**, and **Ms. Pratiti Biswas** for assisting me during various stages of project implementation and patiently quelling my numerous doubts. Their company during my period of work at RRI was truly wonderful.

My thanks to all the **staff & students** of various departments at RRI who have directly or indirectly helped me during the course of this project.

Lastly, I am grateful to my parents and friends for all the support and understanding they have given me.

M.GOVIND

Displaying gray shades in passive matrix LCD using Amplitude modulation

Synopsis

Liquid crystal displays , since their advent , have moved into a variety of applications like notebook computers, palm-tops, mobile phones, digital and video cameras , monitors and televisions. LCD's are well suited for mobile and portable applications wherein low power consumption, low voltage operation ,compactness and good readability are desirable.

A typical LCD panel comprises of an array of pixels (picture elements) arranged in the form of a matrix. Every pixel in the matrix is connected to a row address and column address line .The row and column address lines form a matrix with the individual pixels at their intersections. Since a number of pixels share a common row or column line, a non-linear electro-optic characteristic is essential to drive the pixels to the desired states.

Alt and Pleshko technique (APT) is one of the simplest techniques for addressing matrix displays. APT is a line by line addressing technique . Here the rows are selected in a sequential manner one at a time by a voltage (Vr) and the rest of the rows are grounded. Column voltage depends upon the data to be displayed in the selected row. It has the same polarity as the row select voltage for an off pixel and opposite polarity for an on pixel. APT gives maximum discrimination between on and off pixels (i.e maximum selection ratio). The time required to scan all rows once, is called the frame period. The display must be addressed with a.c fields to ensure long life. The polarity of row and column waveforms are reversed periodically to ensure d.c free operation.
With increased use of multimedia applications, comes the added responsibility of faithful representation of images. This demands capability to control the brightness of pixels over a wide range of gray shades.

Amplitude modulation (AM) can be used in conjunction with APT to generate a large number of gray shades without flicker, as compared to conventional methods like frame modulation or pulse width modulation.

The aim of this project is to display gray shades using the **AM (amplitude modulation) technique** using a 16 x 16 passive matrix display. The drive electronics will be implemented on an EPLD (Erasable Programmable Logic Device) based on FPGA architecture.

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CHAPTER 1

INTRODUCTION

INTRODUCTION

The CRT has been the mainstay of information display technology for a number of applications, but on advances in microelectronics and growing trend in miniaturization in electronics, it has become necessary to have flat panel alternatives to the CRT. CRTs are bulky in size and consume considerable power. One important alternative to the CRT is liquid crystal display (LCDs). The main advantages of LCDs are reduction in size, low power consumption, flexibility in size and format and portability.

LCDs do not emit light but modulate light passing through them depending upon the electric field applied to the pixels. They exhibit non-linear electro-optic characteristics required for displaying images in matrix displays. LCDs are slow responding devices, which are not sensitive to the polarity of the applied electric field. Therefore they exhibit rms response to the applied field. There are two types of matrix LCDs. Active matrix LCDs are popular in the high information content applications. They have an external non-linear element like a diode or thin film transistor associated with each pixel but this makes the fabrication of these displays elaborate and expensive. Passive matrix LCDs utilize the intrinsic nonlinear electro-optic characteristics for addressing the displays. They have a simple construction and offer good display performance.

The objective of this project is to display eight levels of gray shades using Amplitude Modulation technique on a 16x16 passive matrix display.

This report is organized into five chapters. Following this chapter of introduction the second chapter presents an overview of TNLCDs. The third chapter describes the various techniques used for addressing and gray shade generation. The fourth describes the hardware used in implementation of the display system .All results and conclusions and results have been enumerated in chapter five. Appendix–A and Appendix-B provide some mathematical proofs and data sheets for ease of reference.

CHAPTER 2

TNLCDs:

AN OVERVIEW

2.1 BACKGROUND

Liquid crystals are states of condensed matter in which the molecular organizations are intermediate between those of a crystal with a periodic arrangement and of the isotropic liquid in which the arrangement is random. Liquid crystals made of rod-like molecules were discovered by Reinitzer in 1888.

Liquid crystalline materials used in practical displays must be stable in liquid crystalline state over a wide range of temperatures. In this regard two temperatures can be defined for any liquid crystal namely

1) melting point which is the temperature at which the liquid crystal material melts from solid phase to liquid crystalline phase.
2) clearing point which is the temperature at which the liquid crystal material undergoes transition from liquid crystalline phase to isotropic liquid.

For LC mixtures used in displays, melting point ranges from -30° to 0° and clearing point ranges from 60° to 90°.

Nematics are the simplest liquid crystalline materials known. The have a rod like molecular structure and align themselves spontaneously in one direction called the optical axis or the director. Nematics have two dielectric constants one in the direction of the director and the other perpendicular to the director. Dielectric anisotropy is the difference between these two dielectric constants. LC materials with positive dielectric anisotropy align themselves parallel to an external electric field while those with negative dielectric anisotropy align themselves with their director perpendicular to the electric field.

2.2. ELECTRO-OPTIC EFFECT IN TNLCD

The twisted nematic liquid crystal display (TNLCD) cell is made up of two glass plates treated for planer alignment. The cell is assembled such that the direction of alignment in one of the plates is perpendicular to that of the other plate of the cell. This display cell is filled with a NLC mixture having a positive dielectric anisotropy. The liquid crystal molecules confined in the cell form a 90° twisted structure as shown in the fig. 2.1(a). This twisted structure acts like a wave-guide and gradually rotates the plane of polarization of incident light by 90°. Hence, a linearly polarized light incident on the cell emerges linearly polarized in a orthogonal direction when the following conditions are satisfied:-

-The plane of polarization of the incident light is parallel or perpendicular to the director at the surface of the cell; and

-The product of the optical anisotropy (Δn) and the pitch (P) is high as compared to the wavelength of the incident light, where P is four times the thickness of the cell.

The cell is in the unexcited state (OFF) rotates the plane of polarization of the incident light by 90°. Hence; the cell appears-

- dark, when viewed between two polarizers parallel to each other; and
- transparent ,when viewed between two polarizers perpendicular to each other(Fig.2.1(a))

The 90° twist in the cell is lost when a sufficiently strong electric field is applied to the cell (ON). Hence the cell appears –

- transparent between two polarizers ; and
- dark between two polarizers (Fig.2.1(b))

The difference in transmission between the unexcited and the excited states is exploited in TNLCDs. Only one optical mode is excited here by placing the polarizers parallel or perpendicular to the director at the surface of the cell.

BRIGHT

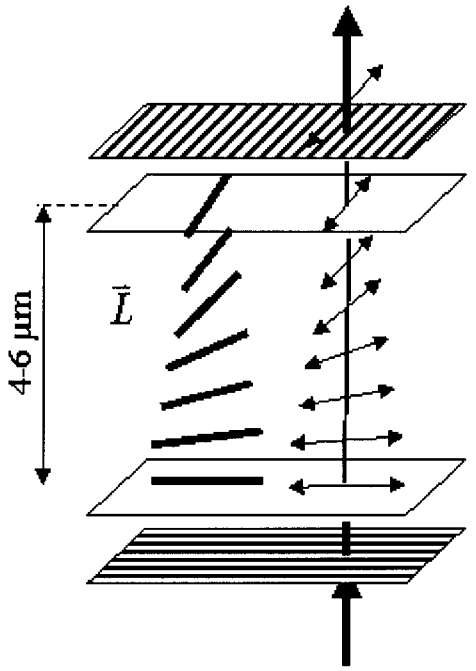


Fig.2.1(a)

DARK

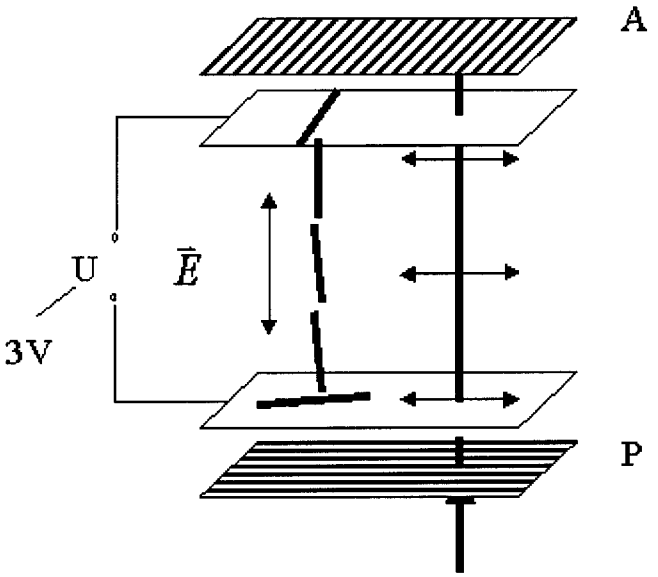


Fig. 2.1(b)

TNLCDs require low power to operate; (~1uw/cm2) since they modulate the incident light and do not emit light. A voltage in the range of 2-5 volts is enough to excite the ON pixels. The TNLCDs can be of the following types:

-Transmissive type with the light source at the back and the observer in the front of the display. This type of display is preferred for use in dark environments;

-Reflective type with both the light source and the observer in the front of the display. A polarizer with a reflector is used at the back of the display. This type of display is suitable for use in well-lit, bright environment.

-Transreflective type with a transreflector instead of reflector at the back. This type of display is suitable for both dark and bright environments. The transreflector allows sufficient light from the back illumination to fall on the display, for a good readability in a dark environment.

The displays can be operated in the following modes:-

-Positive contrast mode with dark symbols against a bright background. This is achieved by placing the top and bottom polarizers perpendicular to each other in TNLCDs; and

-Negative contrast mode with bright symbols against a dark background. This is achieved by placing the top and bottom polarizers parallel to each other in TNLCDs.

A positive contrast mode is preferred in a reflective type of display, while a negative contrast mode is preferred in a transmissive type of display.

2.3.MATRIX LCDs

A matrix display consists of an array of picture elements (pixels) arranged in a rectangular matrix format. The information being displayed depends on the collective state of the pixels. The intersection of a row and a column uniquely defines a pixel. A pixel in the row i and column j is represented by P_{ij}. Figure 2.3 gives the schematic diagram of a matrix display.

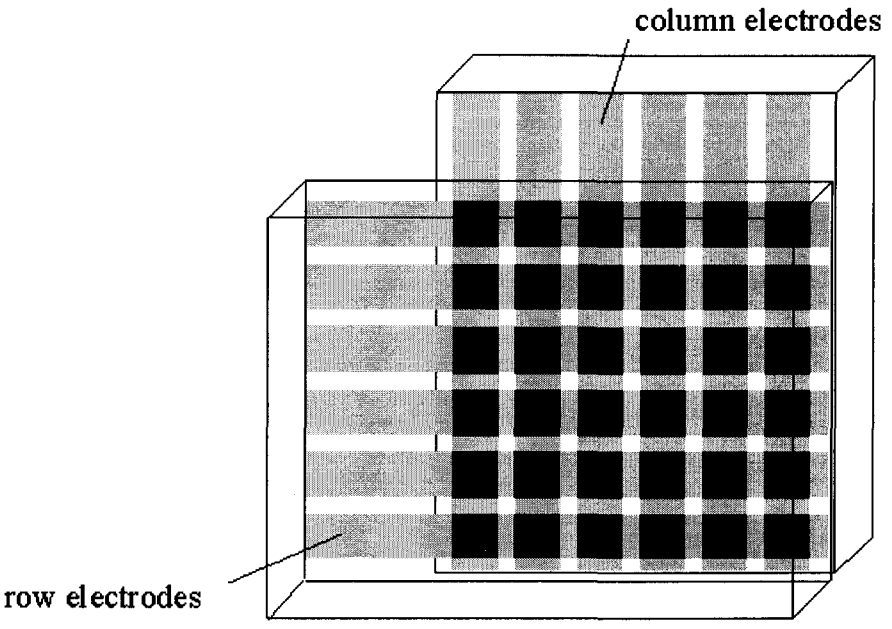


Fig2.2) Passive matrix displays

The size of the pixel determines the resolution of the display. An image can be faithfully displayed if the intensity of each pixel can be controlled independently. In a display with a limited number of pixels, each pixel can be directly connected to the drive electronics (drivers). Hence the pixels are driven to the desired state without affecting the other pixels. This approach is called direct drive or static drive. However, if the number of pixels is very large then it is not possible to connect each pixel separately to the drive electronics. This problem is surmounted by using the matrix display and the technique used for driving such displays is called **matrix addressing** or **multiplexing**. A matrix display with N rows and M columns has N*M pixels while the number of connections is just (N+M). A row address line connects one terminal of the pixels in a given row while a column address line is connected to the other terminal of pixels in a given column. Thus pair of row and column address lines uniquely defines a pixel located at the intersection of these address lines.

The advantages of multiplexing are

1) Reduction in number of external connections
2) Reduction in the number of display drivers
3) Better reliability

The intrinsic non-linear electro-optic characteristics of the LCD are exploited in driving matrix panels with moderate complexity and such displays are called Passive Matrix LCDs (PMLCD). If the matrix is large, a non-linear device like a thin film transistor is incorporated with each pixel. These displays are called Active Matrix LCDs (AMLCD).

The equivalent circuit of a pixel is just a capacitor. The electrical conductance of the liquid crystal is very low and the capacitance of the pixel depends on the dielectric constant of the liquid crystal material, size of the pixel and the cell gap of the display. The two terminals of a pixel are connected to the drive electronics. The response of the liquid crystalline material is independent of the polarity of the electric field. Although LCDs can be driven by a DC (direct current) field, this will result in migration of ionic impurities to the electrodes in the display. Application of a DC field over a long period of time leads to electrochemical reactions near the electrodes resulting in loss of alignment of the molecules and permanent damage to the cell. Hence LCDs are always driven by AC (alternating current) fields to ensure a long life of the display. The shape of the AC field is not very important since the liquid crystals respond relatively slowly to the applied electric field. Hence the instantaneous variations in the electric field are not important for the overall response of a pixel but they contribute to the energy delivered to the pixels. The root-mean-squared (RMS) value of the field determines the state of the pixels as long as the period of the waveform is small compared to the response time of the LCD. While we can drive a pixel with sine, triangular or any other arbitrarily shaped waveforms, square or pulse shaped waveforms are preferred since they are easy to generate. LCDs are low power devices and it is important to make sure that the drive electronics do not consume excessive power. Complimentary Metal Oxide Semiconductor (CMOS) devices are well suited for driving LCDs since they consume very little power to operate.

2.4. ELECTRO-OPTIC RESPONSE OF LCDs

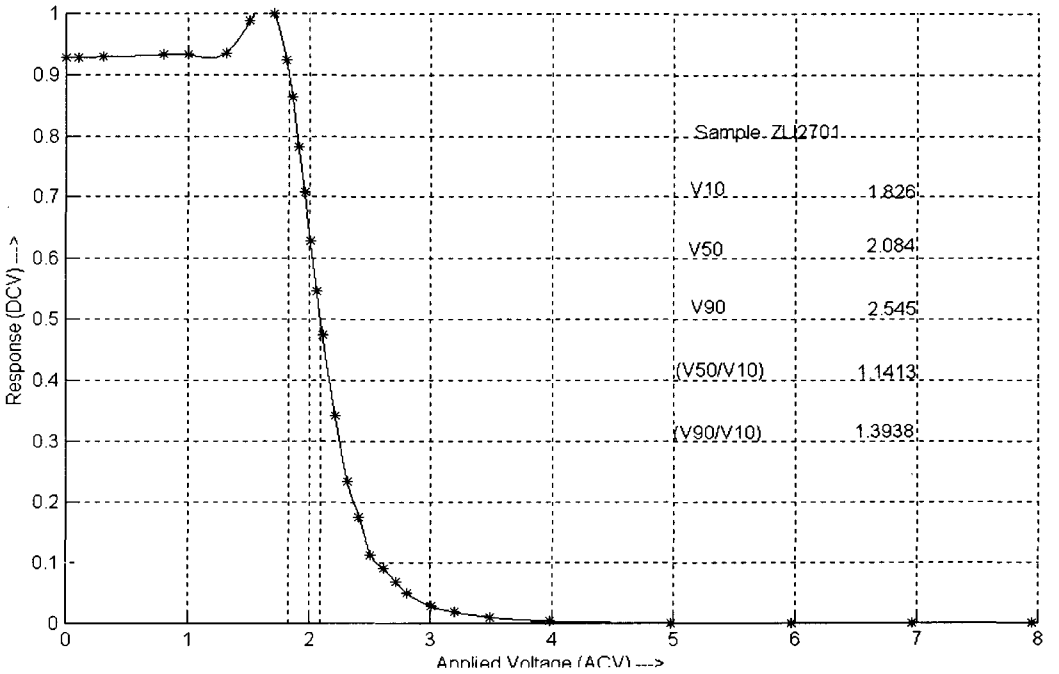


Fig 2.3

The performance of the display in terms of the contrast, gray shades and response time depends on the electro-optic response of the LCD as well as the addressing technique used to drive the display. A non-zero threshold voltage and a sharp electro- optic characteristic are essential in the case of passive matrix LCDs. Fig.2.3 shows the electro-optic response of a TNLC cell.

The threshold voltage (V_{th} or V_{10}) is the voltage below which further change in the optical characteristic (transmission or reflection) is relatively small i.e. the voltage at which the luminance has changed by 10% of the maximum change in luminance.

The saturation voltage (V_{th} or V_{90}) is the voltage above which the change in the optical characteristic is relatively small i.e. the voltage at which the luminance has changed by 90% of the maximum change in luminance.

The sharpness of the electro-optic characteristic (γ) is a measure of the slope of the electro-optic response expressed as $(V_{50}-V_{10})/V_{10}$;

where V_{50} is the voltage at which the luminance has changed by 50% of the maximum change in luminance.

The contrast ratio is defined as a ratio of luminance of a liquid crystal device under bright state to that in dark state under conditions of constant illumination.

Selection ratio is defined as the ratio of the RMS voltage across an ON pixel (V_{ON}) to that of an OFF pixel (V_{OFF}). Selection ratio together with the sharpness determines the contrast in a passive matrix display. The contrast is the ratio of the brightness of the ON pixel to that of the OFF pixel.

2.5 IMPORTANT DISPLAY PARAMETERS

In addressing a passive matrix display, the intrinsic non-linear characteristics of the electro-optic response are exploited. Sharpness of the electro-optic response, angle of viewing, the selection ratio (of the drive technique) and the response times are the important parameters that decide the performance of the display.

The response time of the display is another parameter of interest especially in video applications. The turn ON delay, rise time, turn OFF delay and the fall time determine the response time of the display. Switching times between gray shades should also be considered while displaying graphics. Although all these parameters are necessary to describe the response of the display, often the average of turn ON and turn OFF times is the only parameter that is found in most of the product specifications.

The change in contrast depending on the angle of viewing is another important characteristic of the display. The viewing angle is usually small in a multiplexed display as compared to a display using static drive. The contrast in LCDs also depends upon the quality of polarizers (both transmission as well as the polarization efficiency), reflection of light at the various surfaces in the display cell, light leakage through the area surrounding the pixels and the brightness of the back light if any as well as its uniformity.

2.6 EXPERIMENTAL SETUP FOR ELECRO-OPTIC RESPONSE MEASUREMENT

The experimental setup for measuring the electro optic response is shown in Fig.2.4 It consists of a programmable waveform generator, light source, polarizers, test cell, photo diode and a logging multi-meter.

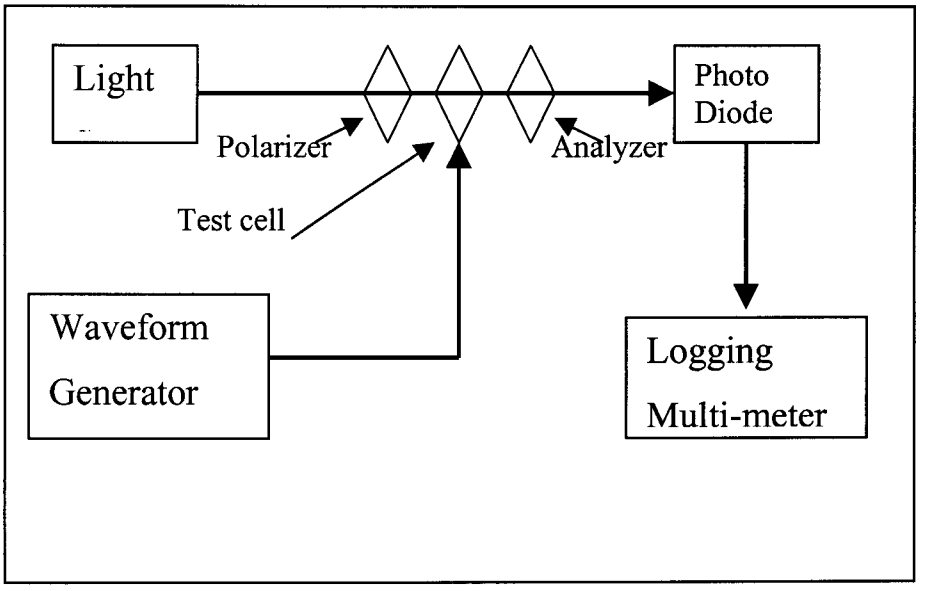


Fig.2.4

The LC cell under test is placed between the polarizer and analyzer. Light from a light source is passed through the cell. The polarizer and analyzer are adjusted for minimum transmission of light through the cell. The light passing through this combination (polarizer, cell, analyzer) is measured using a photodiode to give the equivalent d.c voltage. The voltage across the cell is varied and photodiode reading logged down. A plot of the transmission across the pixel (photodiode reading) versus the rms voltage across the pixel gives the electro-optic response of the LC cell.

CHAPTER 3

ADDRESSING AND GRAY SHADE GENERATING TECHNIQUES

3.1 Addressing techniques

The process of transmitting information to all pixels &activating the appropriate ones called addressing

Addressing techniques can be broadly classified into

1] Direct addressing

2] Line by line addressing

3] Multi-line addressing techniques

Desirable characteristics of addressing techniques.

. Minimisation of crosstalk.

. Ensuring uniforms rms voltage across pixels in identical states.

. Selection ratio should be high for high contrast.

. Selection ratio $R = \frac{V_{on}(rms)}{V_{off}(rms)}$

. Should have dc free operation, thus ensuring long life of display.

. Supply voltage requirement should be low since LCD's are mostly used in portable applications.

3. 2 Alt & Pleshko Technique

Alt & Pleshko discovered this technique in 1974. In this technique the instantaneous voltage across an OFF pixel can far exceed threshold voltage (V_{th}) if the following constraints are satisfied:

- Its duration is small compared to the response time of the display and
- The rms voltage across the pixel is lower than V_{th}

The rows are sequentially selected with row voltage V_r while the unselected rows are grounded. The column voltage depends upon the data to be displayed in the selected row as given below.

- It is Vc i.e. in phase with row select voltage OFF the pixels.
- It is $-V_c$ i.e. out of phase with row select voltage for ON pixels. The instantaneous voltages across the pixel for various combinations of the row and column voltages are given below in the Table 3.1.

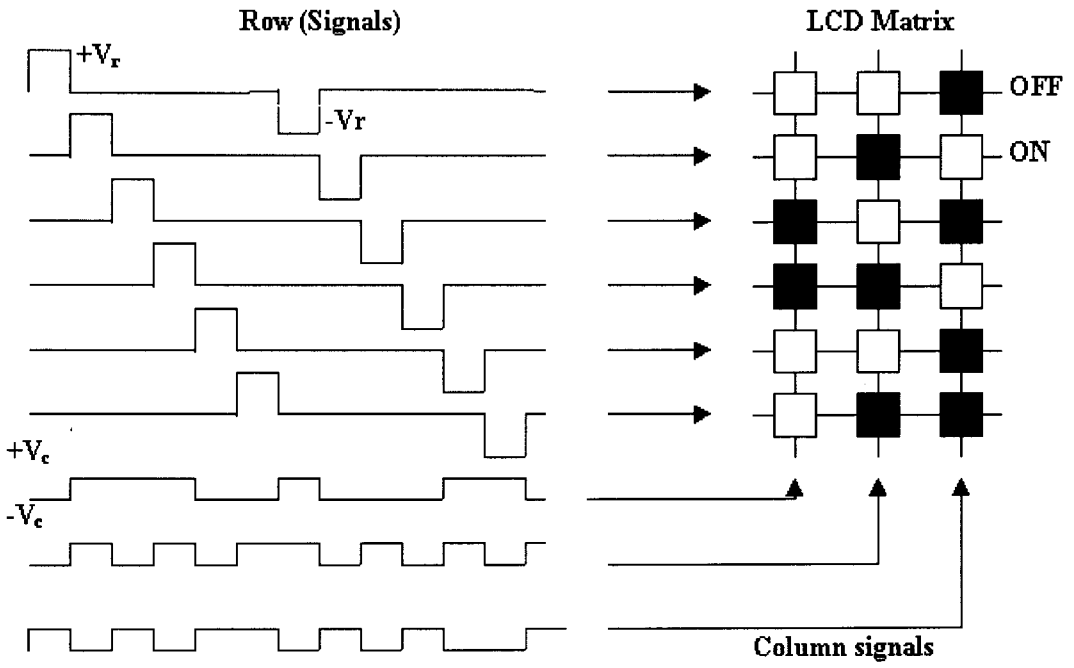
Applied voltages		Resultant voltage across pixels
Row	Column	
+Vr, (-Vr) Selected	*-Vc, (+Vc)* Selected	*Vr+Vc, -(Vr+Vc)* ON pixels
+Vr, (-Vr) Selected	*+Vc, (-Vc)* Unselected	*Vr-Vc, -(Vr-Vc)* OFF pixels
0, (0) Unselected	*-Vc, (+Vc)* Selected	*+Vc, -(Vc)* Both ON and OFF Pixels

Table 3.1 Voltages across pixels in APT

The theoretical background of this technique is as follows:

Consider a matrix with N rows, let V_{on} and V_{off} be the rms voltage OFF and ON pixels the in a particular column, the instantaneous voltage across the selected pixel is (V_r+V_c) for ON state

of (V_r-V_c) for OFF state respectively, while the voltage across the pixel for the rest of $(N-1)$ time intervals will be $\pm Vc$.



Waveforms of APT with polarity reversal after 6 rows

Fig 3.1

A frame is completed when N rows are scanned once. In the analysis, the frame period T is divided into N subintervals of duration 't' and within this interval both the row and column voltages remain constant.

The rms voltage across the ON and OFF pixels are given as follows:

$$V_{on}(rms) = \sqrt{\frac{(Vr+Vc)^2 + (N-1)Vc^2}{N}}$$

$$V_{off}(rms) = \sqrt{\frac{(Vr-Vc)^2 + (N-1)Vc^2}{N}}$$

where N=Number of lines multiplexed in the given display.

Selection ratio (SR) is defined as rms voltage across ON pixel to that across an OFF pixel.

$$Selection\ ratio = \frac{Von(rms)}{Voff(rms)}$$

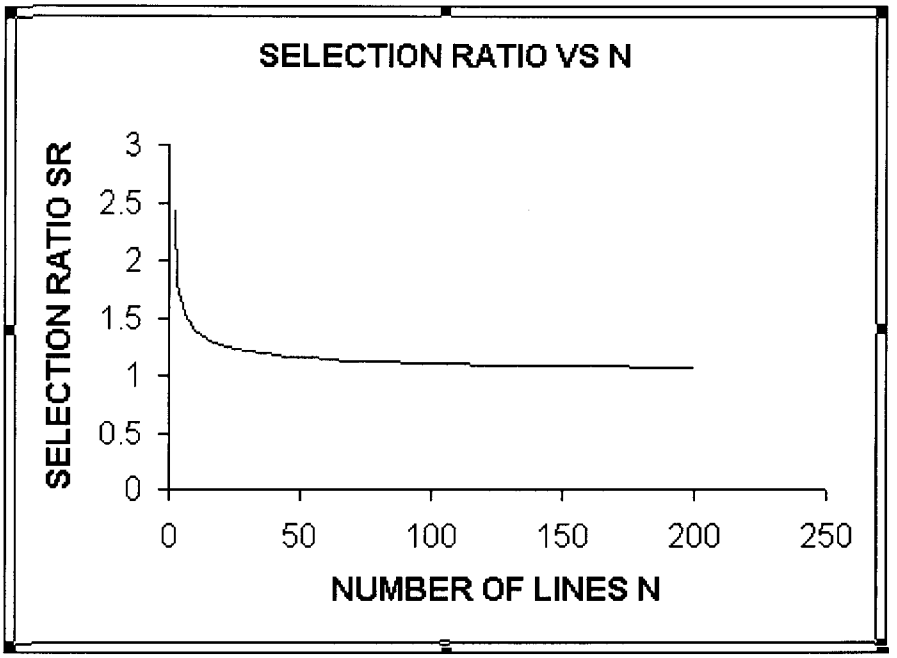
Selection ratio gives a measure of the discrimination achieved between ON and OFF pixel and it is preferable to have a high SR.

Selection Ratio is maximum when $Vr = \sqrt{N}Vc$

$$(SR)max = \sqrt{\frac{\sqrt{N}+1}{\sqrt{N}-1}}$$

From the above equation we see that select ratio is a function of N. The plot of SR versus N is given in the Graph 3.1.

It is seen from the plot that the selection ratio asymptotically approaches one for large N. For N=50, SR=1.1530 and for N=100, SR=1.1055. These voltage margins of 15.30 % are quite narrow. Hence a very steep electro optic characteristic is necessary to achieve adequate contrast in display.



Graph 3.1

Reversing the polarity of the row and the column voltages simultaneously in a periodic manner ensures DC free operation. The polarity maybe changed

- within the row select time or
- after selecting N rows or
- after selecting a few rows

The supply voltage is determined by maximum voltage swing in the addressing waveform. The supply of voltage for the APT is given in the following equation.

$$V_{supply}(APT)=2Vr= 2\sqrt{N}Vc = \left(\sqrt{\frac{4N}{2(1-\frac{1}{\sqrt{N}})}}\right)Vth$$

Alt and Pleshko technique is simple and it achieves maximum Selection Ratio.The maximum instantaneous voltage across any pixel is *(Vr+Vc)*.

3.3Displaying Grey Shades

Bi-level displays where the pixels are either on or off cater to some applications like calculators and watches, however the capability to display intermediate gray shades is desirable in most of the applications.

A pixel can be made to display intermediate gray shades by applying appropriate voltage in the range of threshold voltage to saturation voltage of the LCD used. While this appears simple care must be taken to ensure that changing the voltage for a given pixel does not alter the state of other pixels in a matrix display. The conventional approaches for gray shade generation are pulse width modulation and Frame modulation. The time duration for which a pixel is ON is varied in both these techniques to achieve the required gray shade.

Pulse width modulation

Figure below shows the pulse width modulation. The row select time is divided into $(2^n - 1)$ time intervals to display 2^n gray shades. The width of the pulse becomes smaller and smaller as the number of gray shades are increased. This results in brightness non-uniformity of pixels.

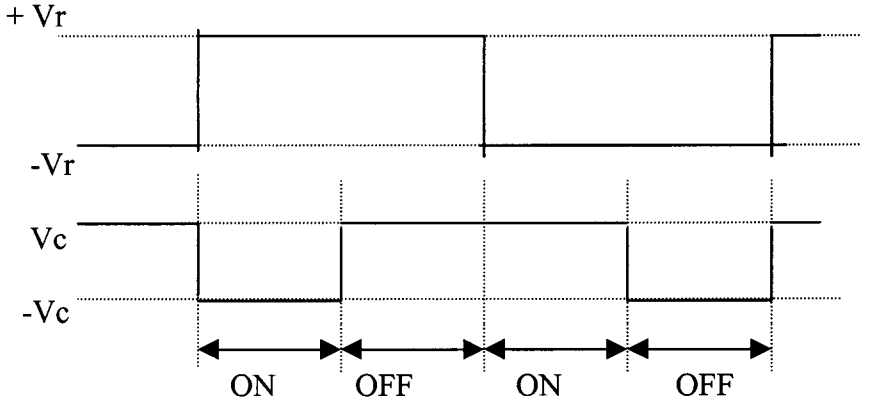


Fig 3.3 Pulse width modulation

Frame modulation

In the case of frame modulation shown in Fig 3.4 the pixels are turned ON or OFF in different frames to obtain the necessary gray shades. In general, $(2^n - 1)$ frames are used to display 2^n gray shades. The display exhibits flicker as the number of gray shades in increased

Frame number	**1**	**2**	.....	**N**
Pixel state	**On/ off**	**On/ off**		**On/ Off**

Fig 3.4 Frame modulation for generating gray shades in LCD.

In the conventional addressing techniques 2n time intervals are necessary for d.c free operation. In the general (n+1) gray shades can be displayed when the row select time is divided in to n time intervals in pulse width modulation. Both these techniques thus have practical limit of about eight gray shades. An alternative approach to display gray shade is Amplitude modulation

3.4.Amplitude Modulation

In the conventional addressing techniques, the amplitude of the column voltage is the same (Vc) while sign or polarity of this voltage is changed depending on the data. This is necessary to make rms voltage across the pixels to be independent of the data displayed in a column. In amplitude modulation the amplitude of the column voltage is varied in

accordance with the data. The principle of amplitude modulation applied to conventional Alt and Pleshko technique is outlined below.

Amplitude modulation (for APT)

The amplitude of the column voltage maybe changed to change the rms voltage across a pixel, however this results in a change of rms voltage across all the pixels in that column.

Let kVc be the column voltage applied to display the gray shade in a pixel (the value of k ranges from –1 to 1). The rms voltage will depend on the value k and is given by

$$V_{pixel} = \sqrt{\frac{(Vr - k \cdot Vc)^2 + (N-1)Vc^2}{N}}$$

The rms voltage across another pixel in the same column is given by,

$$V_{coloumn} = \sqrt{\frac{(Vr - Vc)^2 + (k \cdot Vc)^2 + (N-2)Vc^2}{N}}$$

From the above expression it is clear that the rms voltage across all other pixels in the same column has also changed. There is thus the need to choose a voltage scheme such that rms voltage is changed only for the desired pixel and does not affect the other pixels in the unselected rows.

This is possible when the row select time is split into two time intervals. The column voltages for these two time intervals are different as given below:

$$V_{c1}, V_{c2} = (k \pm \sqrt{(1 - k^2)})Vc$$

When these two column voltages are used the rms voltage of the pixel in the selected row is changed without altering the rms voltage across the other pixels. The second term in the

above equation i.e. $\sqrt{(1-k^2)}$ can be thought of as correction term which is added in one time slot and subtracted in the other. The rms voltage across the pixel is now given by:

$$V_{pixel} = \sqrt{\frac{(Vr - Vc_1)^2 + (Vr - Vc_2)^2 + (N-1)Vc^2}{2N}}$$

This reduces to the following expression,

$$V_{pixel} = \sqrt{\frac{Vr^2 - 2 \cdot k \cdot Vr \cdot Vc + NV_c^2}{2N}}$$

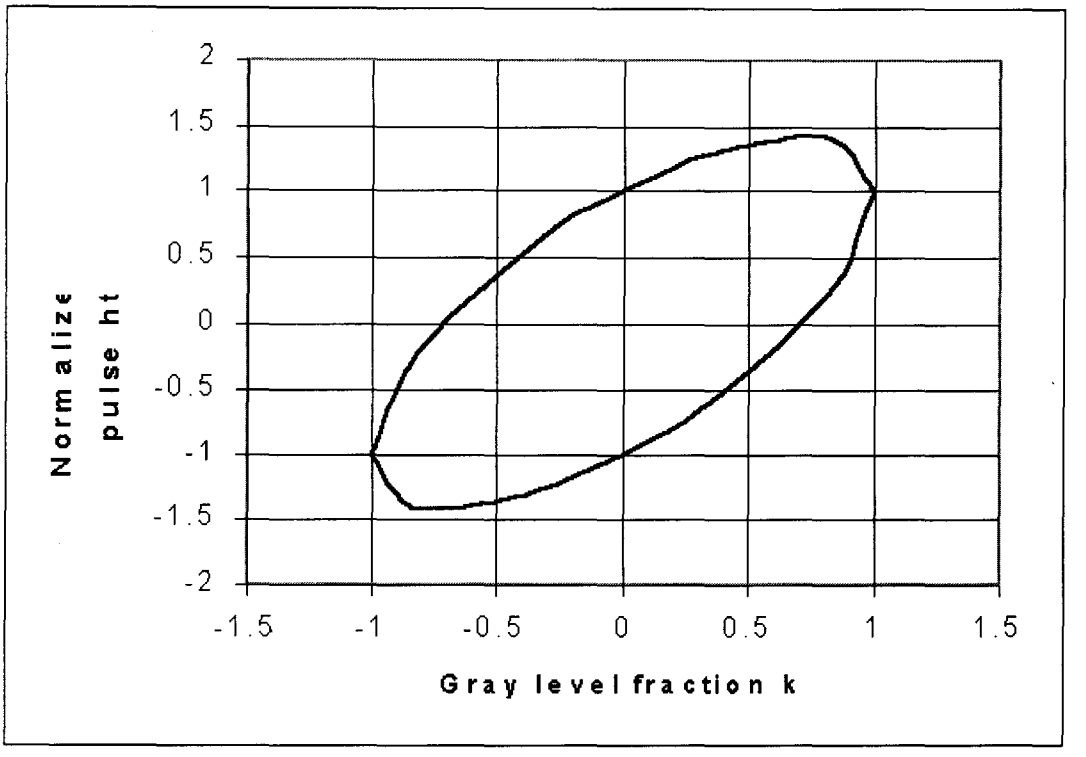
Note: Detailed mathematical derivation provided in section 2 of Appendix -A

From the above expression it is clear that the rms voltage across a pixel can be varied to achieve gray shades. The value (k =-1) corresponds to the fully ON state while (k =+1) corresponds to fully **OFF.** Assigning appropriate values for k within this range can generate any intermediate gray shade. The column voltage has many voltage levels and an analog type column driver is necessary.

The main advantage of this technique is that large number of gray shades can be displayed without any flicker, since only two frames are necessary to complete the cycle.

All the schemes listed in (which are modifications of scheme1) can be used to achieve similar results. For the project schemes 3 and 4 have been considered. This is because in these schemes the net dc voltage error to be corrected during polarity reversal frame is much smaller.

A combination of schemes 3 and 4 has been used to achieve a reduction in hardware. Scheme 3 is used for the first four gray shades while scheme 4 has been used for the remaining gray shades. The various voltage levels to be applied during various time slots are given in tables 3.3 and 3.4



Graph 3.2

Graph 3.2 shows a plot of normalized column voltages versus gray level fraction k for values of k ranging between –1 and 1.

Scheme	Slot 1		Slot 2	
	Row voltage	Column voltage	Row voltage	Column voltage
1	$+Vr$	$(k+\sqrt{1-k^2})Vc$	$+Vr$	$(k-\sqrt{1-k^2})Vc$
2	$+Vr$	$(k-\sqrt{1-k^2})Vc$	$+Vr$	$(k+\sqrt{1-k^2})Vc$
3	$+Vr$	$(\sqrt{1-k^2}+k)Vc$	$-Vr$	$(\sqrt{1-k^2}-k)Vc$
4	$+Vr$	$(-\sqrt{1-k^2}+k)Vc$	$-Vr$	$(-\sqrt{1-k^2}-k)Vc$

Table 3.2

SCHEME 3			Frame 1		Frame2 (polarity reversal)	
	k	$(1-k^2)^{1/2}$	Slot1	Slot2	Slot1	Slot2
Row voltage			$+\sqrt{N}$	$-\sqrt{N}$	$-\sqrt{N}$	$+\sqrt{N}$
Col voltage			$(1-k^2)^{1/2}+k$	$(1-k^2)^{1/2}-k$	$-(1-k^2)^{1/2}-k$	$-(1-k^2)^{1/2}+k$
000	-1	0	-1	1	1	-1
001	-(5/7)	0.6998	-0.0144	1.4141	0.0144	-1.4141
010	-(3/7)	0.9035	0.4750	1.3320	-0.4750	-1.3320
011	-(1/7)	0.9897	0.8470	1.1326	-0.8470	-1.1326
100	+(1/7)	0.9897	1.1326	0.8470	-1.1326	-0.8470
101	+(3/7)	0.9035	1.3320	0.4750	-1.3329	-0.4750
110	+(5/7)	0.6998	1.4141	-0.0144	-1.4141	0.0144
111	+1	0	1	-1	-1	1

TABLE 3.3

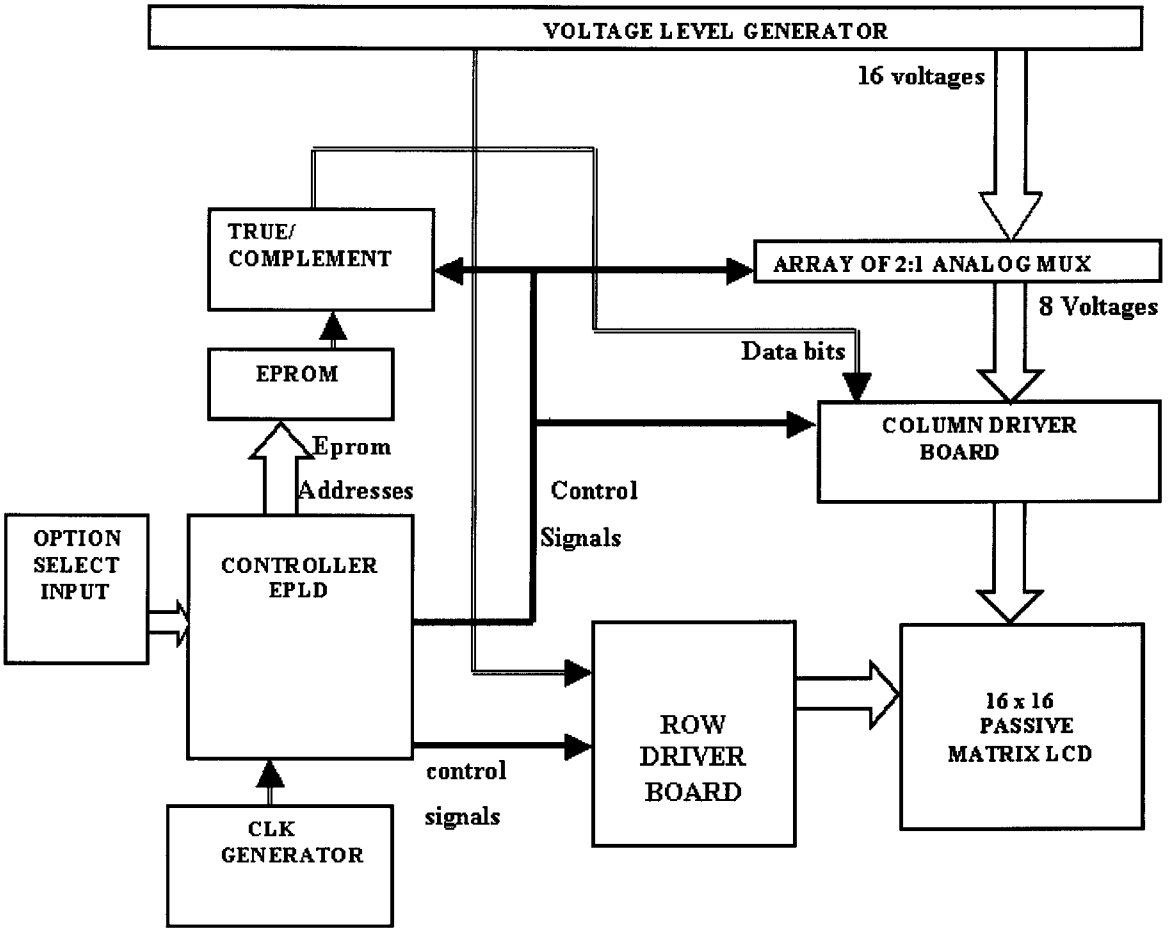
SCHEME 4			Frame 1		Frame2 (polarity reversal)	
	k	$(1-k^2)^{1/2}$	Slot1	Slot2	Slot1	Slot2
Row voltage			$+\sqrt{N}$	$-\sqrt{N}$	$-\sqrt{N}$	$+\sqrt{N}$
Col voltage			$(1-k^2)^{1/2}+k$	$(1-k^2)^{1/2}-k$	$-(1-k^2)^{1/2}-k$	$-(1-k^2)^{1/2}+k$
000	-1	0	-1	1	1	-1
001	-(5/7)	0.6998	-1.4141	0.0144	1.4141	-0.0144
010	-(3/7)	0.9035	-1.3320	-0.4750	1.3320	0.4750
011	-(1/7)	0.9897	-1.1326	-0.8470	1.1326	0.8470
100	+(1/7)	0.9897	-0.8470	-1.1326	0.8470	1.1326
101	+(3/7)	0.9035	-0.4750	-1.3329	0.4750	1.3320
110	+(5/7)	0.6998	0.0144	-1.4141	-0.0144	1.4141
111	+1	0	1	-1	-1	1

TABLE 3.4

NOTE: All entries in tables are referenced to a column voltage (Vc) of 1 volt.

CHAPTER 4

HARDWARE IMPLEMENTATION



BLOCK DIAGRAM OF DISPLAY SYSTEM

FIG4.1

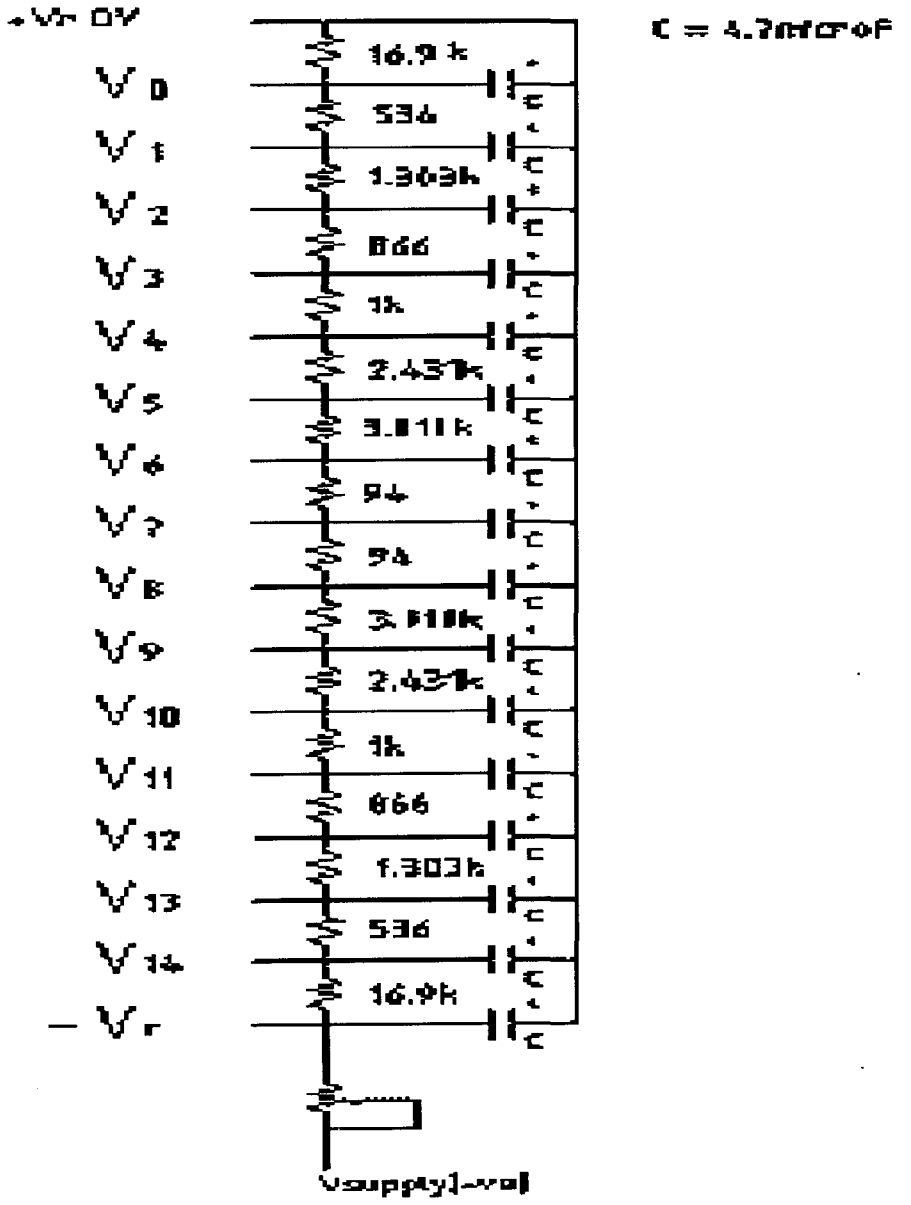


Fig.4.2a. Voltage level generator

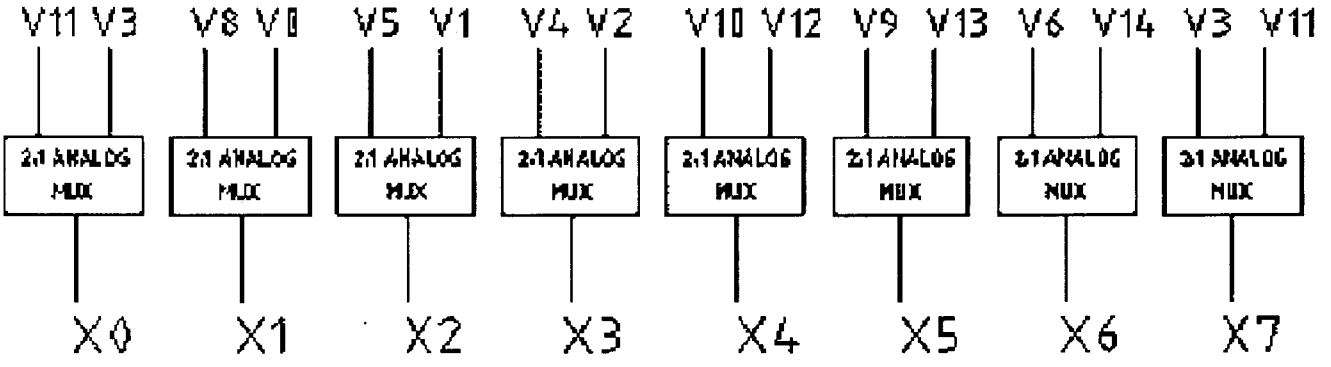


Fig.4.2b Array of 2:1 analog multiplexers

4.1 VOLTAGE LEVEL GENERATOR

The voltage levels necessary for the amplitude modulation technique are generated using a resistive divider network. This enables changing absolute values of the row and column voltages without changing their relative ratios. Optional buffer amplifiers may be used for row and column voltages to reduce the source impedance and is especially useful in large displays. Capacitors are incorporated to provide stability of voltages. Accuracy of resistor values is vital to achieve properly spaced gray shades. A potentiometer is used at the lower end of the resistive divider network to adjust the contrast of the display.

4.2 ARRAY OF 2:1 MULTIPLEXERS

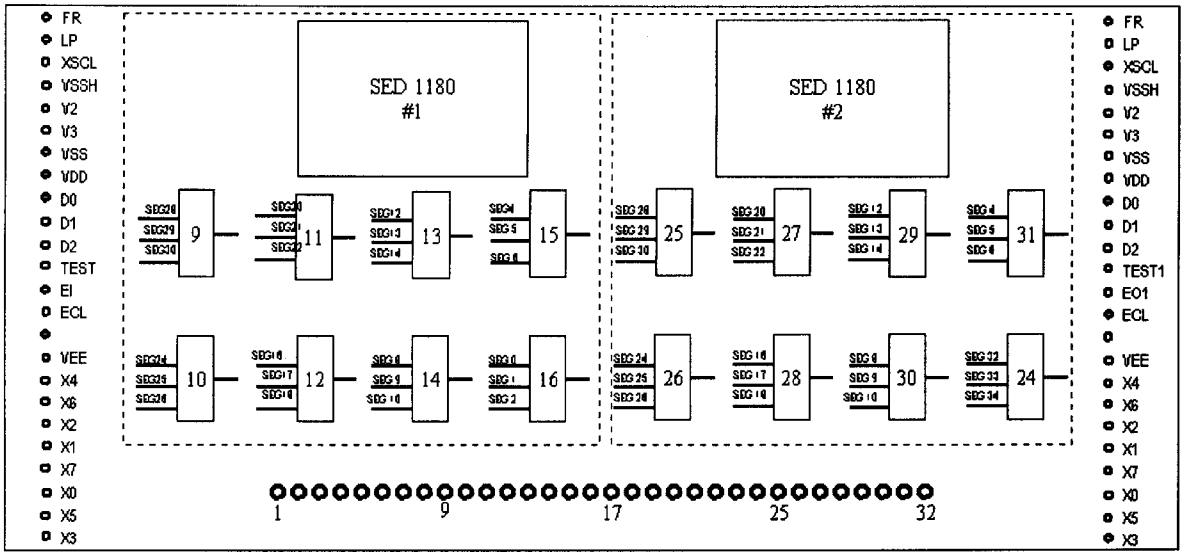
It is seen that at any given instant of time only a definite eight of the sixteen column voltage levels are required i.e. eight voltages are required during the first slot and rest of the eight voltages during the second time slot. This is achieved by feeding the sixteen voltages derived from the voltage level generator to an array of eight 2:1 analog multiplexers. The eight multiplexer outputs are fed to the column driver board. The controller generates the signal to control the select inputs of the 2:1 multiplexer.

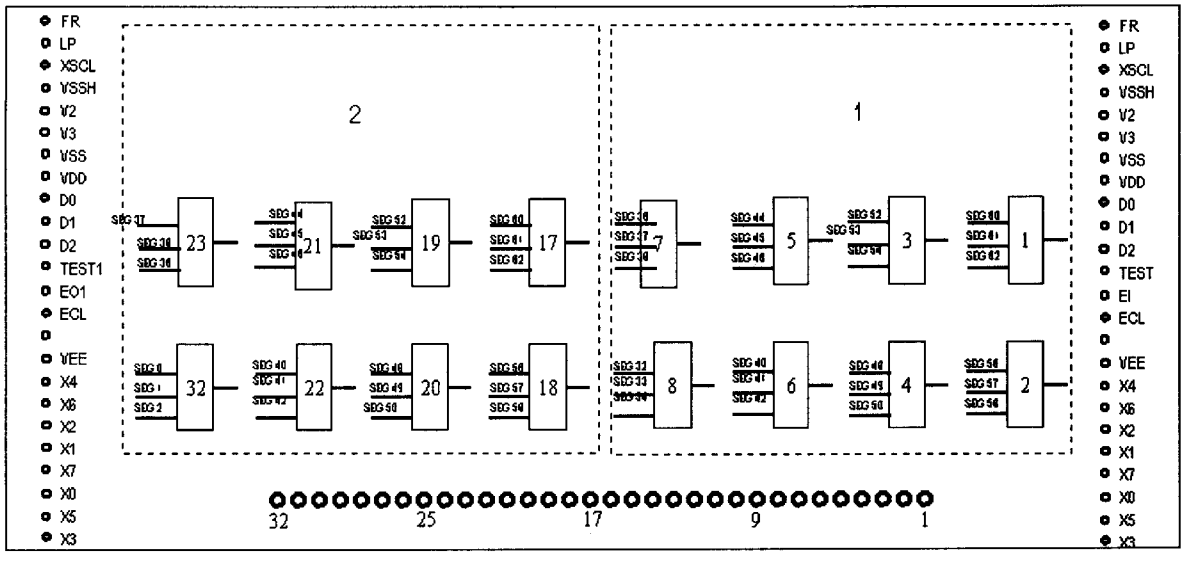
4.3 EPROM

The information to be displayed may be taken from any memory source. In the project, image information to be displayed is stored in an EPROM. Intel's 2764A(8k x 8) EPROM has been used. A minimum of 3 bits is required to distinguish between eight gray shades. Thus for a given image each pixel in the matrix display will have a 3-bit code corresponding to the gray shade to be displayed on it. The 3-bit information for each pixel in the display is stored in a separate byte. Since there are (16 x 16)= 256 pixels, 256 bytes are required to store data for a single frame.

The design requires complementing of data bits (in alternate frames) to obtain d.c free operation. This is achieved by ex-oring the data bits from the EPROM with a control signal that alternates between as high and low levels as required.

4.4.COLUMN DRIVER BOARD





Column Driver (SED1180):

Column Drivers need to handle higher data rates than row drivers, as they have to accept complete row of data within a row select interval. So SED1180 is provided with four data inputs for faster operation. The architecture of the column driver is given in fig 4.2

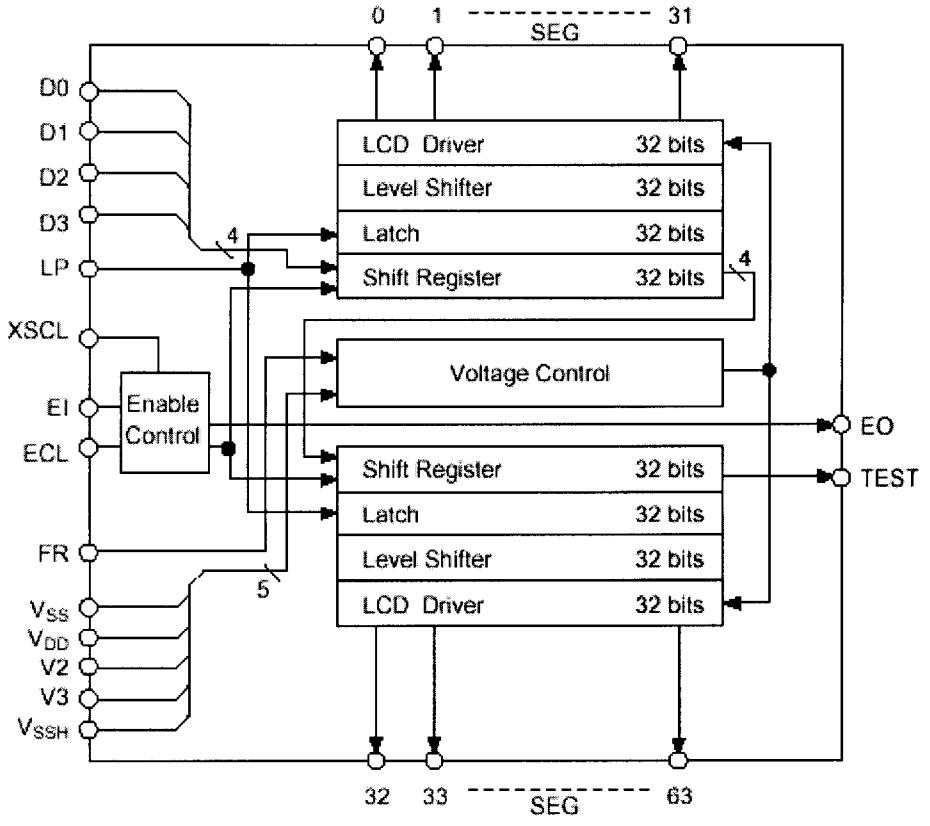


Fig 4.3

The logic power supply for the column driver is +5v(V_{DD}) and GND (V_{SS}). The LCD drive voltages are V_{DD}, V2, V3 and V_{SSH}.

The various input and control signals to the driver are:

Shift clock for data (XSCL)

The EPSON column driver can shift in a nibble of data in parallel. Only three bits are used for eight gray levels, one bit is left unused. Three bits of column data is shifted into the shift registers at the negative edge of the shift clock. There are 16 x16x 2 sets of three bit data for each frame. So for a refresh rate of 50 frames/second we require [50x16x 16x2] sets of three-bit data. Therefore the frequency of XSCL is [50 x 16 x16 x 2] i.e. 25.6kHz. This signal is derived from pin11 of astable multi-vibrator (CD4047). The R and C components of 4047 are calculated using the formula:

$$f = 1/(4.4 \cdot R \cdot C)$$

Assuming the value of C=33pf, we get R=270k

Latch Pulse (LP)

After shifting one complete row of data of 16 columns, a latch pulse initiates the parallel transfer of 16 sets of three bit data into a latch register. Since the data is to be latched after sixteen shift clocks, the LP frequency will be =25.60kHz/16=1.60kHz.This signal is derived from the control circuitry.

Enable Input (EI)

The clock (XSCL) is enabled when this pin is high, and disabled when low. This input is maintained high.

ECL

It is clock pulse for propagation of enable signals. This input signal is generally used in driving large displays where a number of column drivers are to be cascaded. For our operation, only a single column driver is sufficient and hence this pin is grounded.

Phase control or polarity control (FR)

The FR signal is used for DC free operation. The latch outputs set the switch positions in the analog multiplexers to apply the appropriate voltages to column electrodes simultaneously during a select interval. Although the driver can support four different voltage levels, only

two output levels are available at any time. The FR selects which of the two levels are to be switched as shown in the TABLE 4.1.

DATA	*FR* (Polarity Signal)	COLUMN VOLTAGE
H	L	V_{DD}
H	H	V_{SSH} (Ref)
L	L	V_2
L	H	V_3

Table 4.1

With polarity control being separately provided FR is maintained at logic high level.

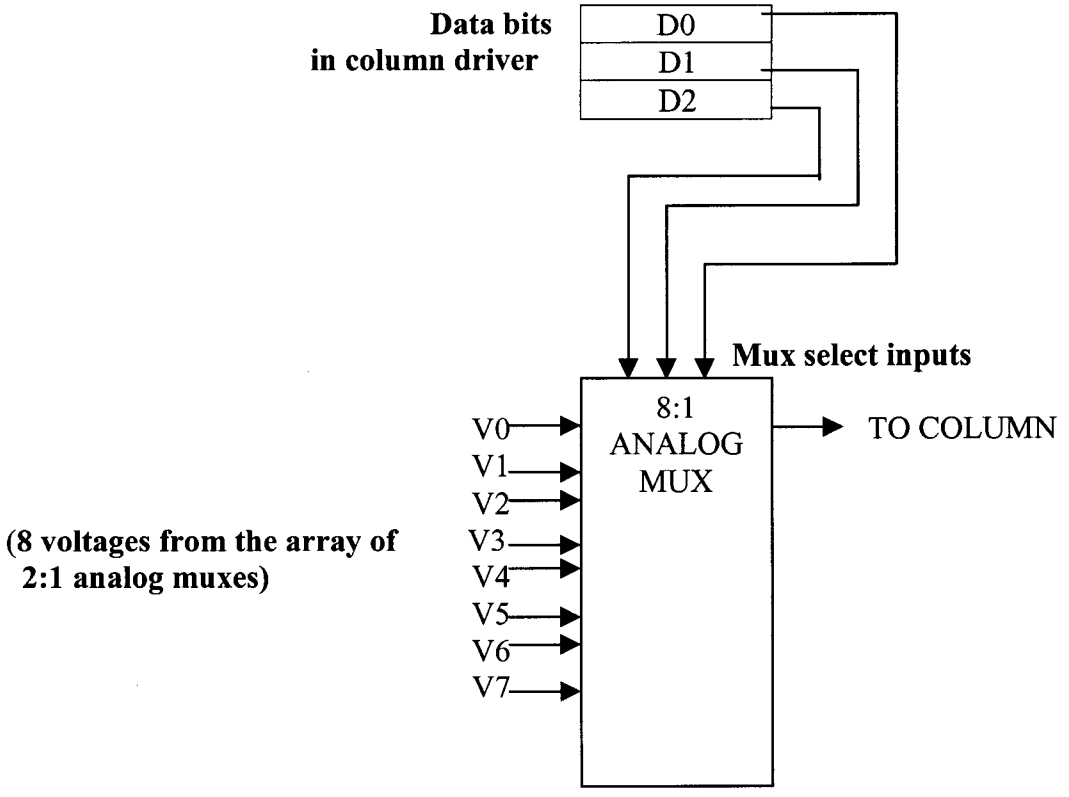


Fig 4.4

8:1 analog multiplexers are the other components that constitute the column driver board. One 8:1 analog multiplexer is necessary for each column of the display. CD4051-single 8:1 analog multiplexer IC package is used.

The eight analog voltages are derived from the array of eight 2:1 multiplexers and are common to all the multiplexers. The select bits for each multiplexer are obtained from the three-bit set that has been shifted in parallel into the column driver. These bits are available at the driver outputs and are fed to the select inputs of the mux as indicated in fig.4.4. Depending on the select inputs one of the eight analog voltages is connected to the respective column line.

4.5 ROW DRIVER BOARD

Row Driver (SED1190)

The rows are used for scanning display, with one row selected at one time. The row driver need not handle the high data rates, so they can work at lower frequencies than the corresponding row column drivers. Hence the complexity of the driver is greatly reduced .The APT has three voltage levels in the row waveforms taking the DC free operation into consideration. The internal block diagram of SED1190F shown in the fig 4.5

The four voltage levels are V_{DD}, V_1, V_4, V_{SSH} and the logic power supply is +5v (V_{DD}) and (V_{SS}). Some of the controls required for the row driver are

Data Inputs (DI)

This serial data input should go high only once at the start of every frame so that it is shifted in by the shift clock for row driver (YSCL) and thereafter shifted 16 times to sequentially scan of 16 rows one at a time. The controller generates signal for DI.

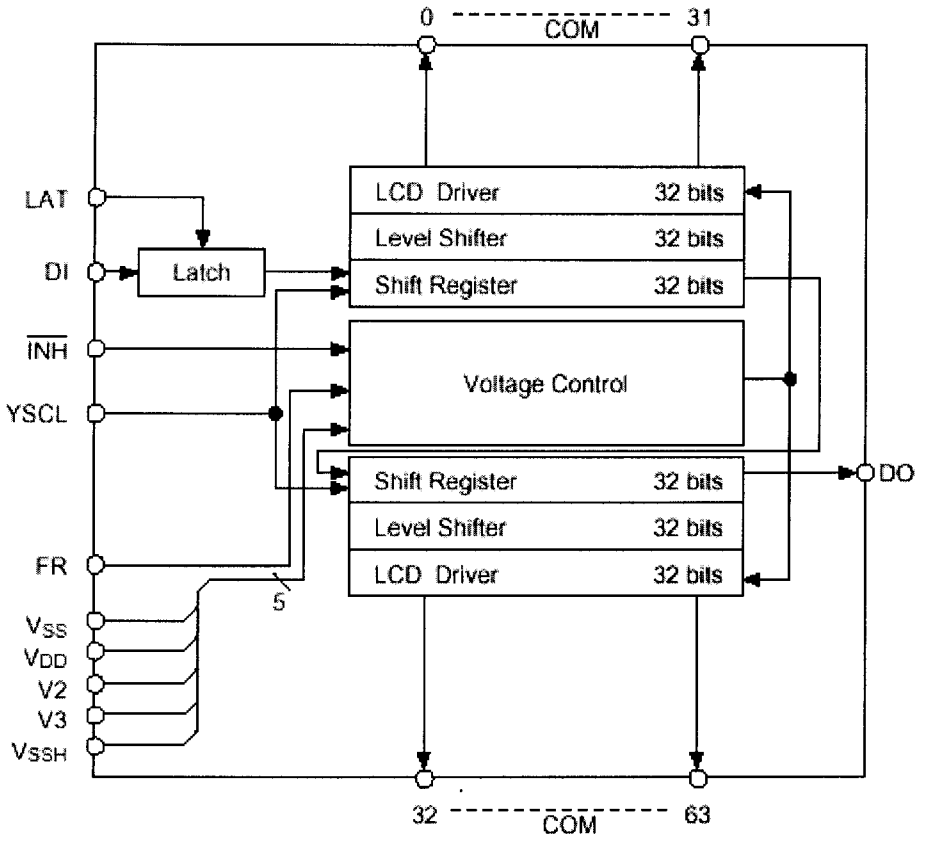


Fig 4.5

Serial data shift clock (YSCL)

DI is shifted through the driver on the falling edge of this signal. The operation of the YSCL should be such that a particular row is scanned when the data required for that particular row is present at the column driver output. Hence the latch pulse (LP) of the column driver and YSCL should be synchronized. The frequency of this shift clock is the same as that as that of LP i.e. 1.6khz. The controller generates signal for YSCL.

Frame Signal (FR)

The FR signal is used for DC free operation. The latch outputs set the switch positions in the analog multiplexers to apply the appropriate voltages to row electrodes simultaneously during a select interval. Although the driver can support four different voltage levels, only

Two output levels are available at any time. The FR selects which of the two levels are to be switched as shown in the TABLE 4.2

INH (active low)	FR	DI	Outputs
H	H	H	V_{SSH}
H	H	L	V_{DD}
H	L	H	V_1
H	L	L	V_4
L	X	H	V_1
L	X	L	V4

Table 4.2

4.6) THE CONTROLLER

The controller has been designed using VHDL and implemented on an EPLD. The various aspects involved in controller design in VHDL can be summarized as follows-

Decomposing the system into suitable blocks or modules with one or more levels of hierarchy.

Developing code for each of these modules.

Code compilation followed by simulation and functional verification of each module.

Integration of lower level modules into higher-level blocks, which are then configured to yield the system.

At various stages in the design process one may need to back track and iteratively repeat the design flow process for purposes of debugging, modification and optimization.

The pof file corresponding to the final system after testing may be downloaded onto a suitable EPLD package for hardware implementation.

a) Objectives of design

To design a general purpose lcd controller capable of

-generating control signals for line-by line addressing of variable sized matrix displays.

-generating control signals required for AM method of gray shade generation for variable sized matrix displays.

-generating EPROM addresses for given matrix size.

-providing a flexible phase control options.

b) The platform

The MAX-PLUS design package from ALTERA has been used as the platform for all the VHDL coding, debugging and simulation involved in the project.

c) Capabilities of the developed design

Taking into account the above listed objectives the following design has been developed, successfully tested and implemented on chip. In its final form it requires 96 logic cells and has been fit on ALTERA's EPM5128JC-1 chip (appendix). The pin out diagram of the programmed EPLD is given in fig 4.5.

The functions of the various in/out pins and their respective functions are listed below.

1) MROW (7) to MROW (0)-8 pins

MCOL (7) to MCOL (0)-8 pins

These two 8 bit select inputs lines enable the user to select matrix displays of any size ranging from a single pixel with a single row and column to matrix displays with a maximum of 256 rows and 256 columns (256x256).

Any particular size can be selected by applying the binary equivalent of the number of rows/columns along the respective 8-bit select lines.

2) CLKA

This is the input master clock with respect to which all internal operations are synchronized.

3) EPROM (16)-EPROM (0)

These sixteen output lines carry EPROM addresses.

4) STR

The negative edge of this strobe pulse enables both latching and shifting row data and latching of column data.

5) OPT, MODE

These select inputs specify different modes of operation.

OPT	MODE	Size catered to	Comments
0	x	Variable	Generates addresses for one image of variable size specified by mrow(7-0) and mcol(7-0). Provides a pulse after each frame for external address generating circuitry.
1	0	16 x 16	Dedicated 16x 16 operation. Allows presetting of address bits eprom(11)-eprom(8)for scanning of single images with variable starting addresses.
1	1	16 x16	Dedicated 16x 16 operation. Allows presetting of address bits eprom(11)-eprom(8)for scanning of upto 16 different images successively with starting addresses 0000h.

Table 4.3

6) RINZ

This signal provides the frame marker or frame synchronization pulse .It is fed to the serial input DI of the row driver chip.

7) EXR

This signal is used to complement the data bits during alternate frames before shifting into the column driver

8) ROWINV

This signal is used to polarity inversion in alternate frames

9) RESET

This is an asynchronous system reset pin. It can be configured as power on reset by connecting it as shown in fig 4.6

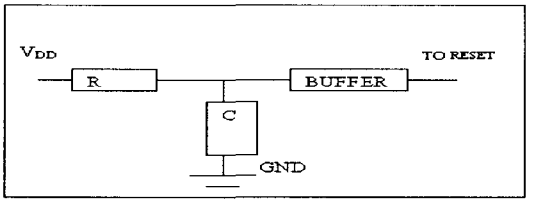


Fig. 4.6 Power on reset configuration

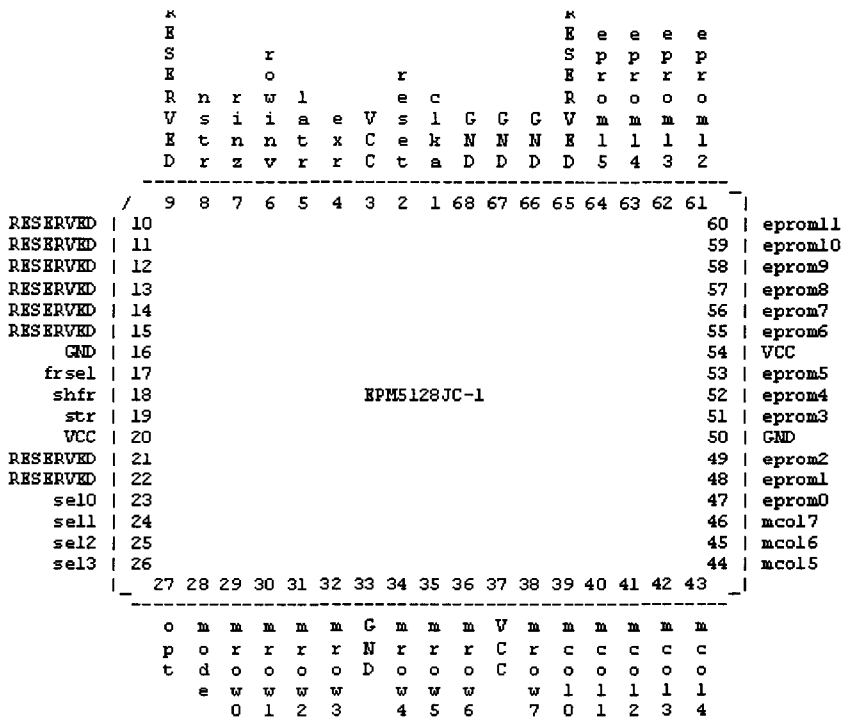


Fig 4.7 Pin out diagram of programmed EPLD

CHAPTER 5

RESULTS AND CONCLUSIONS

RESULTS

This chapter discusses the various results obtained during course of the project, conclusions inferred from them and also various improvements possible.

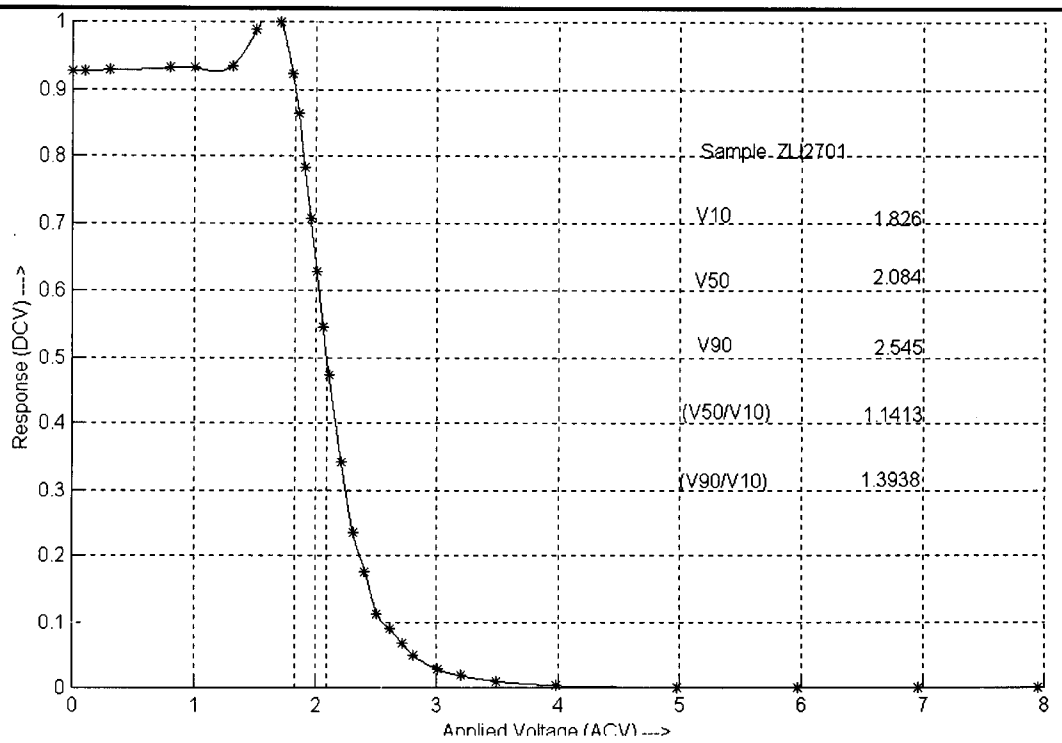
The electro-optic response of the liquid crystalline material used in the 16 x 16 matrix display namely ZLI2701 has been measured as shown in fig 5.1. The threshold voltage reading estimated from the electro-optic characteristic has been used for all supply voltage calculations.

The hardware implementation has been successfully realized to -

Display pictures (patterns) with eight distinct gray shades on a 16x16 matrix display.

The RMS voltage generated across a pixel for each of the eight gray shades has been measured using a RMS meter for different supply voltages. The readings are tabulated in the following pages.

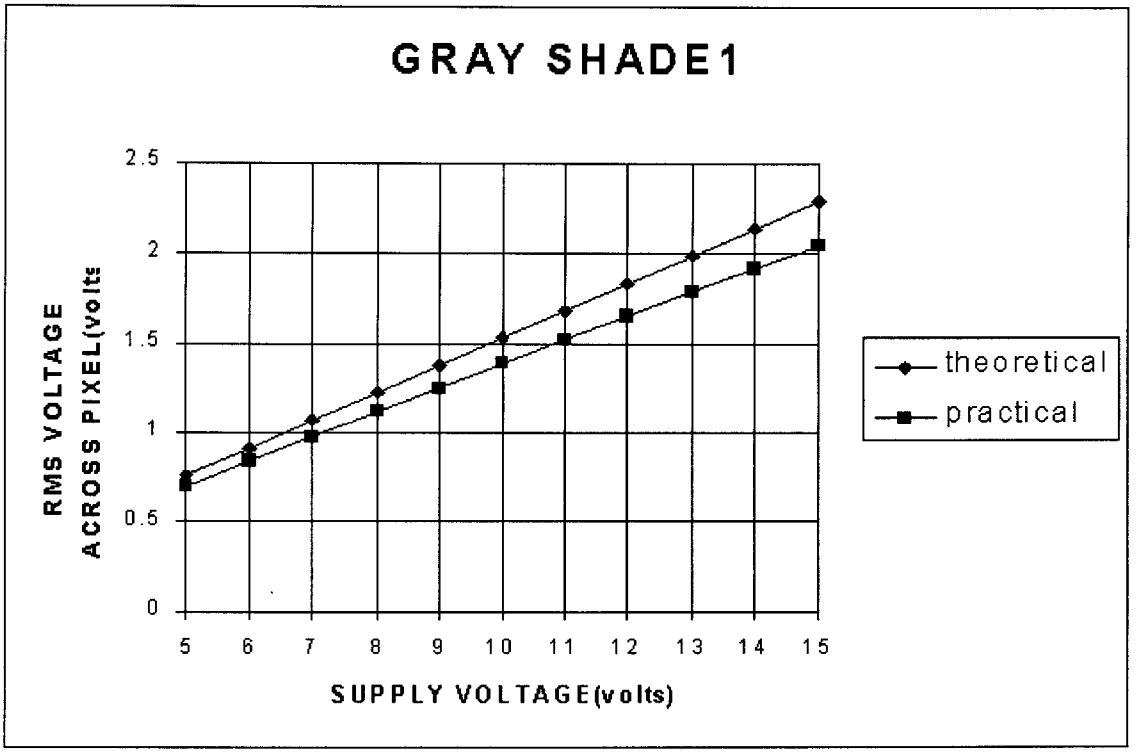
A few sample simulation waveforms of the controller are shown in Fig 5.1 and 5.2



Graph 5.1 electro-optic response of zli2701 test cell

Applied rms voltage (v)	Measured dc Voltage (v)
0	5.198
0.0994	5.195
0.3016	5.201
0.7981	5.220
0.9973	5.222
1.3079	5.236
1.5072	5.508
1.7059	5.563
1.8050	5.174
1.8550	4.876
1.9040	4.466
1.9540	4.090
2.0050	3.680
2.055	3.270
2.1040	2.894
2.2070	2.240

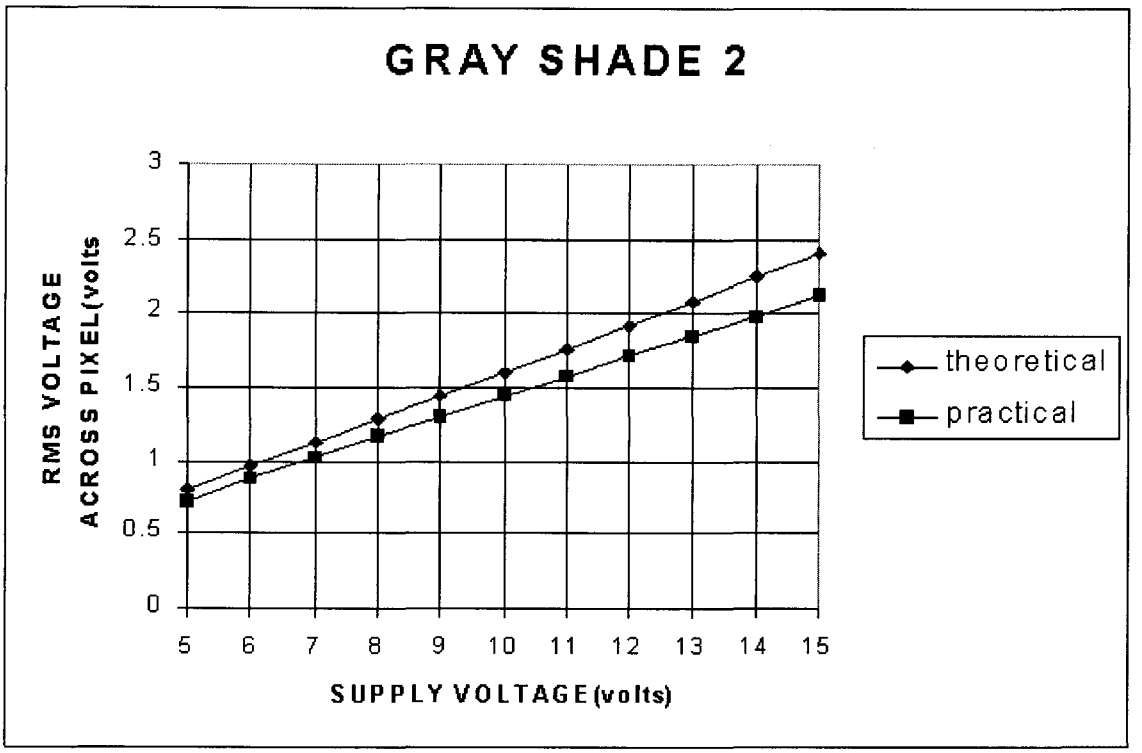
Applied rms voltage(v)	Measured dc voltage(v)
2.307	1.691
2.406	1.3943
2.506	1.0761
2.608	0.9637
2.709	0.8452
2.807	0.7561
3.01	0.6485
3.194	0.5999
3.49	0.5582
3.988	0.5241
4.983	0.5119
5.97	0.5109
6.964	0.5081
7.953	0.5099
8.947	0.5121
9.946	0.5108



Graph 5.2

GRAY SHADE 1:

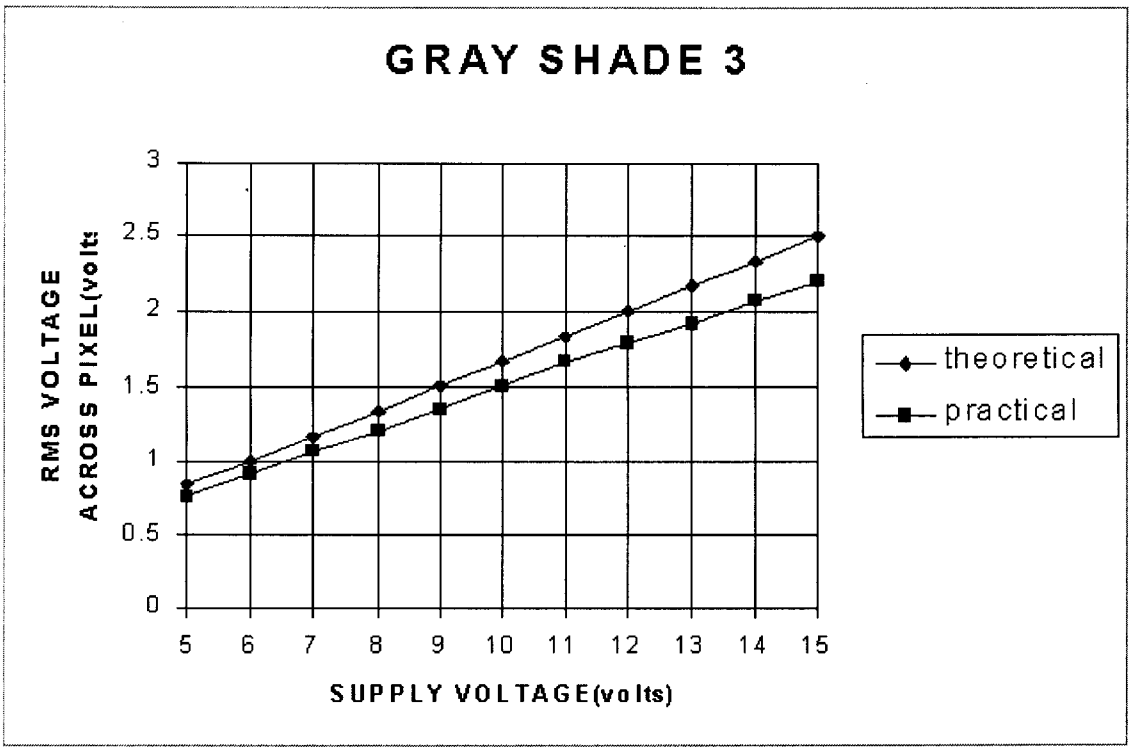
V_{supply}(V)	$V_{rms(theoretical)}$(V)	$V_{rms(practical)}$(V)
5	0.7656	0.6976
6	0.9186	0.8404
7	1.0762	0.9805
8	1.2247	1.1202
9	1.3778	1.2553
10	1.5309	1.3879
11	1.6840	1.5180
12	1.8371	1.6500
13	1.9902	1.7813
14	2.1433	1.9110
15	2.2961	2.0450



Graph 5.3

GRAY SHADE 2:

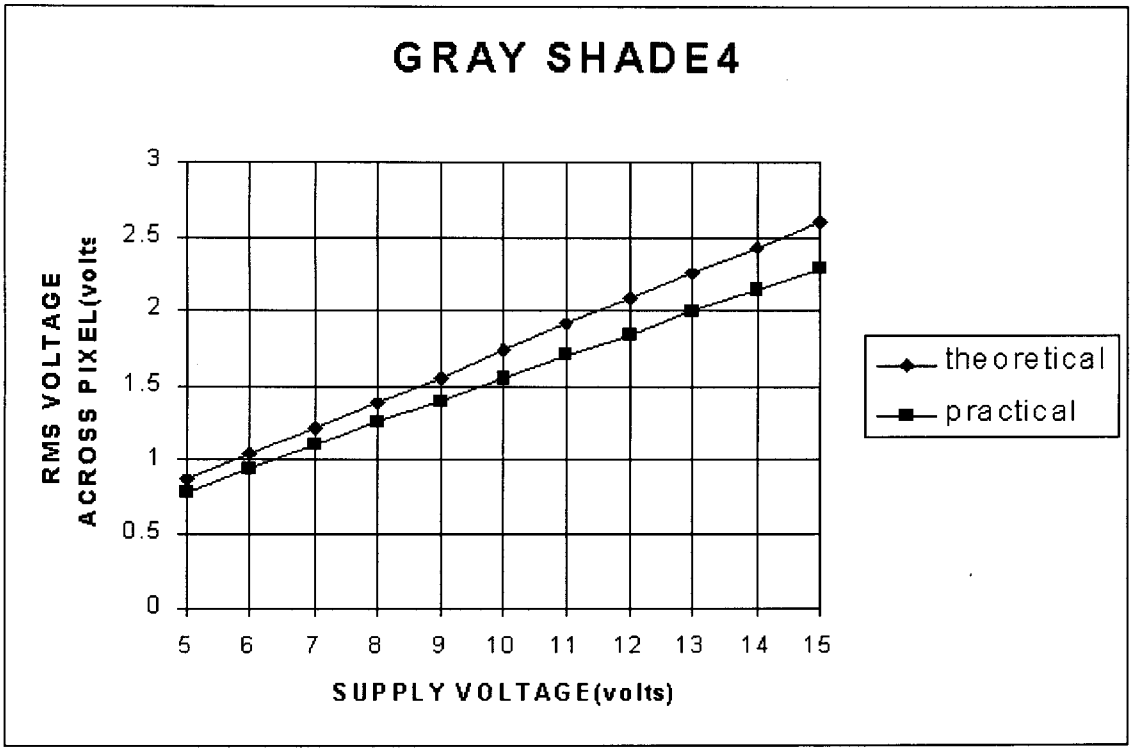
V_{supply}(V)	$V_{rms(theoretical)}$(V)	$V_{rms(practical)}$(V)
5	0.8011	0.7271
6	0.9613	0.8747
7	1.1215	1.0195
8	1.2817	1.1623
9	1.4420	1.2993
10	1.6022	1.444
11	1.7623	1.5766
12	1.9226	1.7116
13	2.0828	1.8414
14	2.2430	1.9790
15	2.4032	2.1200



Graph 5.4

GRAY SHADE 3:

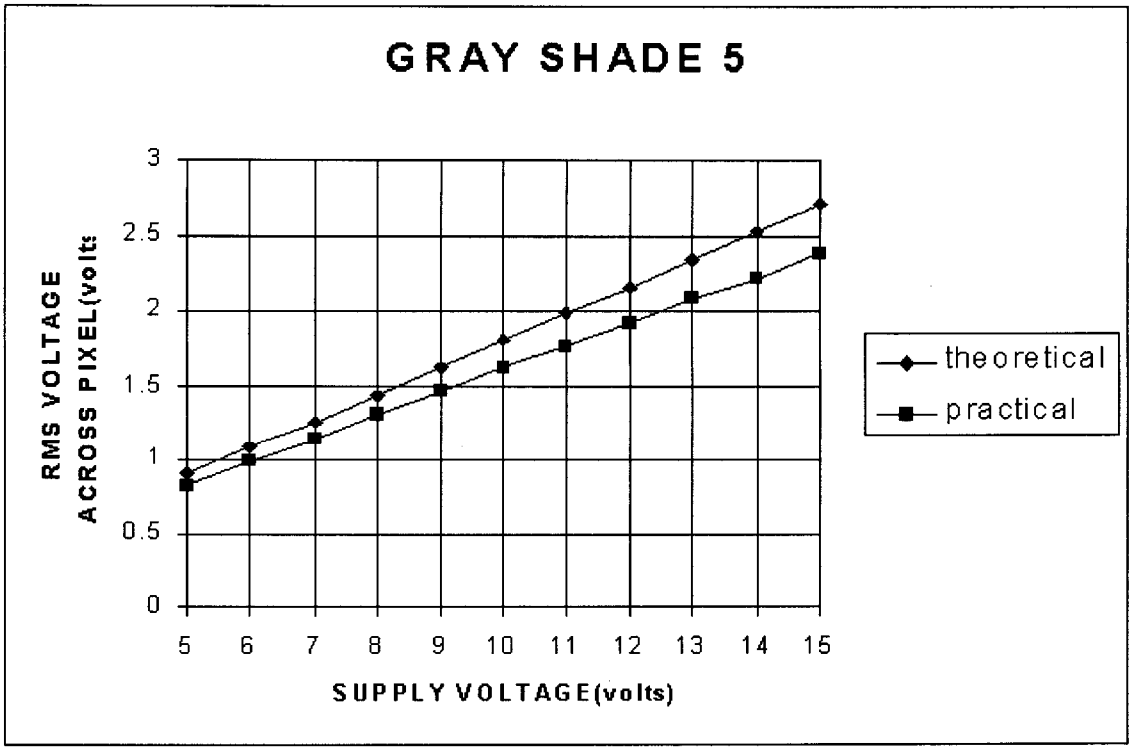
V_{supply}(V)	$V_{rms(theoretical)}$(V)	$V_{rms(practical)}$(V)
5	0.8352	0.7542
6	1.0022	0.9091
7	1.1693	1.0611
8	1.3363	1.2129
9	1.5033	1.3560
10	1.6704	1.5008
11	1.8374	1.6569
12	2.0045	1.7934
13	2.1715	1.9200
14	2.3385	2.0690
15	2.5055	2.2090



Graph 5..5

GRAY SHADE 4:

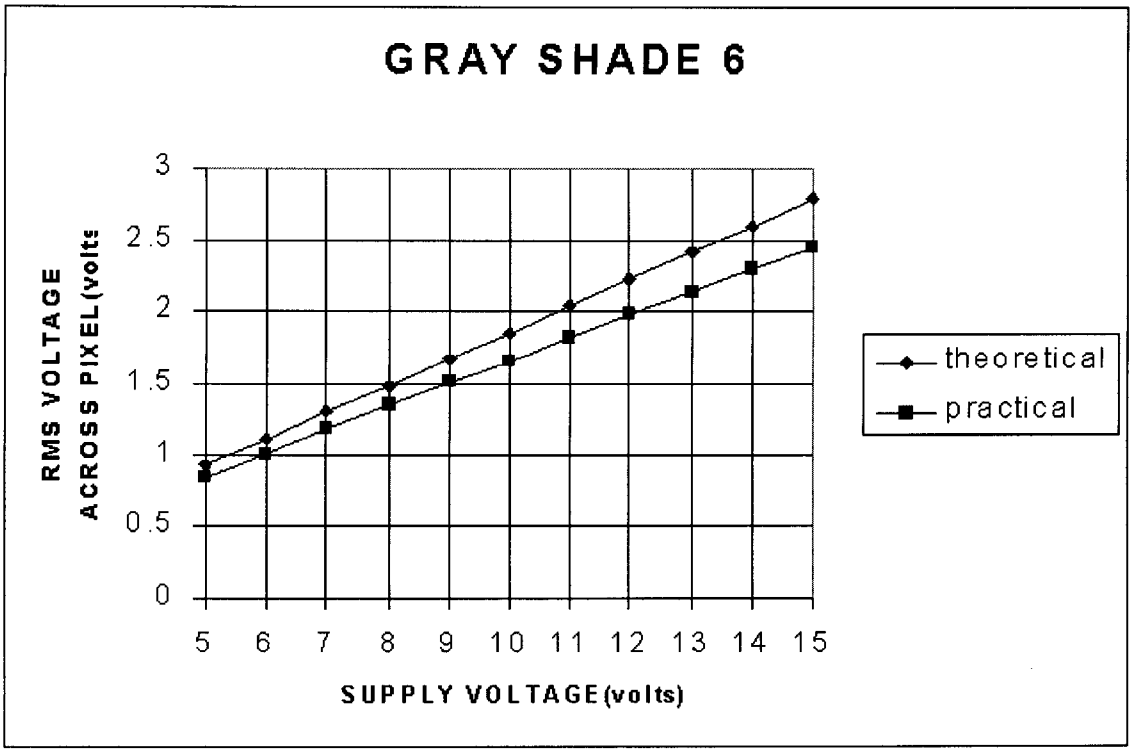
V_{supply}(V)	$V_{rms(theoretical)}$(V)	$V_{rms(practical)}$(V)
5	0.8680	0.7860
6	1.0415	0.9466
7	1.2151	1.1037
8	1.3887	1.2602
9	1.5623	1.4045
10	1.7359	1.5596
11	1.9095	1.7080
12	2.0831	1.8446
13	2.2567	1.9960
14	2.4303	2.1410
15	2.6038	2.2910



Graph 5.6

GRAY SHADE 5:

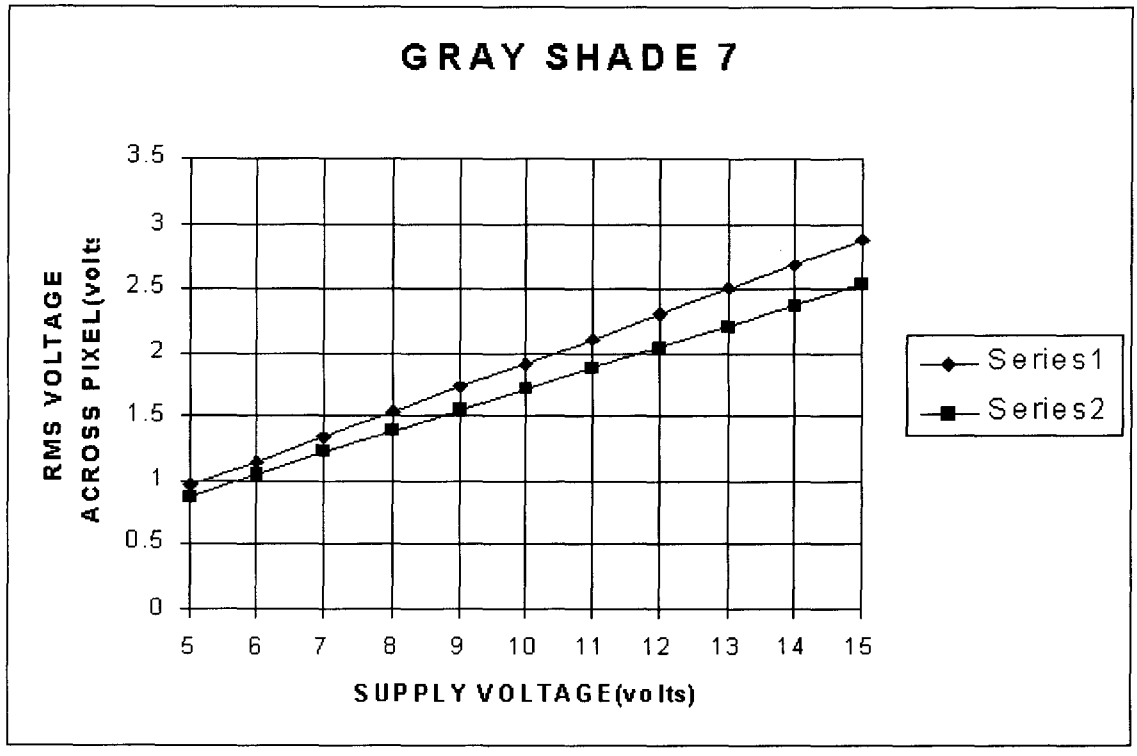
V_{supply}(V)	$V_{rms(theoretical)}$(V)	$V_{rms(practical)}$(V)
5	0.8990	0.8135
6	1.0794	0.9795
7	1.2593	1.1441
8	1.4392	1.3051
9	1.6192	1.4606
10	1.7991	1.6146
11	1.9789	1.7607
12	2.1588	1.9180
13	2.3387	2.0830
14	2.5187	2.2080
15	2.6985	2.3760



Graph 5.7

GRAY SHADE 6:

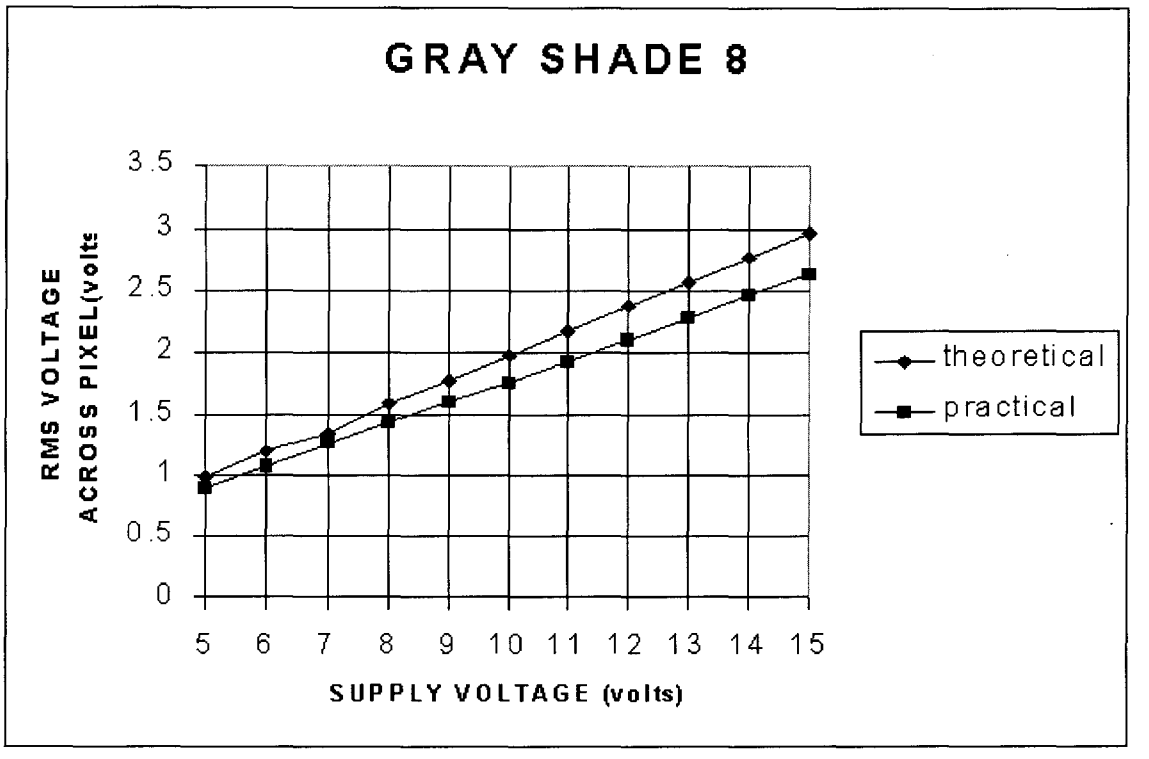
V_{supply}(V)	$V_{rms(theoretical)}$(V)	$V_{rms(practical)}$(V)
5	0.9300	0.8430
6	1.1160	1.0086
7	1.3020	1.1839
8	1.4881	1.3517
9	1.6740	1.5116
10	1.8601	1.6687
11	2.0461	1.8261
12	2.2321	1.9840
13	2.4180	2.1450
14	2.6041	2.3070
15	2.7901	2.4440



Graph 5.8

GRAY SHADE 7:

V_{supply}(V)	$V_{rms(theoretical)}$(V)	$V_{rms(practical)}$(V)
5	0.9596	0.8686
6	1.1515	1.0462
7	1.3434	1.2211
8	1.5353	1.3950
9	1.7272	1.5594
10	1.9191	1.7242
11	2.1110	1.8840
12	2.3029	2.0440
13	2.4949	2.2070
14	2.6868	2.370
15	2.8787	2.5340



Graph 5.9

GRAY SHADE 8:

V_{supply}(V)	$V_{rms(theoretical)}$(V)	$V_{rms(practical)}$(V)
5	0.9882	0.8900
6	1.1855	1.0722
7	1.3490	1.2514
8	1.5811	1.4281
9	1.7787	1.5969
10	1.9764	1.7643
11	2.1740	1.9290
12	2.3717	2.0910
13	2.5693	2.2570
14	2.7669	2.4260
15	2.9646	2.5770

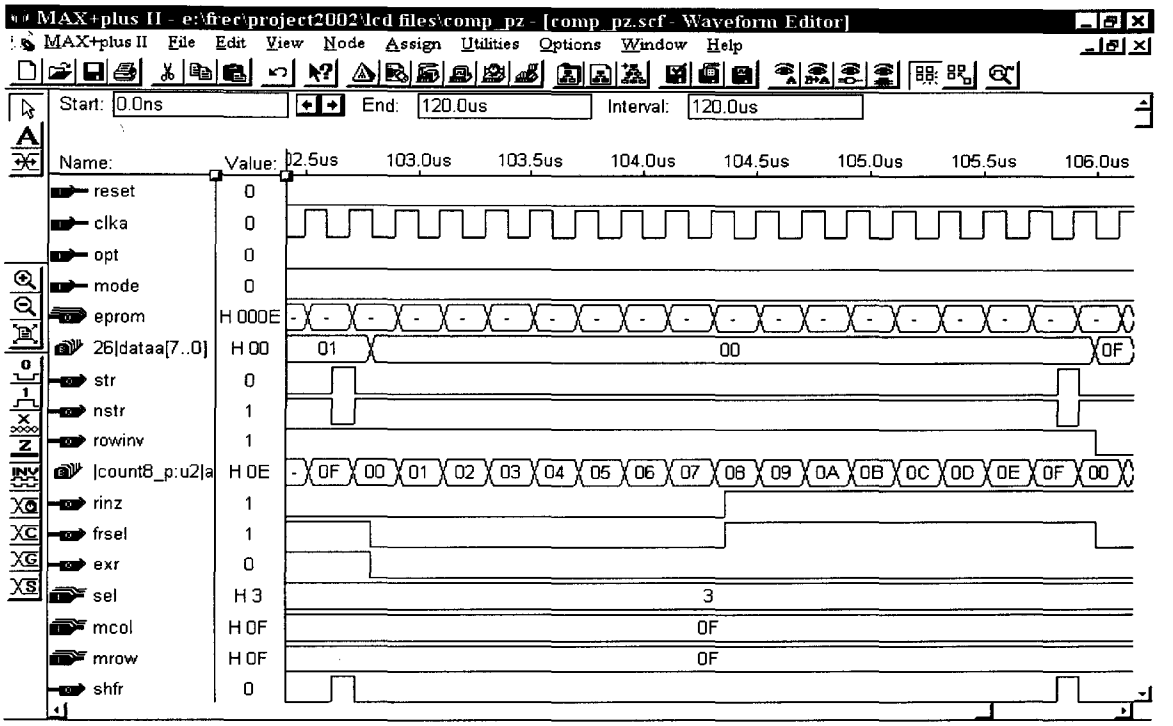

MAX+plus II - e:\frec\project2002\lcd files\comp_pz - [comp_pz.scf - Waveform Editor]
MAX+plus II File Edit View Node Assign Utilities Options Window Help
Start: 0.0ns End: 120.0us Interval: 120.0us
Name: Value:
reset 0
clka 0
opt 0
mode 0
eprom H 000E
26|dataa[7..0] H 00
str 0
nstr 1
rowinv 1
|count8_p:u2|a H 0E
rinz 1
frsel 1
exr 0
sel H 3
mcol H 0F
mrow H 0F
shfr 0
02.5us 103.0us 103.5us 104.0us 104.5us 105.0us 105.5us 106.0us
01 00 0F
0F 00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F 00
3
0F
0F

Fig 5.1

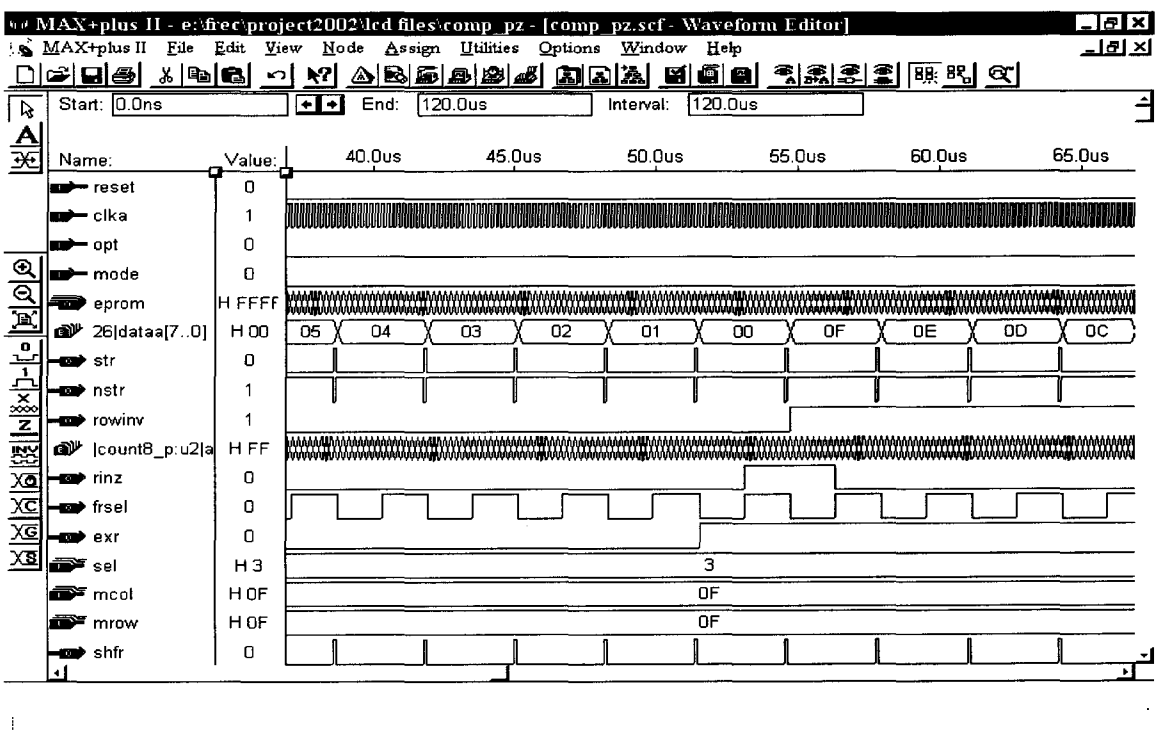

MAX+plus II - e:\frec\project2002\lcd files\comp_pz - [comp_pz.scf - Waveform Editor]
MAX+plus II File Edit View Node Assign Utilities Options Window Help
Start: 0.0ns End: 120.0us Interval: 120.0us
Name: Value:
reset 0
clka 1
opt 0
mode 0
eprom H FFFF
26|dataa[7..0] H 00
str 0
nstr 1
rowinv 1
|count8_p:u2|a H FF
rinz 0
frsel 0
exr 0
sel H 3
mcol H 0F
mrow H 0F
shfr 0
40.0us 45.0us 50.0us 55.0us 60.0us 65.0us
05 04 03 02 01 00 0F 0E 0D 0C
3
0F
0F

Fig 5.2

CONCLUSION

The circuits have been successfully designed and implemented to display eight levels of gray shades on a16x 16 displays. A display with greater picture details can be obtained by increasing the number of gray shades using AM technique. Same circuit with proportionate change in clock, memory size, voltage generator etc. can be used for this purpose.

FUTURE SCOPE

Work can be done to increase the number of gray shades for a given number of voltage levels. Schemes involving non-linear spacing of gray levels can be experimented upon to increase number of gray shades and improve contrast. The effect of variations in voltage levels on the accuracy of information displayed can also be studied.

APPENDIX -A

1) SELECTION RATIO MAXIMIZATION

$$V_{on}(rms) = \sqrt{\frac{(Vr+Vc)^2 + (N-1)Vc^2}{N}}$$

$$V_{off}(rms) = \sqrt{\frac{(Vr-Vc)^2 + (N-1)Vc^2}{N}}$$

$$Selection\ ratio = \frac{Von(rms)}{Voff(rms)}$$

$$SR = \sqrt{\frac{(Vr+Vc)^2 + (N-1)Vc^2}{(Vr-Vc)^2 + (N-1)Vc}} = \sqrt{\frac{(Vr^2 + 2VrVc + NVc^2)}{(Vr^2 - 2VrVc + NVc\ )}}$$

$Put\ a = Vr/Vc$

$$SR = \sqrt{\frac{(a^2 + 2a + N)}{(a^2 - 2a + N)}}$$

Differentiating above equation and equating to zero to obtain maxima

$(a^2-2a+N)(2a+2N)-(a^2+2a+N)(2a-2N)=0$

$(a^2-2a+N)(a+2)-(a^2+2a+N)(a-2)=0$

$a(a^2-2a+N-a^2-2a-N)+ a(a^2-2a+N+a^2+2a+N)=0$

$a(-4a)+2a^2+2N=0$

$a^2=N$

$a=\sqrt{N}$

Substituting for a in expression for SR

$$SR=\sqrt{\frac{(N+2\sqrt{N}+N)}{(N-2\sqrt{N}+N)}}$$

$$SR=\sqrt{\frac{(\sqrt{N}+1)}{(\sqrt{N}-1)}}$$

2) AMPLITUDE MODULATION

Expression for rms voltages across pixel over one row select interval

$$V_{c1,}=(k+\sqrt{(1-k^2)}Vc$$

$$V_{c1,}=(k-\sqrt{(1-k^2)}Vc$$

$$V_{pixel}=\sqrt{\frac{(Vr-Vc_1)^2T+(Vr-Vc_2)^2T}{2T}}$$ where *2T=row select time*

$$V^2_{pixel}=0.5\left\{Vr-(k+\sqrt{1-k^2})Vc]^2+[Vr-(k-\sqrt{1-k^2})Vc]^2\right\}$$

$$2V^2_{pixel}=\left\{Vr^2-(k+\sqrt{1-k^2})^2Vc^2-2VrVc\,(k+\sqrt{1-k^2})]\right\}+$$

$$\left\{Vr^2-(k-\sqrt{1-k^2})^2Vc^2-2VrVc\,(k-\sqrt{1-k^2})]\right\}$$

$$2V^2_{pixel}=\left\{2Vr^2-2VrVc\,(k+\sqrt{1-k^2}+k-\sqrt{1-k^2}]\right\}+$$

$$\left\{Vc^2(2k^2+2-2k^2+2k\sqrt{1-k^2}-2k\sqrt{1-k^2}\right\}$$

$$2V^2_{pixel}=2Vr^2-4kVrVc+2Vc^2$$

APPENDIX-B

SED1180

CMOS LCD 64-SEGMENT DRIVER

■ DESCRIPTION

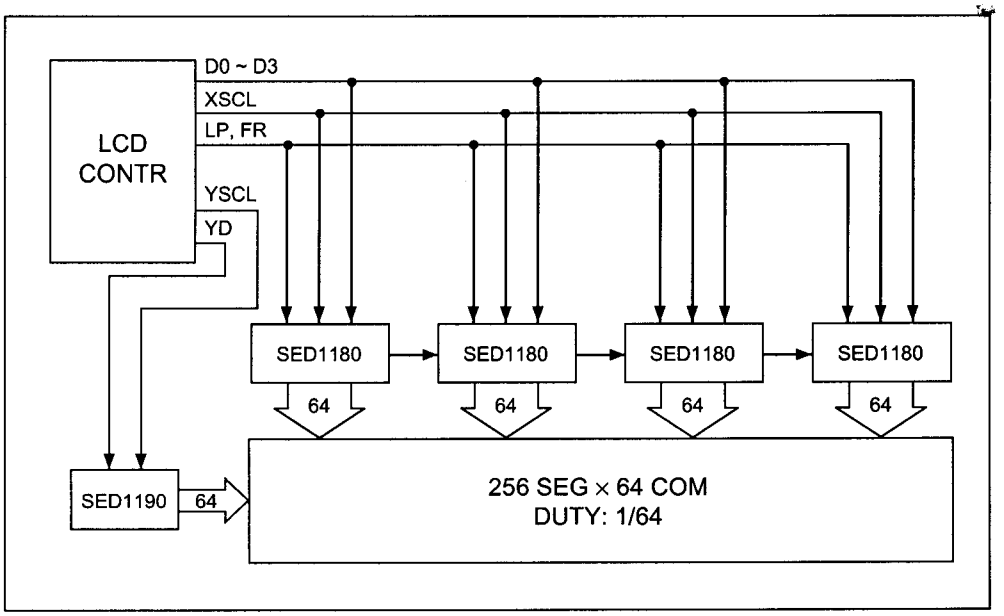
The SED1180 is a dot matrix LCD segment (column) driver for driving high-capacity LCD panel at duty cycles higher than 1/64. The LSI contains 64-bit shift register for display data. The display data is supplied through 4-bit bus, and serially transferred through 16 × 4 bit shift register. The display data is held in a 64-bit latch circuit. The LSI converts the level of the latched data to an LCD drive waveform.

The SED1180 is used in conjunction with the SED1190 (64-bit row driver) to drive a large-capacity dot matrix LCD panel.

■ FEATURES

- Low-power CMOS technology
- 64-bit segment (column) driver
- High-speed 4-bit data
- Duty cycle ..... 1/64 to 1/128
- Daisy chain enable support
- Wide range of LCD voltage .....–14V to –25V
- Supply voltage ..... 5.0V ±10%
- Package ..... QFP1-80 pin (F0A)
  QFP5-80 pin (F5A)
  DIE: Al pad chip (D0A)

■ SYSTEM BLOCK DIAGRAM



Number	Name	Number	Name	Number	Name	Number	Name
1	SEG27	21	SEG 7	41	SEG36	61	SEG56
2	SEG26	22	SEG 6	42	SEG37	62	SEG57
3	SEG25	23	SEG 5	43	SEG38	63	SEG58
4	SEG24	24	SEG 4	44	SEG39	64	SEG59
5	SEG23	25	SEG 3	45	SEG40	65	SEG60
6	SEG22	26	SEG 2	46	SEG41	66	SEG61
7	SEG21	27	SEG 1	47	SEG42	67	SEG62
8	SEG20	28	SEG 0	48	SEG43	68	SEG63
9	SEG19	29	EO	49	SEG44	69	V_{SSH}
10	SEG18	30	D3	50	SEG45	70	V2
11	SEG17	31	D2	51	SEG46	71	V3
12	SEG16	32	D1	52	SEG47	72	V_{SS}
13	SEG15	33	D0	53	SEG48	73	V_{DD}
14	SEG14	34	XSCL	54	SEG49	74	TEST
15	SEG13	35	LP	55	SEG50	75	EI
16	SEG12	36	FR	56	SEG51	76	ECL
17	SEG11	37	SEG32	57	SEG52	77	SEG31
18	SEG10	38	SEG33	58	SEG53	78	SEG30
19	SEG 9	39	SEG34	59	SEG54	79	SEG29
20	SEG 8	40	SEG35	60	SEG55	80	SEG28

■ PIN DESCRIPTION

Pin Name	Function
SEG0 to SEG63	Outputs to segment pins of LCD. Output level changes at each latch pulse LP falling edge.
XSCL	Data shift clock input: display data is shifted in on the falling edge of this signal.
LP	Latch pulse for displayed data, falling edge trigger: display data is latched on the falling edge of this signal.
FR	LCD AC-drive signal
EI	Active high daisy chain enable input
EO	Active high daisy chain enable output
ECL	Daisy chain enable clock: the daisy chain enable is propagated on the falling edge of this clock.
D0 to D3	4-bit display data input
TEST	Test output
V_{DD}, V_{SS}	Logic power inputs
V2, V3, V_{SSH}	LCD drive power inputs V_{SSH}: –14V to –23V $V_{DD} \geq V2 \geq V3 \geq V_{SSH}$

■ ELECTRICAL CHARACTERISTICS

● DC Electrical Characteristics

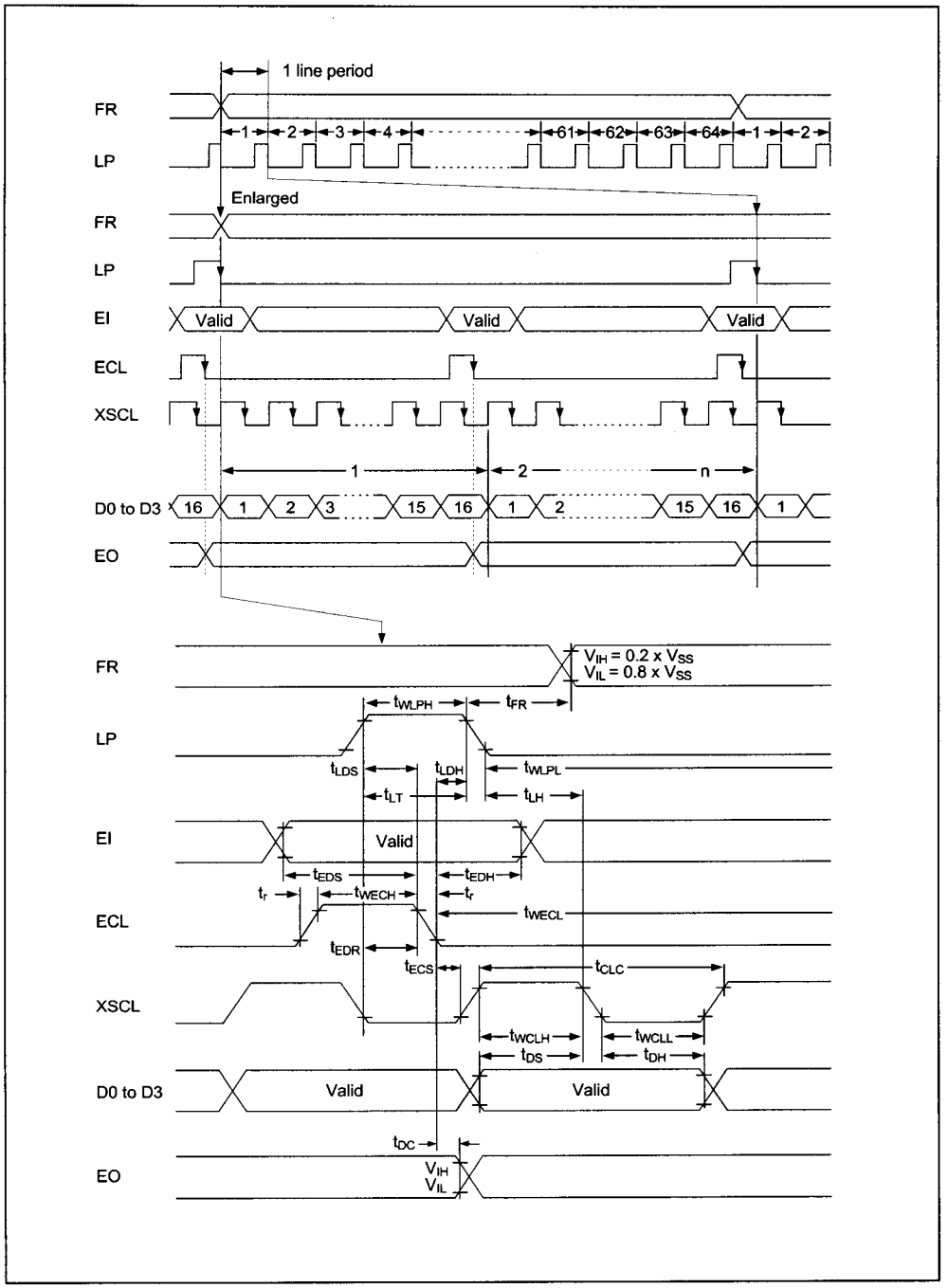
(V_{DD} = 0V, V_{SS} = –5.0 V ± 10%, T_a = –20 to 75°C)

Parameters	Symbol	Condition		Rating Min	Rating Typ	Rating Max	Unit
Supply voltage (1)	V_{SS}			–5.5	–5.0	–4.5	V
Supply voltage (2)	V2			V_{SSH}	—	V_{DD}	V
	V3			V_{SSH}	—	V_{DD}	V
	V_{SSH}	Recommended V_{SSH}		–25.0	—	–14.0	V
		Operable V_{SSH} (see note)		–25.0	—	–5.0	V
HIGH-level input voltage	V_{IH}			0.2V_{SS}	—	V_{DD}–0.3	V
LOW-level input voltage	V_{IL}			V_{SS}–0.3	—	0.8V_{SS}	V
HIGH-level output voltage	V_{OH}	I_{OH} = -0.6 ma		-0.4	—	—	V
LOW-level output voltage	V_{OL}	I_{OL} = 0.6 ma		—	—	V_{SS}+0.4	V
Input leakage current	I_{LI}	0 V ≤ V_I ≤ V_{SS}		—	0.05	2.0	µA
Output leakage current	I_{LO}	0 V ≤ V_O ≤ V_{SS}		—	0.05	5.0	µA
Shift clock	XSCL			—	—	6.0	MHz
Frame signal	FR			—	1/60	—	S
Input capacitance	CI	T_a = 25°C		—	5.0	8.0	pF
Segment output on resistance	R_{SEG}	V_{OH} = V_{DD} = –0.5 V V_{OL} = V_{SSH} = +0.5 V SEG bit	V_{SSH} = –20.0 V	—	1.9	2.9	kΩ
			V_{SSH} = –14.0 V	—	2.4	3.9	
			V_{SSH} = –9.0 V	—	3.6	7.0	
			V_{SSH} = –5.0 V	—	11.5	500.0	
Quiescent current	I_Q	V_{SSH} = –25 V, V_{SSH} = –5.5 V, V_I = V_{DD}		—	0.05	30	µA
Operating current for the logic	I_{SSO}	FR cycle = 16.7 ms ECL cycle = 13 µS	V_{SS} = –5.0 V, V_{IH} = V_{DD}, V_{IL} = V_{SS}, LP cycle=130 µS, XSCL=1.5 MHz, (duty 50%) All data input reversed bit by bit. All output pins are open.	—	90	200	µA
Operating current for the LCD	I_{SSHO}	FR cycle = 16.7 ms ECL cycle = 13 µS	V_{SS} = –4.5 V, V_2 = –4.0 V, V_1 = –16.0 V, V_{SSH} = –20.0 V, V_{IH} = V_{DD}, V_{IL} = V_{SS}, XSCL=1.5 MHz, (duty 50%), all data input reversed bit by bit. All output pins are open.	—	40	80	µA

(continued)

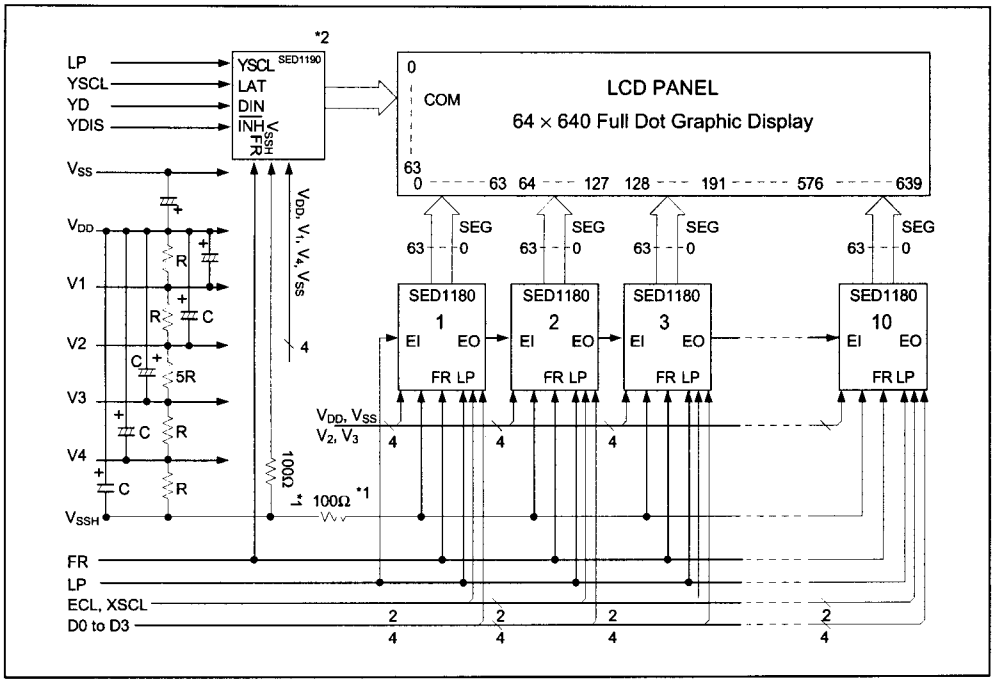
■ AC ELECTRICAL CHARACTERISTICS

● Data I/O Timing



■ TYPICAL SYSTEM CONNECTION

(64 × 640 pixels, 1/64 duty ratio)



Notes:

1. Current limiting resistors
2. Bypass Vss and VSSH with capacitors of at least 0.01 µF

SED1190

CMOS LCD 64-COMMON DRIVERS

■ DESCRIPTION

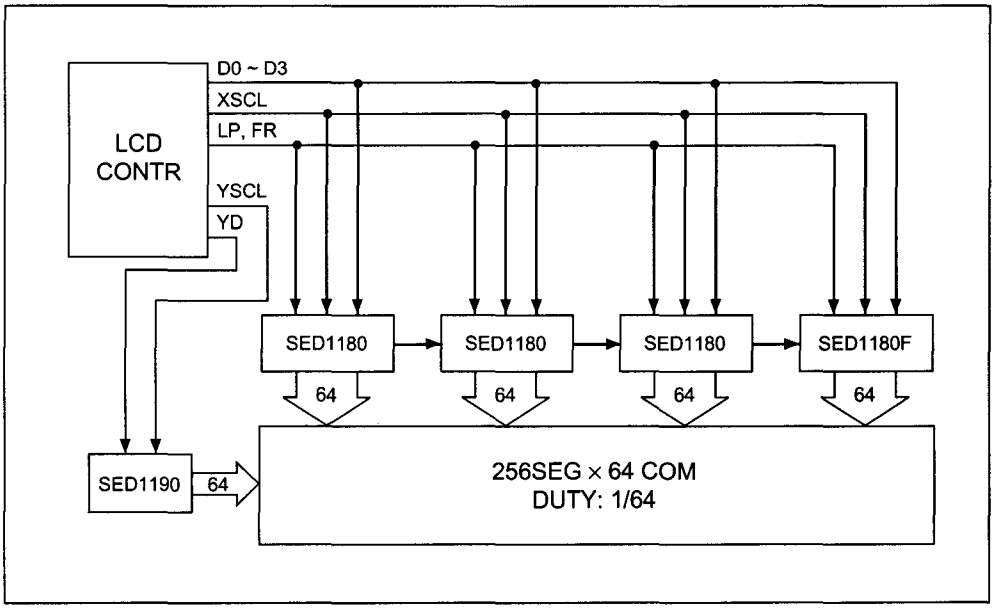
The SED1190 is a dot matrix LCD common (row) driver for driving high-capacity LCD panel at duty cycles higher than 1/64. The LSI uses two serially connected, 32-bit shift registers to hold the display data, and level shifter converts the TTL level 64-bit parallel data from the shift registers to levels suitable for use by the LCD drive circuitry. The SED1190 generates common drive signals using the voltages supplied to LCD drive voltages pins.

The SED1190 is used in conjunction with the SED1180 (64-bit row driver) to drive a large capacity dot matrix LCD panel.

■ FEATURES

- Low-power CMOS technology
- 64-bit common (row) driver
- Display blanking
- Duty cycle: 1/64 to 1/128
- Daisy chain enable support
- Wide range of LCD voltage: –14V to –25V
- Supply voltage: 5.0V ±10%
- Package: ..... QFP1-80 pin (F0A)
  QFP5-80 pin (F5A)
  DIE: Al pad chip (D0A)

■ SYSTEM BLOCK DIAGRAM



Number	Name	Number	Name	Number	Name	Number	Name
1	COM31	21	COM11	41	COM40	61	COM60
2	COM30	22	COM10	42	COM41	62	COM61
3	COM29	23	COM 9	43	COM42	63	COM62
4	COM28	24	COM 8	44	COM43	64	COM63
5	COM27	25	COM 7	45	COM44	65	DO
6	COM26	26	COM 6	46	COM45	66	V_{SSH}
7	COM25	27	COM 5	47	COM46	67	V4
8	COM24	28	COM 4	48	COM47	68	NC
9	COM23	29	COM 3	49	COM48	69	NC
10	COM22	30	COM 2	50	COM49	70	NC
11	COM21	31	COM 1	51	COM50	71	NC
12	COM20	32	COM 0	52	COM51	72	V1
13	COM19	33	COM32	53	COM52	73	V_{SS}
14	COM18	34	COM33	54	COM53	74	V_{DD}
15	COM17	35	COM34	55	COM54	75	NC
16	COM16	36	COM35	56	COM55	76	DI
17	COM15	37	COM36	57	COM56	77	LAT
18	COM14	38	COM37	58	COM57	78	$\overline{INH}$
19	COM13	39	COM38	59	COM58	79	FR
20	COM12	40	COM39	60	COM59	80	YSCL

NC = Not connected

■ PIN DESCRIPTION

Pin Name	Function
COM0 to COM63	LCD common drive outputs
DI	Serial data input
LAT	Transparent latch control input: LAT = H, DI = H → DI latch output: H LAT = H, DI = L → DI latch output: L LAT = L, DI = X → DI latch output: DI latch
DO	Serial data output
YSCL	Serial data shift clock. Data is shifted through the controller on the falling edge of this clock
FR	LCD AC-drive signal input
$\overline{INH}$	Active-low blanking input
V_{DD}, V_{SS}	Logic power supply inputs
V1, V4, V_{SSH}	LCD drive power inputs $V_{DD} \geq V1 \geq V4 \geq V_{SSH}$

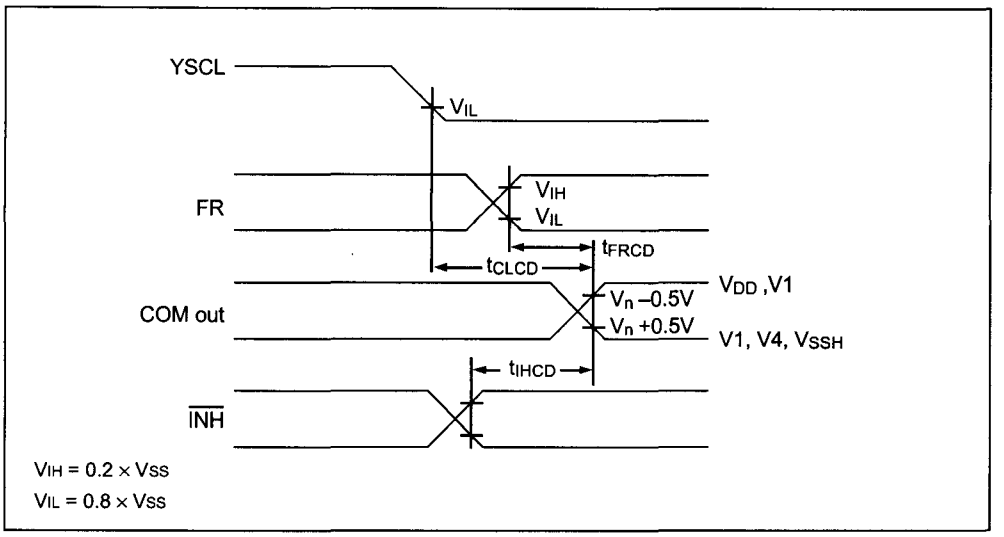
● DC Characteristics

(V_{DD} = 0V, V_{SS} = –5.0 V ±10%, T_a = –20 to 75°C)

Parameter	Symbol	Conditions		Rating Min	Rating Typ	Rating Max	Unit
Supply voltage (1)	V_{SS}			–5.5	–5.0	–4.5	V
Supply voltage (2)	V1			V_{SSH}	—	V_{DD}	V
	V4			V_{SSH}	—	V_{DD}	V
	V_{SSH}	Recommended V_{SSH}		–25.0	—	–14.0	V
		Operable V_{SSH} (see note)		–25.0	—	–5.0	V
High level input voltage	V_{IH}			0.2V_{SS}	—	V_{DD}+0.3	V
Low level input voltage	V_{IL}			V_{SS}–0.3	—	0.8V_{SS}	V
High level output voltage	V_{OH}	I_{OH} = –0.6 mA		–0.4	—	—	V
Low level output voltage	V_{OL}	I_{OL} = 0.6 mA		—	—	V_{SS}+0.4	V
Input leakage current	I_{LI}	0 V ≥ V_I ≥ V_{SS}		—	0.05	2.0	µA
Output leakage current	I_{LO}	0 V ≥ V_O ≥ V_{SS}		—	0.05	5.0	µA
Shift clock	YSCL			—	—	2.5	MHz
Frame signal	FR			—	1/60	—	s
Input capacitance	C_I	T_a = 25°C		—	5.0	8.0	pF
Common output on resistance	R_{COM}	V_{OH} = V_{DD} –0.5 V V_{OL} = V_{SSH} +0.5 V COM bit	V_{SSH} = –20.0 V	—	0.8	1.0	kΩ
			V_{SSH} = –14.0 V	—	0.9	1.3	
			V_{SSH} = –9.0 V	—	1.3	2.0	
			V_{SSH} = –5.0 V	—	3.0	30.0	
Quiescent current	I_Q	SED 1190	V_{SSH} = –25 V, V_{SSH} = –5.5 V, V_I = V_{DD}	—	0.05	30	µA
Operating current for the logic	I_{SS}	FR cycle = 16.7 ms	V_{SS} = –5.0 V, V_{IH} = V_{DD}, V_{IL} = V_{SS}, YSCL cycle = 130 µs (duty 50%), All "H" output terminals are opened at every data input all 1/128 duty.	—	3.0	8.0	µA
Operating current for LCD	I_{SSH}	FR cycle = 16.7 ms	V_{SS} = –4.5 V, V_1 = –2.0 V, V_4 = –18.0 V, YSCL cycle = 130 µs (duty 50%), All "H" output terminals are opened at every data input of 1/128 duty.	—	3.0	8.0	µA
Pull up MOS current	$-I_p$	V_{SS} = –5.0 V, V_{IL} = –5.0 V Applicable to LAT input terminals		10.0	25.0	50.0	µA

Note: Error free operation is guaranteed in this range but the output resistance of the LCD drivers is higher than in the recommended operating range. It is suggested that the driver is tested with the target LCD panel to determine if performance is acceptable.

● **Common Drive**



V_{DD} = 0V, V_{SS} = –5.0V ± 10%, T_a = –20 to 75°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
YSCL – COM output delay time	t_{CLCD}	V_{SSH} = –14.0 to –25.0V C_L = 100pF	—	—	3.0	µs
RF – COM output delay time	t_{FRCD}		—	—	3.0	µs
INH – COM output delay time	t_{IHCD}		—	—	3.0	µs

TEXAS INSTRUMENTS

CD4051B, CD4052B, CD4053B

Data sheet acquired from Harris Semiconductor
SCHS047D

August 1998 - Revised March 2000

CMOS Analog Multiplexers/Demultiplexers with Logic Level Conversion

The CD4051B, CD4052B, and CD4053B analog multiplexers are digitally-controlled analog switches having low ON impedance and very low OFF leakage current. Control of analog signals up to $20V_{P-P}$ can be achieved by digital signal amplitudes of 4.5V to 20V (if V_{DD}-V_{SS} = 3V, a V_{DD}-V_{EE} of up to 13V can be controlled; for V_{DD}-V_{EE} level differences above 13V, a V_{DD}-V_{SS} of at least 4.5V is required). For example, if V_{DD} = +4.5V, V_{SS} = 0V, and V_{EE} = -13.5V, analog signals from -13.5V to +4.5V can be controlled by digital inputs of 0V to 5V. These multiplexer circuits dissipate extremely low quiescent power over the full V_{DD}-V_{SS} and V_{DD}-V_{EE} supply-voltage ranges, independent of the logic state of the control signals. When a logic "1" is present at the inhibit input terminal, all channels are off.

The CD4051B is a single 8-Channel multiplexer having three binary control inputs, A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned on, and connect one of the 8 inputs to the output.

The CD4052B is a differential 4-Channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 of 4 pairs of channels to be turned on and connect the analog inputs to the outputs.

The CD4053B is a triple 2-Channel multiplexer having three separate digital control inputs, A, B, and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole, double-throw configuration.

When these devices are used as demultiplexers, the "CHANNEL IN/OUT" terminals are the outputs and the "COMMON OUT/IN" terminals are the inputs.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD4051BF, CD4052BF, CD4053BF	-55 to 125	16 Ld CERAMIC DIP
CD4051BE, CD4052BE, CD4053BE	-55 to 125	16 Ld PDIP
CD4051BM, CD4051BNS	-55 to 125	16 Ld SOIC
CD4051BPW, CD4052BPW, CD4053BPW	-55 to 125	16 Ld TSSOP

Features

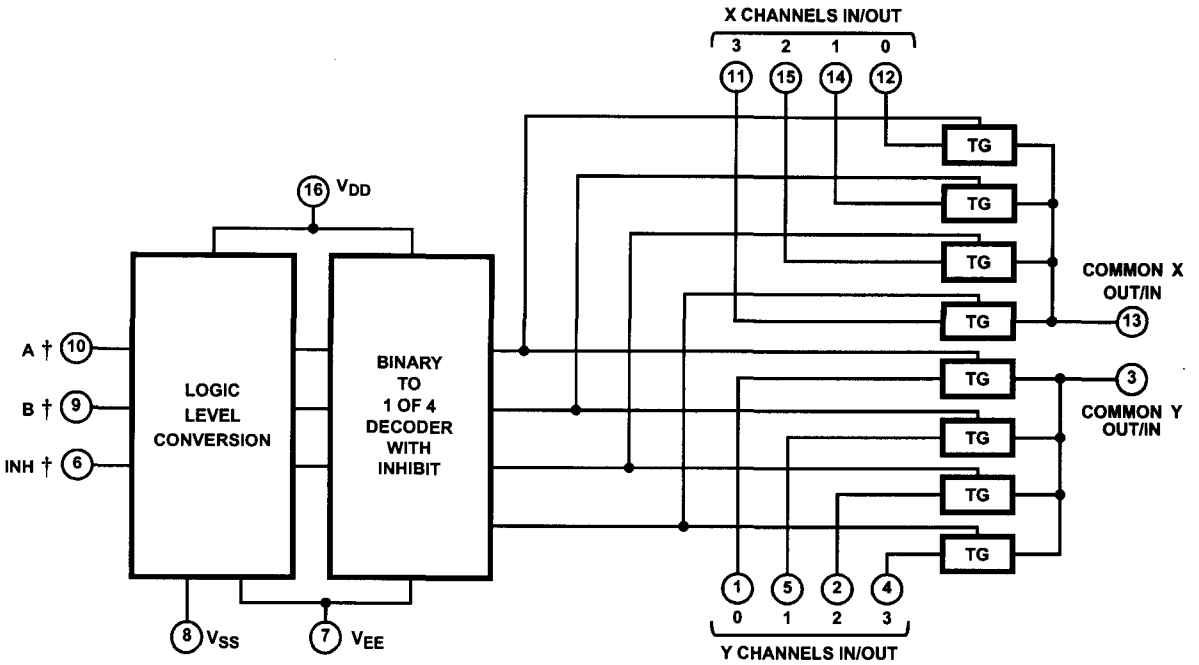
- Wide Range of Digital and Analog Signal Levels
  - Digital . . . . . 3V to 20V
  - Analog. . . . . ≤$20V_{P-P}$
- Low ON Resistance, 125Ω (Typ) Over $15V_{P-P}$ Signal Input Range for V_{DD}-V_{EE} = 18V
- High OFF Resistance, Channel Leakage of ±100pA (Typ) at V_{DD}-V_{EE} = 18V
- Logic-Level Conversion for Digital Addressing Signals of 3V to 20V (V_{DD}-V_{SS} = 3V to 20V) to Switch Analog Signals to $20V_{P-P}$ (V_{DD}-V_{EE} = 20V)
- Matched Switch Characteristics, r_{ON} = 5Ω (Typ) for V_{DD}-V_{EE} = 15V
- Very Low Quiescent Power Dissipation Under All Digital-Control Input and Supply Conditions, 0.2μW (Typ) at V_{DD}-V_{SS} = V_{DD}-V_{EE} = 10V
- Binary Address Decoding on Chip
- 5V, 10V and 15V Parametric Ratings
- 10% Tested for Quiescent Current at 20V
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range, 100nA at 18V and 25°C
- Break-Before-Make Switching Eliminates Channel Overlap

Applications

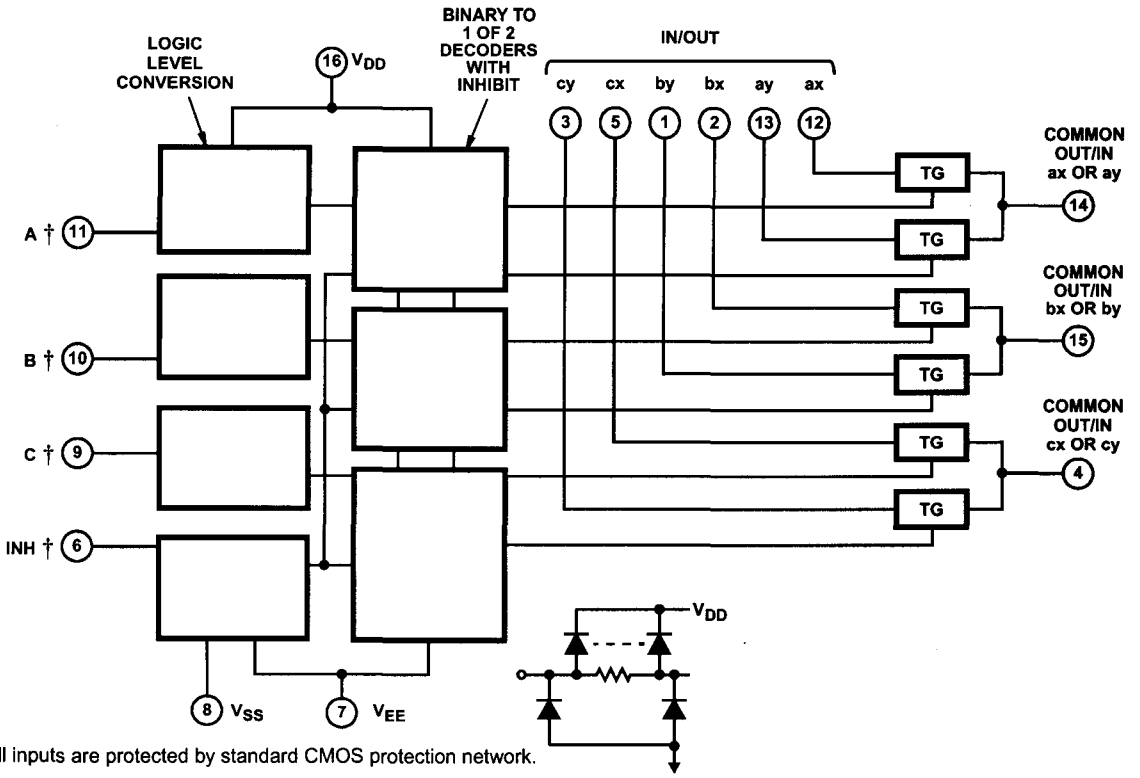
- Analog and Digital Multiplexing and Demultiplexing
- A/D and D/A Conversion
- Signal Gating

Functional Block Diagrams (Continued)

CD4052B



CD4053B



†All inputs are protected by standard CMOS protection network.

Absolute Maximum Ratings

Supply Voltage (V+ to V-)
Voltages Referenced to V_{SS} Terminal ..... -0.5V to 20V
DC Input Voltage Range ..... -0.5V to V_{DD} +0.5V
DC Input Current, Any One Input..... ±10mA

Operating Conditions

Temperature Range ..... -55°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
E Package	67	N/A
F Package	115	45
D Package	73	N/A
NS Package	64	N/A
PW Package	108	N/A

Maximum Junction Temperature (Ceramic Package) ..... 175°C
Maximum Junction Temperature (Plastic Package) ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 265°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance with JESD51.

Electrical Specifications

Common Conditions Here: If Whole Table is For the Full Temp. Range, V_{SUPPLY} = ±5V, A_V = +1, R_L = 100Ω, Unless Otherwise Specified (Note 3)

PARAMETER	CONDITIONS				LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
									25			
	V_{IS} (V)	V_{EE} (V)	V_{SS} (V)	V_{DD} (V)	-55	-40	85	125	MIN	TYP	MAX	
SIGNAL INPUTS (V_{IS}) AND OUTPUTS (V_{OS})												
Quiescent Device Current, I_{DD} Max	-	-	-	5	5	5	150	150	-	0.04	5	µA
	-	-	-	10	10	10	300	300	-	0.04	10	µA
	-	-	-	15	20	20	600	600	-	0.04	20	µA
	-	-	-	20	100	100	3000	3000	-	0.08	100	µA
Drain to Source ON Resistance r_{ON} Max $0 \le V_{IS} \le V_{DD}$	-	0	0	5	800	850	1200	1300	-	470	1050	Ω
	-	0	0	10	310	330	520	550	-	180	400	Ω
	-	0	0	15	200	210	300	320	-	125	240	Ω
Change in ON Resistance (Between Any Two Channels), Δr_{ON}	-	0	0	5	-	-	-	-	-	15	-	Ω
	-	0	0	10	-	-	-	-	-	10	-	Ω
	-	0	0	15	-	-	-	-	-	5	-	Ω
OFF Channel Leakage Current: Any Channel OFF (Max) or ALL Channels OFF (Common OUT/IN) (Max)	-	0	0	18	±100 (Note 2)		±1000 (Note 2)		-	±0.01	±100 (Note 2)	nA
Capacitance: Input, C_{IS}	-	-5	5-	5	-	-	-	-	-	5	-	pF
Output, C_{OS} CD4051					-	-	-	-	-	30	-	pF
CD4052					-	-	-	-	-	18	-	pF
CD4053					-	-	-	-	-	9	-	pF
Feedthrough C_{IOS}					-	-	-	-	-	0.2	-	pF
Propagation Delay Time (Signal Input to Output	V_{DD} 	R_L = 200kΩ, C_L = 50pF, t_r, t_f = 20ns		5	-	-	-	-	-	30	60	ns
				10	-	-	-	-	-	15	30	ns
				15	-	-	-	-	-	10	20	ns

Electrical Specifications

PARAMETER	TEST CONDITIONS					LIMITS	UNITS
	V_{IS} (V)	V_{DD} (V)	R_L (kΩ)			TYP	
Total Harmonic Distortion, THD	2 (Note 3)	5	10			0.3	%
	3 (Note 3)	10				0.2	%
	5 (Note 3)	15				0.12	%
	$V_{EE} = V_{SS}$, f_{IS} = 1kHz Sine Wave						%
-40dB Feedthrough Frequency (All Channels OFF)	5 (Note 3)	10	1	V_{OS} at Common OUT/IN	CD4053	8	MHz
	$V_{EE} = V_{SS}$, $20\text{Log}\frac{V_{OS}}{V_{IS}} = -40\text{dB}$				CD4052	10	MHz
					CD4051	12	MHz
				V_{OS} at Any Channel		8	MHz
-40dB Signal Crosstalk Frequency	5 (Note 3)	10	1	Between Any 2 Channels		3	MHz
	$V_{EE} = V_{SS}$, $20\text{Log}\frac{V_{OS}}{V_{IS}} = -40\text{dB}$			Between Sections, CD4052 Only	Measured on Common	6	MHz
					Measured on Any Channel	10	MHz
				Between Any Two Sections, CD4053 Only	In Pin 2, Out Pin 14	2.5	MHz
					In Pin 15, Out Pin 14	6	MHz
Address-or-Inhibit-to-Signal Crosstalk	-	10	10 (Note 4)			65	mV_{PEAK}
	$V_{EE} = 0$, $V_{SS} = 0$, t_r, t_f = 20ns, $V_{CC} = V_{DD} - V_{SS}$ (Square Wave)					65	mV_{PEAK}

NOTES:

3. Peak-to-Peak voltage symmetrical about $\frac{V_{DD} - V_{EE}}{2}$
4. Both ends of channel.

Typical Performance Curves

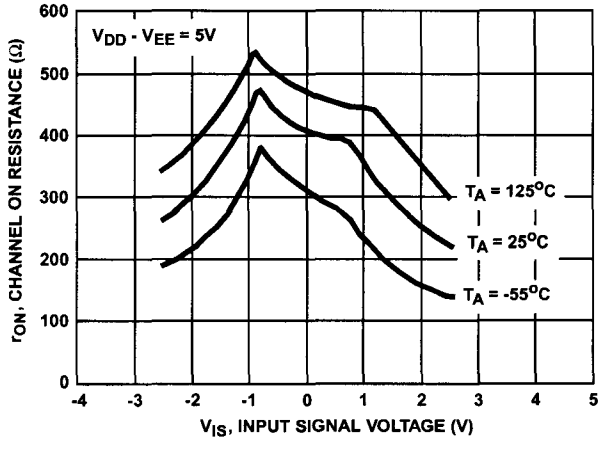


FIGURE 1. CHANNEL ON RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)

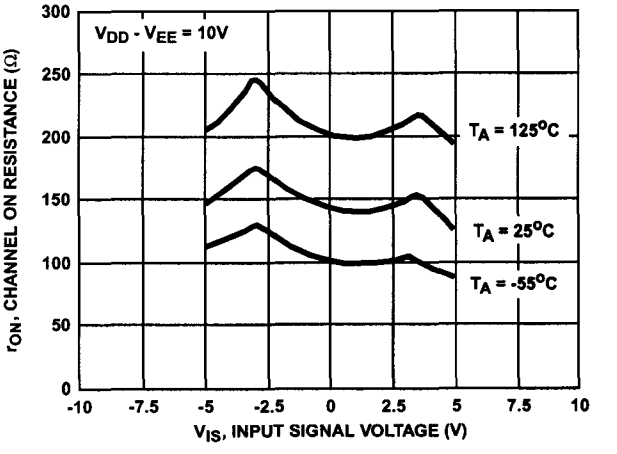
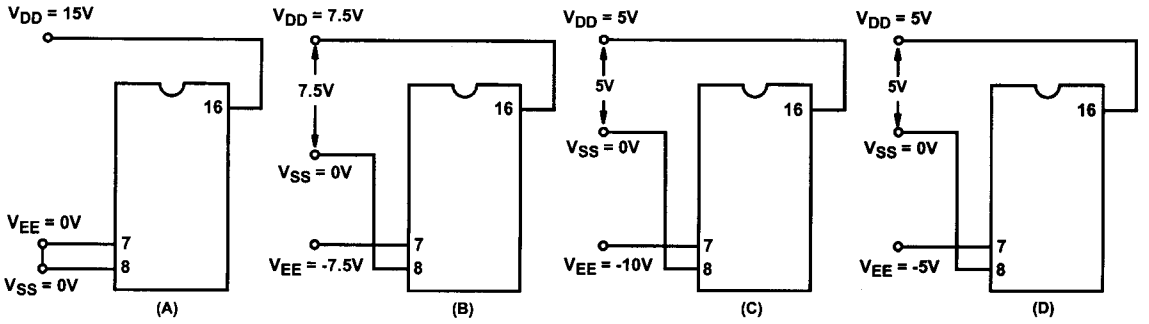


FIGURE 2. CHANNEL ON RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)

Test Circuits and Waveforms



NOTE: The ADDRESS (digital-control inputs) and INHIBIT logic levels are: "0" = V_{SS} and "1" = V_{DD}. The analog signal (through the TG) may swing from V_{EE} to V_{DD}.

FIGURE 9. TYPICAL BIAS VOLTAGES

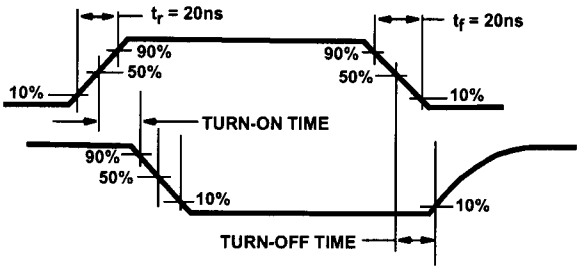


FIGURE 10. WAVEFORMS, CHANNEL BEING TURNED ON (R_L = 1kΩ)

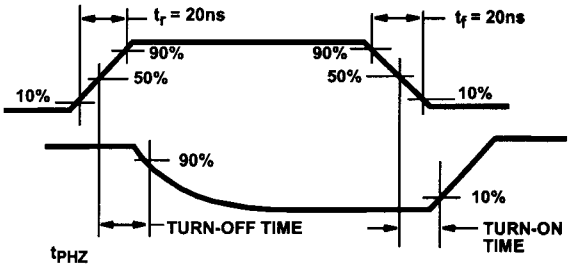


FIGURE 11. WAVEFORMS, CHANNEL BEING TURNED OFF (R_L = 1kΩ)

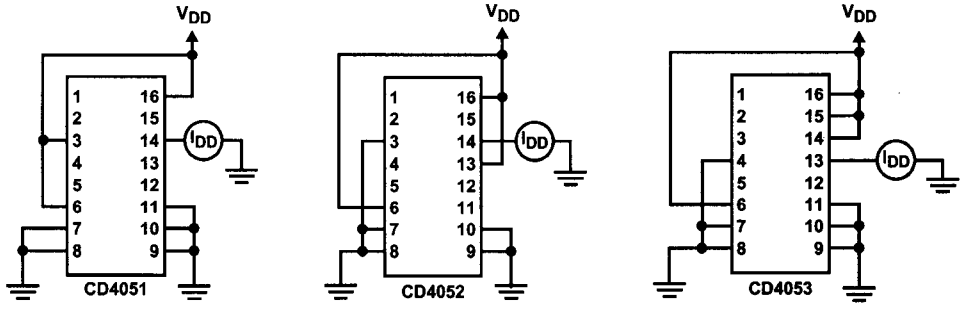


FIGURE 12. OFF CHANNEL LEAKAGE CURRENT - ANY CHANNEL OFF

Test Circuits and Waveforms (Continued)

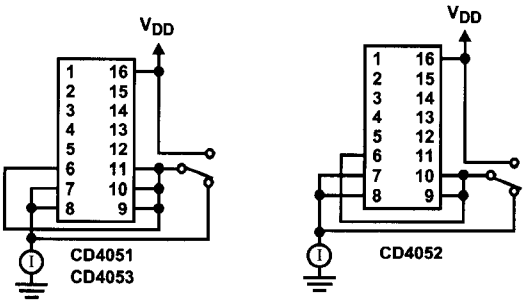


FIGURE 17. QUIESCENT DEVICE CURRENT

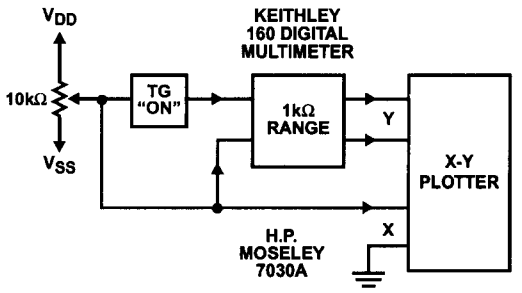
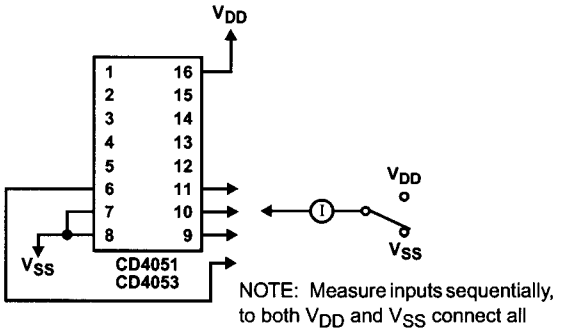


FIGURE 18. CHANNEL ON RESISTANCE MEASUREMENT CIRCUIT



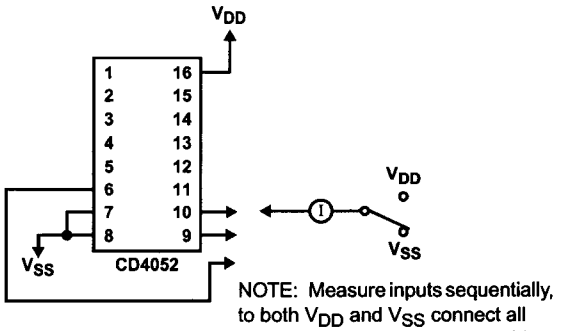


FIGURE 19. INPUT CURRENT

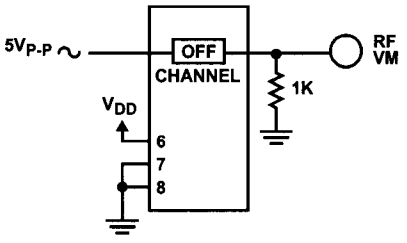


FIGURE 20. FEEDTHROUGH (ALL TYPES)

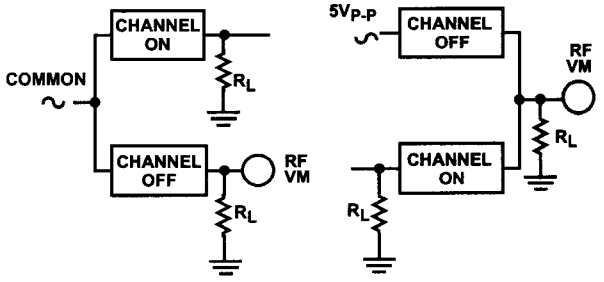


FIGURE 21. CROSSTALK BETWEEN ANY TWO CHANNELS (ALL TYPES)

FIGURE 22. CROSSTALK BETWEEN DUALS OR TRIPLETS (CD4052B, CD4053B)

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TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS044

CD4047B Types

CMOS Low-Power Monostable/Astable Multivibrator

High Voltage Types (20-Volt Rating)

■ CD4047B consists of a gatable astable multivibrator with logic techniques incorporated to permit positive or negative edge-triggered monostable multivibrator action with retriggering and external counting options.

Inputs include +TRIGGER, −TRIGGER, ASTABLE, $\overline{\text{ASTABLE}}$, RETRIGGER, and EXTERNAL RESET. Buffered outputs are $\overline{Q}$, Q, and OSCILLATOR. In all modes of operation, and external capacitor must be connected between C-Timing and RC-Common terminals, and an external resistor must be connected between the R-Timing and RC-Common terminals.

Astable operation is enabled by a high level on the ASTABLE input or a low level on the $\overline{\text{ASTABLE}}$ input, or both. The period of the square wave at the Q and $\overline{Q}$ Outputs in this mode of operation is a function of the external components employed. "True" input pulses on the ASTABLE input or "Complement" pulses on the $\overline{\text{ASTABLE}}$ input allow the circuit to be used as a gatable multivibrator. The OSCILLATOR output period will be half of the Q terminal output in the astable mode. However, a 50% duty cycle is not guaranteed at this output.

The CD4047B triggers in the monostable mode when a positive-going edge occurs on the + TRIGGER-input while the -TRIGGER is held low. Input pulses may be of any duration relative to the output pulse.

If retrigger capability is desired, the RETRIGGER input is pulsed. The retriggerable mode of operation is limited to positive-going edge. The CD4047B will retrigger as long as the RETRIGGER-input is high, with or without transitions (See Fig. 34).

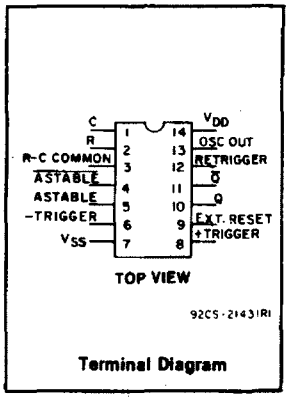
An external countdown option can be implemented by coupling "Q" to an external "N" counter and resetting the counter with the trigger pulse. The counter output pulse is fed back to the $\overline{\text{ASTABLE}}$ input and has a duration equal to N times the period of the multivibrator.

A high level on the EXTERNAL RESET input assures no output pulse during an "ON" power condition. This input can also be activated to terminate the output pulse at any time. For monostable operation, whenever V_{DD} is applied, an internal power-on reset circuit will clock the Q output low within one output period (t_M).

The CD4047B-Series types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

Features:

- *Low power consumption: special CMOS oscillator configuration*
- *Monostable (one-shot) or astable (free-running) operation*
- *True and complemented buffered outputs*
- *Only one external R and C required*
- *Buffered inputs*
- *100% tested for quiescent current at 20 V*
- *Standardized, symmetrical output characteristics*
- *5-V, 10-V, and 15-V parametric ratings*
- *Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"*



TOP VIEW

92CS-21431RI

Terminal Diagram

Monostable Multivibrator Features:

- *Positive- or negative-edge trigger*
- *Output pulse width independent of trigger pulse duration*
- *Retriggerable option for pulse width expansion*
- *Internal power-on reset circuit*
- *Long pulse widths possible using small RC components by means of external counter provision*
- *Fast recovery time essentially independent of pulse width*
- *Pulse-width accuracy maintained at duty cycles approaching 100%*

Astable Multivibrator Features:

- *Free-running or gatable operating modes*
- *50% duty cycle*
- *Oscillator output available*
- *Good astable frequency stability:*
  Frequency deviation:
  = ±2% + 0.03%/°C @ 100 kHz
  = ±0.5% + 0.015%/°C @ 10 kHz
  (circuits "trimmed" to frequency V_{DD} = 10 V ± 10%)

Applications:

Digital equipment where low-power dissipation and/or high noise immunity are primary design requirements:

- *Envelope detection*
- *Frequency multiplication*
- *Frequency division*
- *Frequency discriminators*
- *Timing circuits*
- *Time-delay applications*

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS MIN.	LIMITS MAX.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V
NOTE: IF AT 15 V OPERATION A 10 MΩ RESISTOR IS USED THE OPERATING TEMPERATURE SHOULD BE BETWEEN −25°C and 100°C			

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55°C to +100°C 500mW
For T_A = +100°C to +125°C ..... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

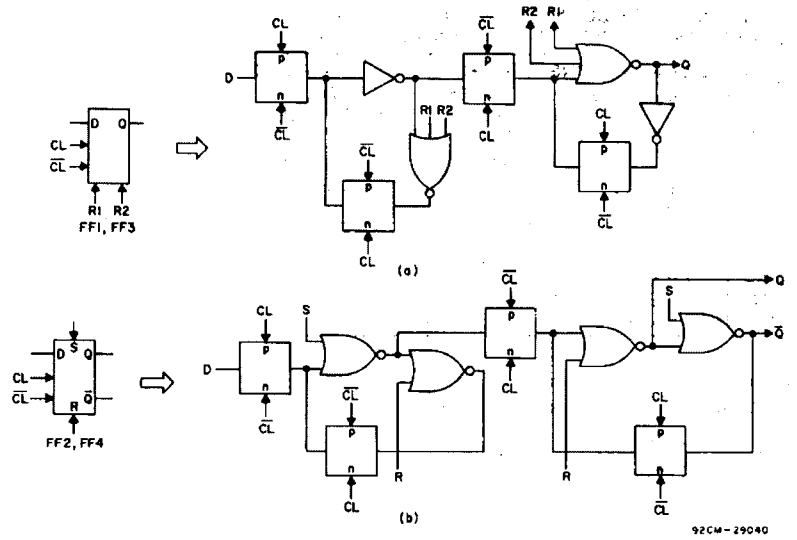


Fig. 3—Detail logic diagram for flip-flops FF1 and FF3 (a) and for flip-flops FF2 and FF4 (b).

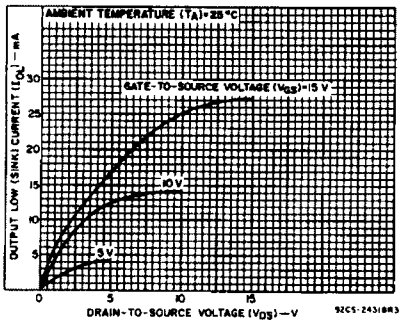


Fig. 4—Typical output low (sink) current characteristics.

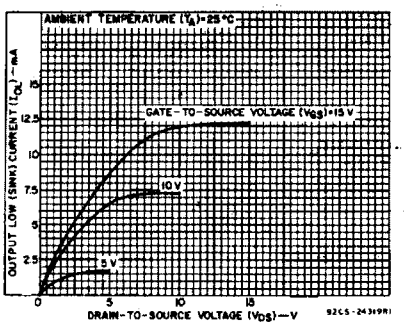


Fig. 5—Minimum output low (sink) current characteristics.

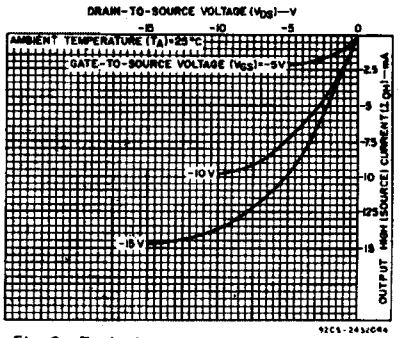


Fig. 6—Typical output high (source) current characteristics.

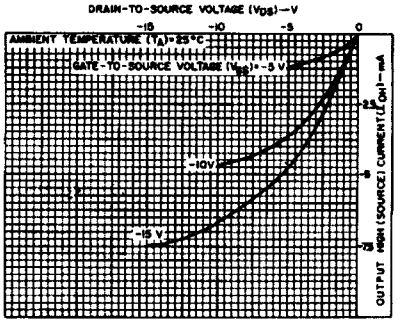


Fig. 7—Minimum output high (source) current characteristics.

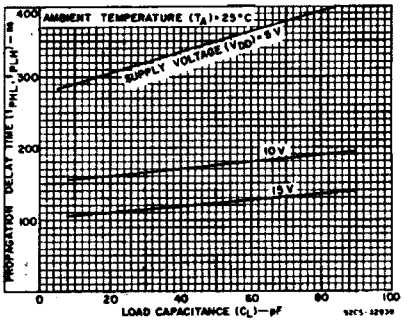


Fig. 8—Typical propagation delay time as a function of load capacitance (Astable, Astable to Q, $\overline{Q}$).

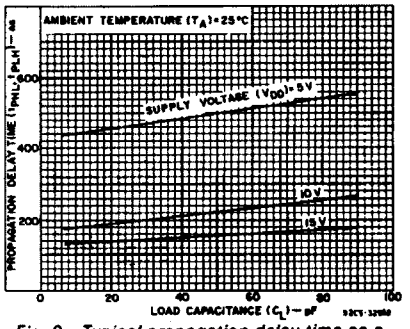


Fig. 9—Typical propagation delay time as a function of load capacitance (+ or − trigger to Q, $\overline{Q}$).

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	—	0,5	5	1	1	30	30	—	0.02	1	μA
	—	0,10	10	2	2	60	60	—	0.02	2	
	—	0,15	15	4	4	120	120	—	0.02	4	
	—	0,20	20	20	20	600	600	—	0.04	20	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	—	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	—	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	—	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	—	
Output Voltage: Low-Level V_{OL} Max.	—	0,5	5	0.05				—	0	0.05	V
	—	0,10	10	0.05				—	0	0.05	
	—	0,15	15	0.05				—	0	0.05	

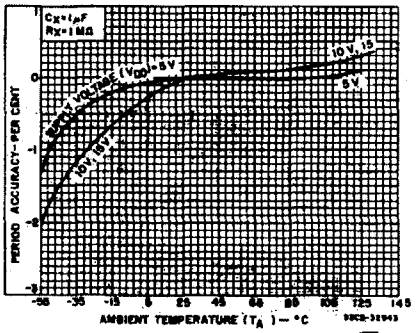


Fig. 14—Typical astable oscillator or Q, $\overline{Q}$ period accuracy vs. ambient temperature (ultra-low frequency).

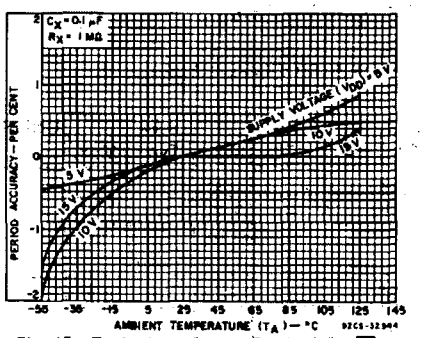


Fig. 15—Typical astable oscillator or Q, $\overline{Q}$ period accuracy vs. ambient temperature (low frequency).

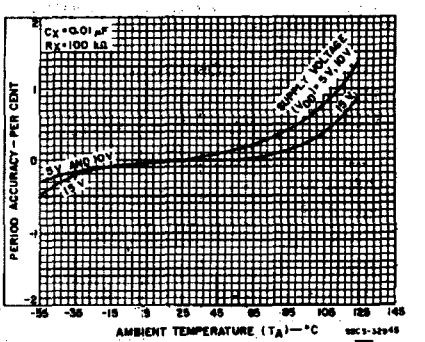


Fig. 16—Typical astable oscillator or Q, $\overline{Q}$ period accuracy vs. ambient temperature (medium frequency).

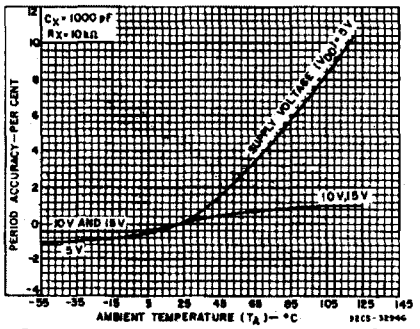


Fig. 17—Typical astable oscillator or Q, $\overline{Q}$ period accuracy vs. ambient temperature (high-frequency).

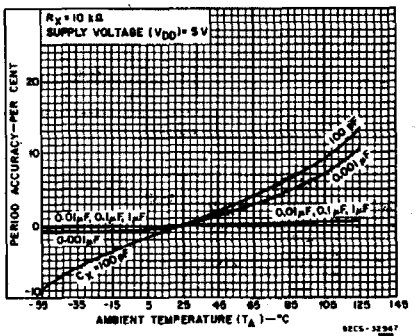


Fig. 18—Typical astable oscillator or Q, $\overline{Q}$ period accuracy vs. ambient temperature.

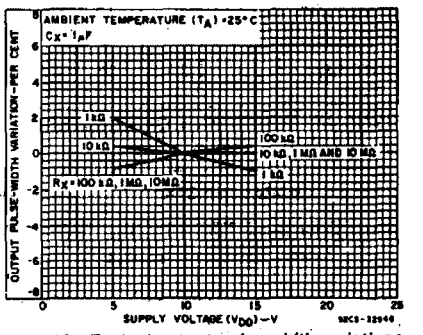


Fig. 19—Typical output pulse-width variations vs. supply voltage.

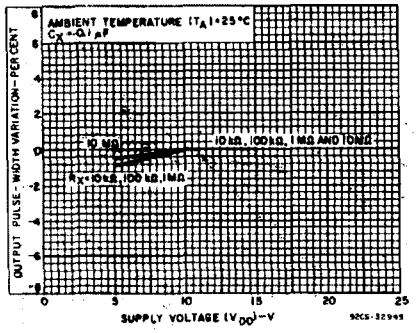


Fig. 20—Typical output pulse-width variations vs. supply voltage.

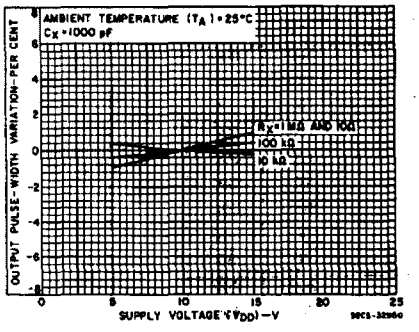


Fig. 21—Typical output pulse-width variations vs. supply voltage.

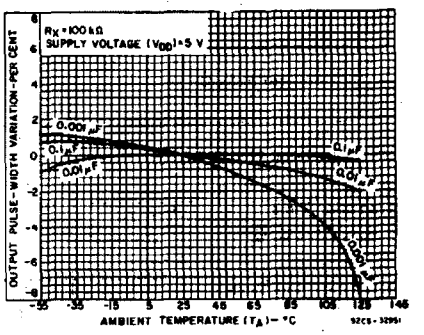


Fig. 22—Typical output pulse-width variations vs. ambient temperature.

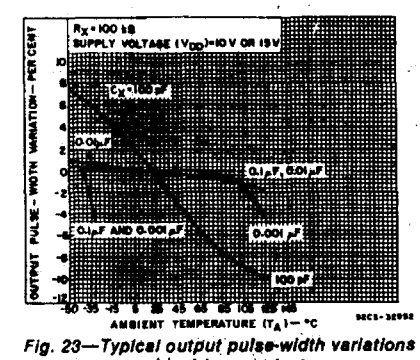


Fig. 23—Typical output pulse-width variations vs. ambient temperature.

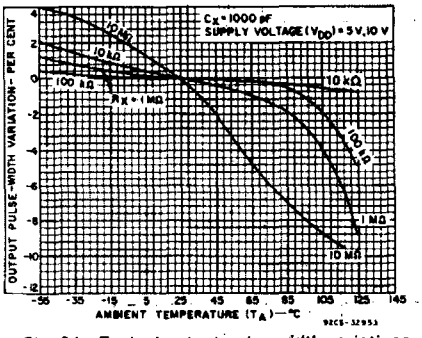


Fig. 24—Typical output-pulse-width variations vs. ambient temperature.

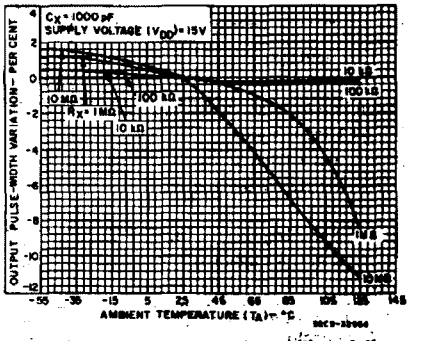


Fig. 25—Typical output pulse-width variations vs. ambient temperature.

III. Retrigger Mode Operation

The CD4047B can be used in the retrigger mode to extend the output-pulse duration, or to compare the frequency of an input signal with that of the internal oscillator. In the retrigger mode the input pulse is applied to terminal 12, and the output is taken from terminal 10 or 11. As shown in Fig. 34 normal monostable action is obtained when one retrigger pulse is applied. Extended pulse duration is obtained when more than one pulse is applied.

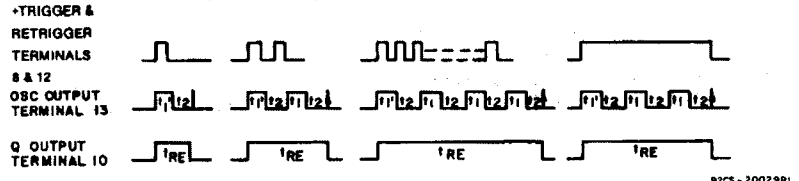


Fig. 34—Retrigger-mode waveforms.

For two input pulses, $t_{RE} = t_1' + t_1 + 2t_2$. For more than two pulses, the output pulse width is an integral number of time periods, with the first time period being $t_1' + t_2$, typically, 2.48RC, and all subsequent time periods being $t_1 + t_2$, typically, 2.2RC.

IV. External Counter Option

Time t_M can be extended by any amount with the use of external counting circuitry. Advantages include digitally controlled pulse duration, small timing capacitors for long time periods, and extremely fast recovery time. A typical implementation is shown in Fig. 35. The pulse duration at the output is

$$t_{ext} = (N - 1)(t_A) + (t_M + t_A/2)$$

where t_{ext} = pulse duration of the circuitry, and N is the number of counts used.

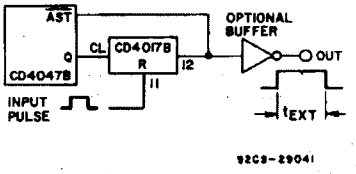


Fig. 35—Implementation of external counter option.

V. Timing-Component Limitations

The capacitor used in the circuit should be non-polarized and have low leakage (i.e. the parallel resistance of the capacitor should be at least an order of magnitude greater than the external resistor used). There is no upper or lower limit for either R or C value to maintain oscillation.

However, in consideration of accuracy, C must be much larger than the inherent stray capacitance in the system (unless this capacitance can be measured and taken into account). R must be much larger than the CMOS "ON" resistance in series with it, which typically is hundreds of ohms. In addition, with very large values of R, some short-term instability with respect to time may be noted.

The recommended values for these components to maintain agreement with previously calculated formulas without trimming should be:

$C \geq 100$ pF, up to any practical value, for astable modes;

$C \geq 1000$ pF, up to any practical value for monostable modes.

$10\ k\Omega \leq R \leq 1\ M\Omega$

VI. Power Consumption

In the standby mode (Monostable or Astable), power dissipation will be a function of leakage current in the circuit, as shown in the static electrical characteristics. For dynamic operation, the power needed to charge the external timing capacitor C is given by the following formulae:

Astable Mode:

$P = 2CV^2f$. (Output at terminal No. 13)

$P = 4CV^2f$. (Output at terminal Nos. 10 and 11)

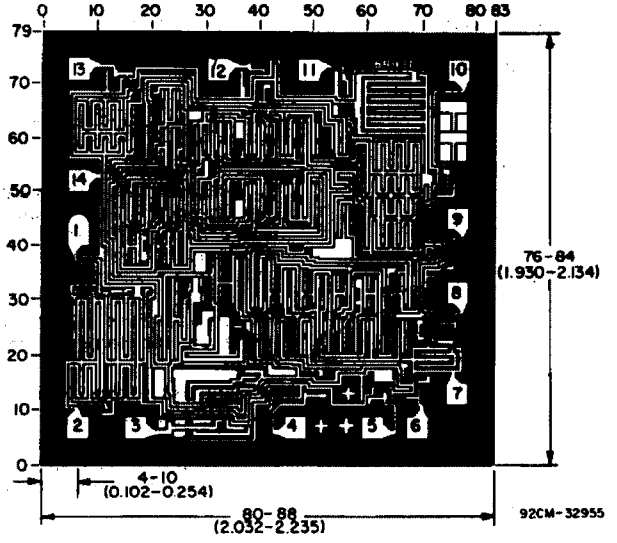
Monostable Mode:

$$P = \frac{(2.9CV^2)\ (\text{Duty Cycle})}{T}$$

(Output at terminal Nos. 10 and 11)

The circuit is designed so that most of the total power is consumed in the external components. In practice, the lower the values of frequency and voltage used, the closer the actual power dissipation will be to the calculated value.

Because the power dissipation does not depend on R, a design for minimum power dissipation would be a small value of C. The value of R would depend on the desired period (within the limitations discussed above). See Figs. 27, 28, and 29 for typical power consumption in astable mode.



Chip dimensions and pad layout for CD4047B

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

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6) Altera design handbook