PROJECT REPORT

SCROLLING ALPHANUMERIC LCD

WORK CARRIED OUT AT

RAMAN RESEARCH INSTITUTE, BANGALORE

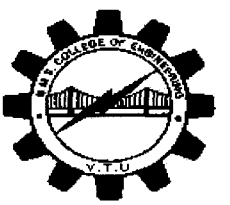
Submitted in partial fulfillment of the requirements of

Visveswariah Technological University, Belgaum for the award of

Bachelor of Engineering

in

Electronics and Communication



2002

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CERTIFICATE

This is to certify that the project work entitled

SCROLLING ALPHANUMERIC LCD

is a bonafide work carried out by

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In partial fulfillment for the award of degree of Bachelor of Engineering in Electronics and Communication of the Visveswaraiah Technological University, Belgaum during the academic year 2001 – 2002.
It is certified that all corrections/ suggestions indicated for Internal Assessment have been incorporated in the Report deposited in the department library. The project report has been approved as it satisfies the academic requirements in respect of Project work prescribed for the Bachelor of Engineering Degree.

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Certificate

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Acknowledgement

These few words of gratitude cannot in any way describe our deeply felt indebtness to the people involved in the successful completion of our project.

Every new venture faces many obstacles. The unflinching support provided by our guide Dr. T N Ruckmongathan with respect to the enormous technical assistance helped us weather these storms bravely. It was his sheer presence and constant encouragement that filled us with enthusiasm and courage without which we could not have completed this project successfully.

Our internal guide Mrs. L Swarnajyothi, probably had the most difficult job off all. She is the one who has been instrumental in moulding us right from the third semester onwards. Her excellent coaching in VHDL and other fields such as microprocessors has helped us tremendously right through this project and surely through the rest of our lives.

It was our wonderful Head of the Department, Mr. P A Ram Reddy whose meticulous help in providing the required facilities and encouragement helped us to work harder in making this project a success.

We would like to thank the management of Raman research Institute for having given us with an opportunity to really put to use all that we

have studied during the four years of our engineering studies, by providing us with this project. The excellent environment coupled with their everlasting support in all matters will be always appreciated.

Others at Raman Research Institute who have been of incredible help are Mr. Pani Kumar, Ms. Pratiti Biswas, Mr. Shashidhara and Mr. Govind Madhavan . They not only guided us throughout our project work but have also been excellent friends providing us with a real homely and warm work environment.

A special reference needs to be made about Mr. Nagraj of the Electronics Lab of Raman Research Institute without whose help it would probably have been impossible for us to learn and use OrCAD.

We would also like to take this opportunity to thank our Principal, Dr. Murugesh Mudaliar for his everlasting support in academic matters.

Last but not the least we would like to thank all the other teaching and no-teaching staff of our department who have at some time or the other have guided and helped us.

Organization Profile

The **Raman Research Institute** was founded by Nobel laureate **Sir C.V.Raman** in 1948 with funds from private sources. The main activity of the institute was basic research in selected areas of physics which were of particular interest to Prof. Raman. The institute owes its origin to action of government of Mysore in gifting to the Indian Academy of Sciences a plot of land in Bangalore in December 1934. In the year 1956, Prof. Raman made an irrevocable gift to the Indian Academy of Sciences, of various movable and immovable properties for the use and the benefit of the Raman Research Institute.

After Prof. Raman's death in November, 1970, The Indian Academy of Sciences created in July 1971 a public charitable educational trust by the name Raman Research Institute Trust(RRI Trust). The Academy transferred to the trust the lands, buildings, deposits, securities, bank deposits, moneys, laboratories, instruments and other movable and immovable properties held by it for the purpose of RRI. One of the main objectives of the RRI Trust is principally to maintain, conduct and sustain the Raman Research Institute.

The institute was reorganized in 1972 and started receiving funds from the Department of Science and Technology of the Government of India. The institute is administered by a Governing Council.

Currently, the main areas of research are Astronomy and Astrophysics, Liquid Crystals, Theoretical Physics and Optics.

The present director of the institute is Prof. N Kumar.

Liquid Crystals has been an active area of research at the Raman Research Institute for nearly three decades. The research programme covers a broad spectrum of activities ranging from the synthesis of

new liquid crystalline materials to display electronics. Discoveries of the columnar phase formed by disc-like molecules and pressure induced mesomorphism are two of the early significant contributions made by the liquid crystal group. Recently, two new liquid crystalline phases, namely the undulating twist grain boundary C phase and the biaxial smectic A phase have been discovered in the laboratory. Addressing techniques for driving passive matrix liquid crystal displays developed here are now widely used. In recent years the group has also been working on electrochemical aspects of surface science and on other soft materials like surfactants, polymers, and on the physics of biological systems.

Abstract

The Binary Addressing Technique (BAT) is an addressing technique wherein all the lines to be multiplexed are simultaneously selected instead of one line at a time as done usually in the technique of line-by-line addressing. This technique requires simple addressing waveforms but is only suitable when the number of lines (N) to be multiplexed is small and the selection ratio requirement is not very high. It also has another advantage in that it naturally makes the addressing waveforms dc-free.

In BAT all the N rows to be multiplexed are selected simultaneously with voltage levels $\pm V_t$ corresponding to 1 or 0, so that the voltage pattern applied to the rows corresponds to an N digit binary number. This is compared with the binary pattern to be displayed in a given column and the column voltage is decided as $+V_c$ or $-V_c$ such that a majority of rows get a favorable voltage. Now, the row select pattern is changed to a new N-digit binary number and the process is continued until all the 2^n possible combinations are exhausted, and the cycle is then repeated.

Our project employs the Binary Addressing Technique (BAT) to drive eight, 5 x 7 matrix LCDs (using the liquid crystal material RO-TN-132) in order to form a **scrolling LCD to display alphanumeric data**. We are implementing the BAT technique and the drivers required on Erasable Programmable Logic Devices(EPLDs). Also Printed Circuit Boards (PCBs) have been designed and fabricated to mount the drivers and also to provide for mounting of the LCDs.

INTRODUCTION

Introduction

The information processing capability of electronic circuits has grown manifold over the past couple of decades, affecting our lives immensely. The speed and power with which information processing is done has reached unprecedented levels. In this scenario the interface between the human and the processor, that is, the display device plays a critical role.

Till quite recently, the cathode ray tube (CRT) has been the only choice in all display devices such as televisions and desktop computer monitors as it was cheap and provided excellent image quality. However the CRT occupies a large volume, and consumes a fair amount of power (~ 100W), and a large reduction in either of these attributes of CRTs is not expected. Flat panel displays (FPDs) save space and among the various possible devices, the liquid crystal displays (LCDs) have the low power consumption (~ 1μW /cm^2 of displayed area). LCDs made a humble beginning in early 1970's by replacing the power hungry LEDs in digital watches and calculators. As portable computers (laptops, palmtops etc.) became a reality, LCD technology progressed rapidly to match their needs and now all such portable devices invariably use LCDs. The quality of thin-film transistor (TFT) addressed LCD is easily comparable to that of a CRT and, LCDs are now being used in a wide range of applications.

A typical LCD consists of an array of display elements or picture elements (pixels) arranged in the form of an X-Y matrix. The arrangement of these pixels is similar to that of memory elements in a two dimensional memory array. The pixels should have non-linear

electro-optic characteristics so that they can be selectively addressed by a method known as matrix addressing or multiplexing. The effectiveness of a display depends largely on the efficiency of a pixel as an electro optic transducer and the addressing technique employed. For this reason considerable research is being directed towards the development of new electro optic effects and new liquid crystal materials.

The Twisted Nematic LCDs (TNLCDs) and the Super Twisted Birefringence Effect Displays (SBE Displays) are among the most popular displays.

The common features relevant to the addressing of these displays are given below:

- Non-linear electro-optic characteristics
- Long response times (~100 mS)
- Identical response to both positive and negative electric fields

Hence, TNLCDs and SBE Displays exhibit **rms** response to the applied electric field.

Some important characteristics desirable in addressing techniques for LCDs are :

- Good Discrimination between the ON and OFF pixels to ensure a good contrast ratio in the display.
- DC-free Operation; the display should be addressed with ac fields to ensure its long life

- Low amplitude of addressing waveform to ensure lower supply voltage requirement of the drive electronics.
- Good Pixel Uniformity and Ease of Implementation.

The following approaches are possible for addressing matrix LCDs:

- **Direct Multiplexing,** wherein the intrinsic non-linear characteristics of the pixels are exploited; this is used in many applications including computer terminals, in which the information to be displayed is bilevel (the pixels are either **on** or **off**).

- **Active matrix addressing,** wherein an extrinsic non-linear element is incorporated in association with each pixel; this is commonly used in small area TV displays, in which gray scale and color are important in addition to having a large number if pixels. The Direct Multiplexed displays are popular because of their simple construction, high yield, and low cost.

1.1 Liquid Crystal Materials

The liquid crystalline phase was discovered by an Austrian botanist, Friedrich Reinitzer, in the year 1888. He found that **cholesteryl benzoate,** unlike many of the organic compounds known at that time exhibited two distinct melting points. Later it was found that many organic materials melt from the solid state to form a turbid liquid, which on further heating undergo a second transition leading to a clear isotropic liquid. The intermediate state between the solid and the isotropic liquid has some properties of both crystalline and liquid phases. This was therefore termed as the liquid crystalline phase. This phase is often called a mesophase or a mesomorphic phase. The materials, which exhibit this phase, are called liquid crystals, mesomorphic substances or mesomorphs.

Liquid crystals are broadly classified into two types as given below:

- Thermotropic liquid crystals, which are obtained either by heating or cooling certain organic materials whose molecules have pronounced non-spherical shapes;

- Lyotropic liquid crystals, which are obtained by dissolving certain solids in appropriate solvents.

Of these, the thermotropic liquid crystals are used in display applications.

1.1.1 Classifications

Thermotropic liquid crystals are classified into four main categories depending on the molecular arrangement as given below:

- **Nematic liquid crystals.** They are the simplest and widely used in practical applications. The rods like molecules are approximately parallel to one another and hence exhibit orientational order. However, they do not have positional order.
- **Cholesteric liquid crystals.** They exhibit orientational order. However, the director rotates continuously about a helical axis with a characteristic pitch. This rotation is due to the presence of one, or more chiral centers within the molecules. The nematics can be considered as a special case of cholesteric liquid crystals with an infinite pitch.
- **Smectic liquid crystals.** They are closer to the solids as they exhibit one-dimensional positional order as well as positional order. Smectics are further classified into subgroups, viz., smectic-A to smectic-H, depending on the ordering within and between the layers.
- **Columnar liquid crystals**. They exhibit a two-dimensional positional order leading to a closely packed flexible columnar structure. The disc-like molecules are piled on each other to form the columns.

1.1.2 Nematic Liquid Crystals

The simplest liquid crystal is the nematic (N), in which the rod-like molecules have no periodic structure, but remain approximately parallel to one another, i.e., have a long-range orientational order (Figure 1.1).

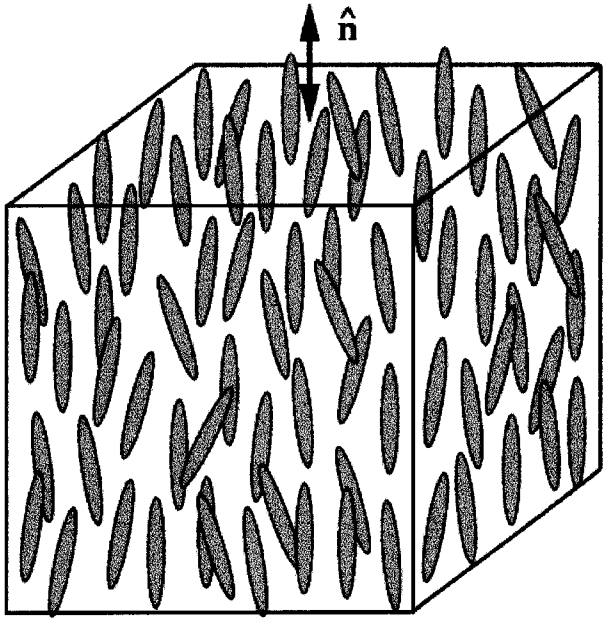


Figure 1.1 Nematic Liquid Crystals

The orientational order generates elasticity in the medium. Unlike the familiar elastic response against elongation or compression of solid materials, the nematic has *curvature* elasticity in which the *orientation* of the director resists spatial gradients. This weak curvature elasticity leads to the low operating voltages of LCDs. The nematic liquid flows easily, i.e. it is not viscous, hence it has a low response time for switching on and switching off the displays.

1.1.3 Physical Properties

The liquid crystal materials should have a proper combination of physical properties for a satisfactory operation of the display. Hence, only a small percentage of the thousands of liquid crystal materials are suitable for display devices. Moreover, none of the single liquid crystal materials known so far, has all the properties required for the display. Hence, it is common practice to use mixtures of a number of liquid crystal materials.

A typical nematic liquid crystal (NLC) material consists of two rings (phenyl or cyclohexyl) connected by bridging group and two end groups. Typical end groups are -CN, -NO_2 or short alkyl chains. The NLC mixtures should have a stable composition over a wide temperature range.

1.1.4 Electro – Optic effects in Liquid Crystals

Liquid crystal materials exhibit anisotropy in many of their physical properties. Moreover, they are sensitive to relatively weak external stimuli. Hence, electric field, magnetic field or thermal energy can be utilized to induce optical effects in liquid crystals. These effects are mainly due to the reorientation of the molecules resulting in absorption, reflection or scattering of light. Practical displays need uniformly oriented and stable layers of molecules with appropriate electrical, optical, elastic and thermal properties. LCDs require a very low power to operate, since they do not emit light and small external stimuli can induce a large change of orientation of the liquid crystal molecules.

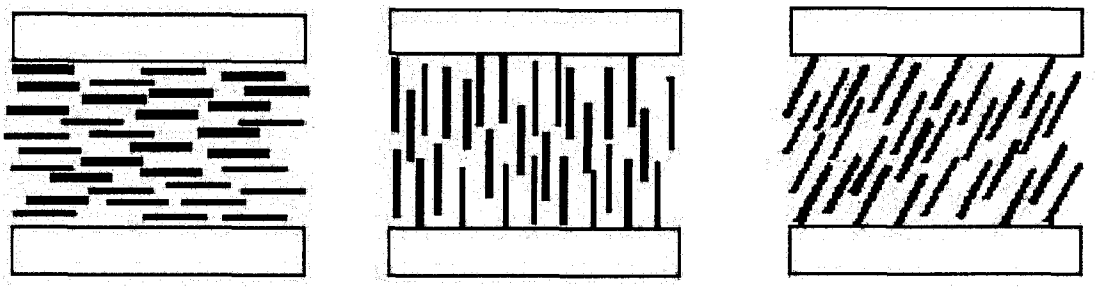
Salient features of the electro-optic effects in liquid crystals are given below: -

- Low voltage operation ;
- Low power consumption;
- Legibility in high ambient light;
- Flexible format;
- Flat panel construction; and
- Choice of size.

1.1.5 Display Cell

A display cell consists of thin layer of liquid crystal materials sandwiched between two glass plates. Most of the electro-optic effects in liquid crystals require a uniformly aligned liquid crystal cell. This is achieved by aligning the molecules at the inner surfaces of the cell and can be one of the following types:

- **Planar or homogeneous** alignment. The orientation of the director is parallel to the surfaces of the glass plates. This is obtained by coating the surface with a thin layer of polyimide and buffing the surface uni-directionally with a cloth or tissue paper
- **Perpendicular or homeotropic** alignment. The orientation of the director is perpendicular to the surface of the glass plate and is obtained by chemical treatment of the glass surface.
- **Tilted** alignment. Here, the director is at an angle to the surface of the glass plate. A tilted arrangement can be obtained by coating the surface with SiO or MgF_2 at a suitable oblique angle in a vacuum coating unit.



Planar Alignment Perpendicular Alignment

Tilted Alignment

Figure 1.2. Types of surface alignment

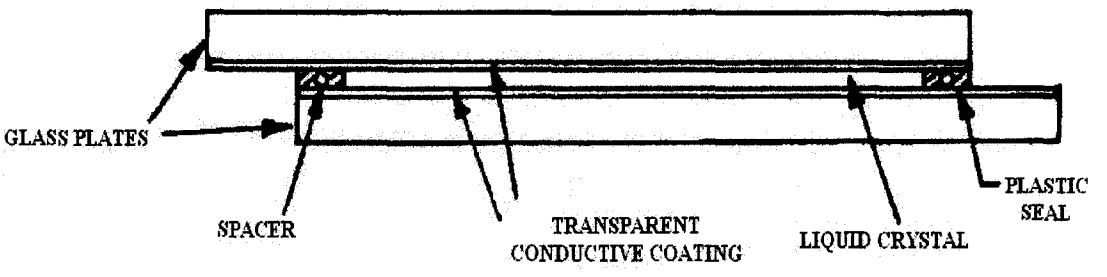


Figure1.3. Cross-section of a display cell

1.2 Twisted Nematic Liquid Crystal Displays (TNLCDs)

The twisted nematic liquid crystal display (TNLCD) cell is made up of two glass plates treated for planar alignment. The cell is assembled such that the direction of the alignment in the top plate is perpendicular to that in the in the bottom plate of the cell. The display cell is filled with a NLC mixture having a positive dielectric anisotropy. The liquid crystal molecules confined in the cell form a 90° twisted structure as shown in the figure. This twisted structure acts like a waveguide and gradually rotates the plane of polarization by 90°. Hence, a linearly polarized light incident on the cell emerges linearly polarized in an orthogonal direction when the following conditions are satisfied:

- The plane of polarization of the incident light is parallel or perpendicular to the director at the surface of the cell; and
- The product of the optical anisotropy(Δn) and the pitch(P) is high compared to the wavelength of the incident light, where P is four times the thickness of the cell.

The cell in the unexcited state (OFF) rotates the plane of polarization of the incident light by 90°. Hence, the cell appears –

- Dark, when viewed between two polarizers parallel to each other; and
- Transparent, when viewed between two polarizers perpendicular to each other.

The 90° twist in the cell is lost when a sufficiently strong electric field is applied to the cell (ON). Hence, the cell appears –

- Transparent between two parallel polarizers; and
- Dark between two perpendicular polarizers.

The difference in transmission between the unexcited and excited states is exploited in TNLCDs. Only one optical mode is excited here by placing the polarizers parallel or perpendicular to the director at the surface of the cell.

TNLCDs require a low power to operate ~ 1□W/cm^2□power since they modulate the incident light and do not emit light. A voltage in the range of 2 - 5 V is adequate to excite the **ON** pixels.

The TNLCDs can be of the following types:

- **Transmissive** type with the light source at the back and the observer in front of the display. This type of display is preferred for use in dark environments.

- **Reflective** type with both the light source and the observer in front of the display. A polarizer with a reflector is used at the back of the display. This type of display is suitable for use in well-lit, bright environment; and

- **Trans-Reflective** type with a transreflector instead of a reflector at the back. This type of display is suitable for both dark and bright environments. The transreflector allows sufficient light from the

back illumination to fall on the display, for a good readability in a dark environment.

The displays can be operated in one of the following modes:

- Positive Contrast Mode with dark symbols against a bright background. This is achieved by placing the top and bottom polarizers perpendicular to each other in TNLCDs; and
- Negative Contrast Mode with bright symbols against a dark background. . This is achieved by placing the top and bottom polarizers parallel to each other in TNLCDs

A positive contrast mode is preferred in a reflective type of display, while a negative contrast mode is preferred in a transmissive type of display.

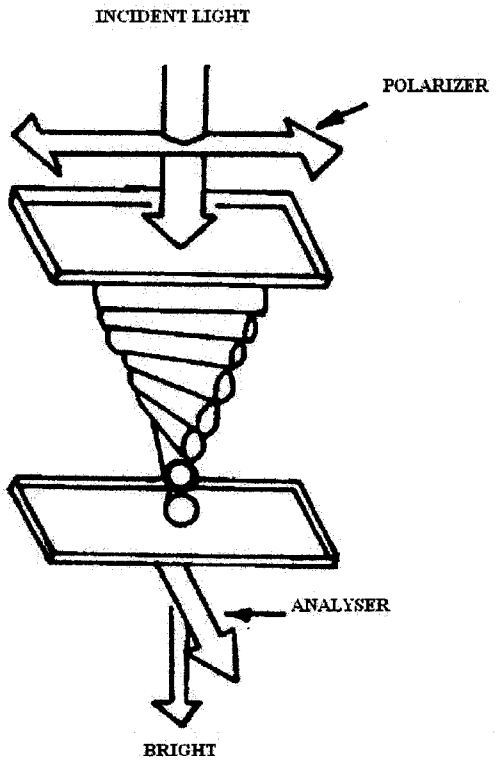


Figure (a)

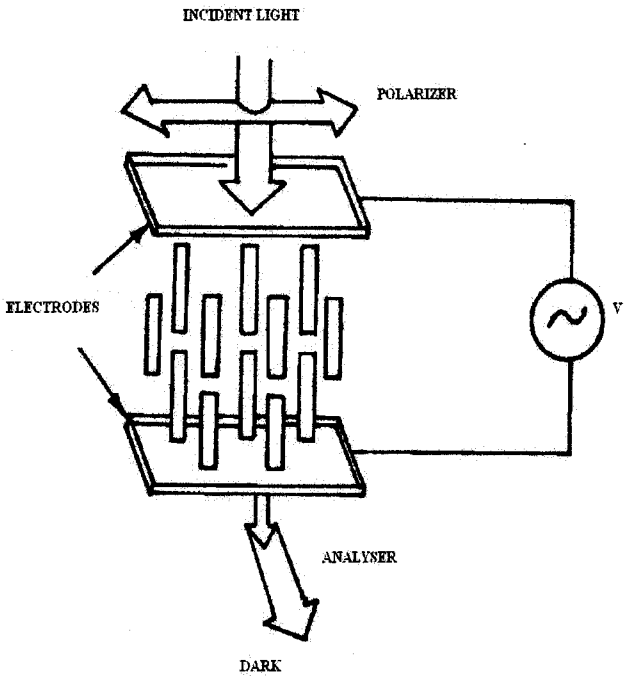


Figure (b)

Figure 1.4. Twisted Nematic Cell. (a) OFF, (b) ON states.

1.2.1 Electro – Optic Response of TNLCDs

The TNLCDs respond equally well to both positive and negative voltages. However, the life of the display is reduced due to irreversible electro-chemical reactions if they are driven with a dc field. Hence, the TNLCDs are normally driven with an ac field. They are slow responding devices with the response time in the range of 10-100 ms. Hence, the electro-optic response is determined by the rms voltage rather than the instantaneous voltages. The electro-optic response is described by the following parameters: -

- **Threshold Voltage (V_{th})**

  The threshold voltage is the voltage below which further change in the optical characteristic is relatively small, i.e., the voltage at which the luminance has changed by 10% of the maximum change in luminance (V_{th} or V_{10})

- **Saturation Voltage (V_{sat})**

  The saturation voltage is the voltage above which further change in the optical characteristic is relatively small, i.e., the voltage at which the luminance has changed by 90% of the maximum change in luminance (V_{sat} or V_{90}).

- **Contrast ratio**

  The ratio of the luminance of a liquid crystal device in the bright state to that in the dark state under conditions of contrast illumination.

- **Response Time**

  The response times with reference to the excitation us as shown in the figure

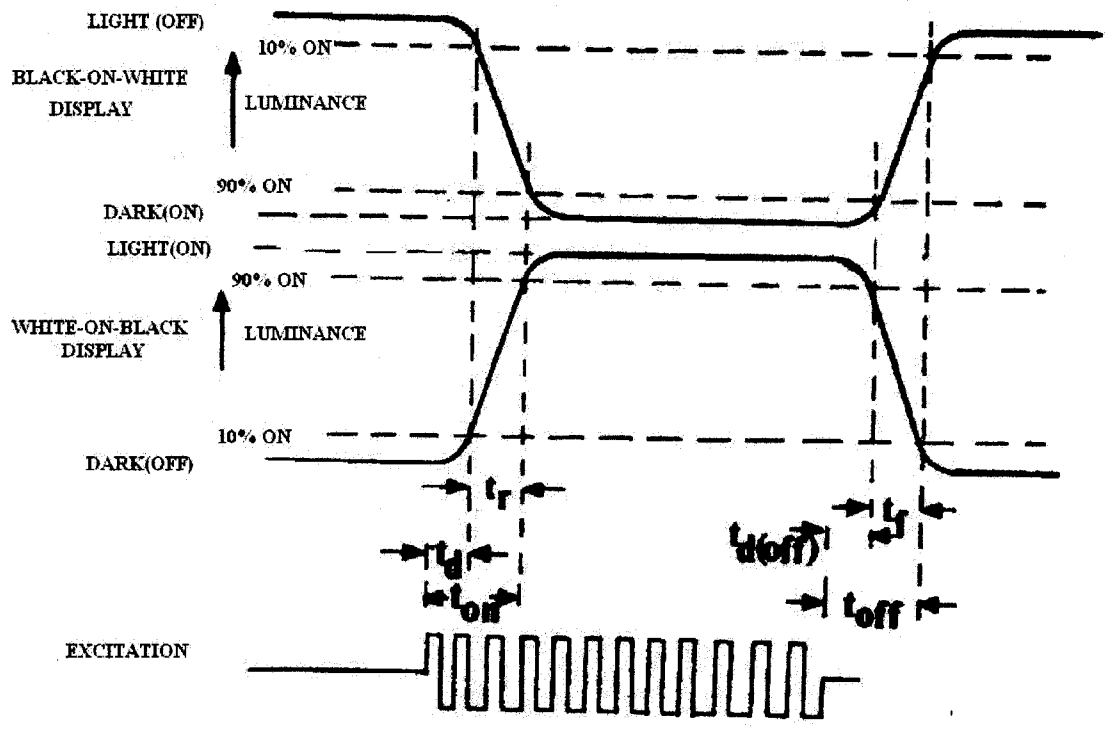


Figure 1.5. Response Time

- **Delay Time (t_d)** is the time interval between the initiation of the input pulse train and the luminance reaching its 10% as shown in the figure
- **Rise Time (t_r)** is time interval during which the luminance is changing from its 10% - **ON** value to its 90% - **ON** value as shown in the figure.
- **Turn -On -Time (t_{on})** is the sum of t_d and t_r.
- **Turn - Off -Delay Time ($t_{d(off)}$)** is the time interval between the end of the input pulse train and the luminance reaching 90% -**ON** value. Usually its negligible compared to the fall time.
- **Fall Time (t_f)** is the time interval during which the luminance is changing from its 90% - **ON** value to its 10% - **ON** value as shown in the figure.
- **Turn -Off-Time (t_{off})** is the sum of $t_{d(off)}$ and t_f..

1.3 Matrix Display and Multiplexing

1.3.1 Matrix Display

A display is made up of a number of picture elements (pixels) as shown in the Figure 1.6.

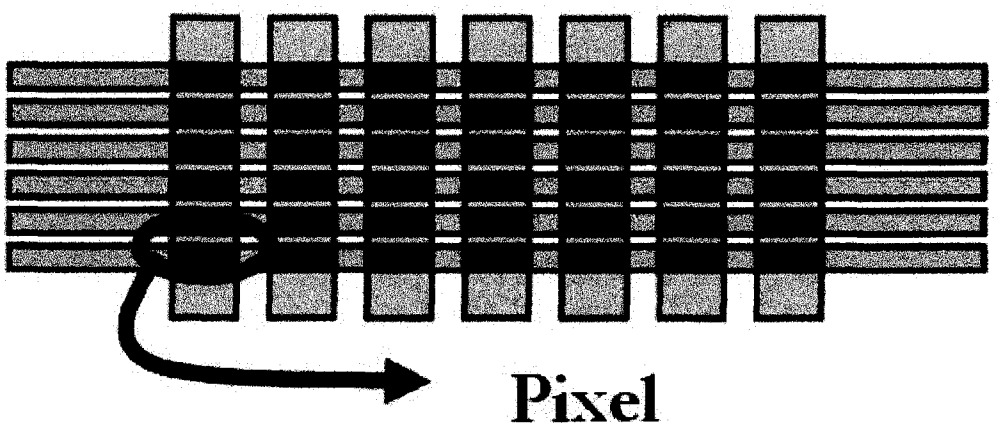


Figure 1.6. A Pixel

The intersection of a row and a column uniquely defines a pixel. A pixel in the row i and column j is represented by P_{ij}. Figure (a) gives the schematic diagram of a matrix display. The size of the pixel determines the resolution of the display. An image can be faithfully displayed if the intensity of each pixel can be controlled independently. In a display with a limited number of pixels, each pixel can be directly connected to the drive electronics (drivers). Hence the pixels are driven to the desired state without affecting the other pixels. This approach is called direct drive or static drive. However, if the number of pixels is very large as in a VGA (Vector Graphics Array) display say,

then it is not possible to connect each pixel separately to the drive electronics. This problem is surmounted by using the matrix display and the technique used for driving such displays is called matrix addressing or multiplexing. A matrix display with N rows and M columns has N*M pixels while the number of connections is just (N+M). A row address line connects one terminal of the pixels in a given row while a column address line is connected to the other terminal of pixels in a given column. Thus a pair of row and column address lines uniquely define a pixel located at the intersection of these address lines. The intrinsic non-linear electro-optic characteristics of the LCD are exploited in driving matrix panels with moderate complexity and such displays are called Passive Matrix LCDs (PMLCD). If the matrix is large, a non-linear device like a thin film transistor is incorporated with each pixel. These displays are called Active Matrix LCDs (AMLCD). Other non-linear elements like diodes or MIM (metal-insulator-metal) have been used in the past in the Active Matrix LCDs.

The equivalent circuit of a pixel is just a capacitor. The electrical conductance of the liquid crystal is very low and the capacitance of the pixel depends on the dielectric constant of the liquid crystal material, size of the pixel and the cell gap of the pixel. The two terminals of a pixel are connected to the drive electronics (see Figure .b). The response of the liquid crystalline material is independent of the polarity of the electric field. Although LCDs can be driven by a DC (direct current) field, this will result in migration of ionic impurities to the electrodes in the display. Application of a DC field over a long period of time leads to electrochemical reactions near the electrodes resulting in loss of alignment of the molecules and permanent damage to the cell.

Hence LCDs are always driven by AC (alternating current) fields to ensure a long life of the display. The shape of the AC field is not very important since the liquid crystals respond relatively slowly to the applied electric field. Hence the instantaneous variations in the electric field are not important for the overall response of a pixel but they contribute to the energy delivered to the pixels. The root-mean-squared (RMS) value of the field determines the state of the pixels as long as the period of the waveform is small compared to the response time of the LCD. While we can drive a pixel with sine, triangular or any other arbitrarily shaped waveforms, square or pulse shaped waveforms are preferred since they are easy to generate. LCDs are low power devices and it is important to make sure that the drive electronics do not consume excessive power. Complimentary Metal Oxide Semiconductor (CMOS) devices are well suited for driving LCDs since they consume very little power to operate.

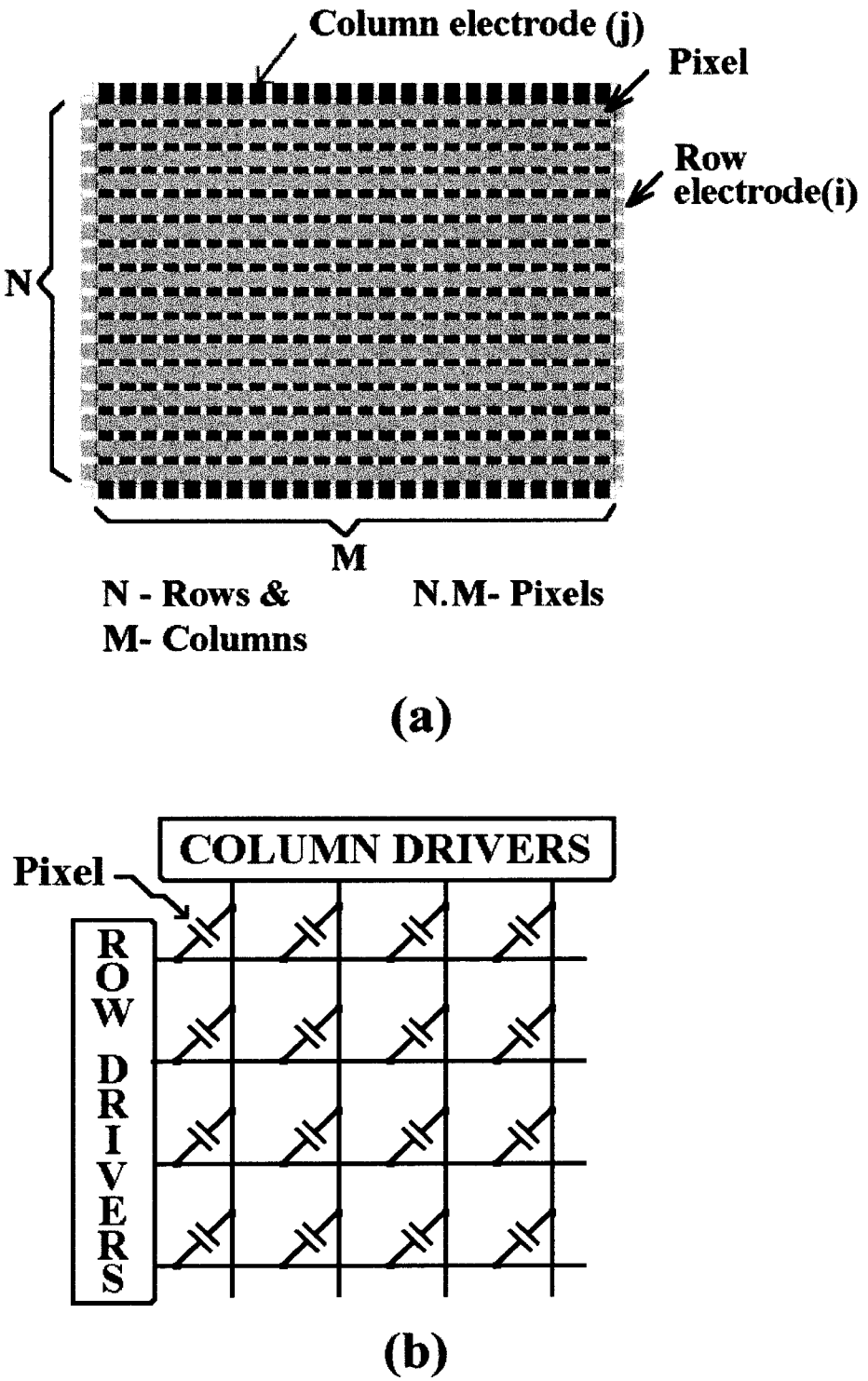


Figure 1.7. Column and Row Drivers

1.3.2 Fonts and Formats

The resolution required in a display is a function of the viewing distance. A person with average eyesight can easily resolve two points subtending at an angle of 1 minute of arc at the eye. This demands at least 12 pixels/mm at a viewing distance of 250 mm. Such a high density of pixels is not only difficult to achieve in display technologies but will be too expensive for many applications. Around 900 pixels are required to display a single character with the size and resolution found in a printed text. The cost of the display, drive electronics and the associated circuits will be high to achieve this resolution. Alphanumeric displays in most of the practical applications use simpler fonts for technical and economical reasons.

The pixels in the LCDs are formed by the intersection of electrode patterns on the top and bottom glass plates of the display cell. Hence, the electrode pattern must be designed such that they intersect only at the pixel and not anywhere else in the active area. The pixels in the Alphanumeric displays are usually interconnected to form a matrix display,

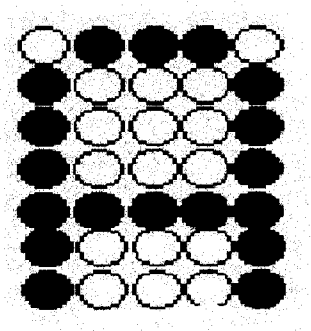


Figure 1.8. 5 x 7 dot matrix

if the number of pixels is large. The electrode pattern on the glass plates forms the pixels as well as the address lines. The 5 x 7 dot matrix font as shown in the Figure 1.8. is an ideal one for display of Alphanumeric, and special characters. The entire ASCII character set for the 5 x 7 dot matrix font is available in Appendix 1.

1.3.3 Multiplexing

A display should be capable of displaying any information. Hence, it should be possible to activate the selected pixels without altering the state of the other pixels. The process of transmitting information to all the pixels and hence activating the appropriate ones is called **addressing**. A line-by-line addressing is used in matrix displays based on many technologies including LCDs. The information to be displayed in a column (or row) is time multiplexed through a single column (or row) address line. This addressing technique is commonly referred to as multiplexing or matrix addressing. A signal applied to a column for activating a pixel in a selected row appears across all the pixels connected to that column. Hence, the display elements should have non-linear characteristic if they are to be multiplexed. The main advantages of multiplexing are as follows:

- A reduction in the number of connections to the display ;
- A reduction in the number of display drivers; and
- Increase in the readability.

However, the performance of a multiplexed display may be limited by the shortcomings in the non-linear characteristics of the display device. But , multiplexing becomes the natural choice when the number of pixels in a display is large, in spite of this drawback.

The matrix displays make use of the intrinsic non-linearity present in the display device. This approach is not suitable when the non-linear characteristics in a display device are:

- Totally absent ; or
- Not adequate for a given application.

Multiplexing is then made possible or enhanced by incorporating a non-linear element with each pixel in the matrix display. The non-linear element can be one of the following devices:

- Varistor
- Diode
- Metal-Insulator-Metal (MIM) device
- Thin Film Transistor (TFT)

Matrix displays fabricated with non-linear elements are usually called **active matrix displays**. The term active in this context refers to the presence of an **extrinsic** non-linear element only. The active matrix approach is becoming popular now-a-days because of the following developments:

- Reduction in the number of steps required for the fabrication of the non-linear devices;
- Introduction of redundancy techniques to improve the yield.

However, multiplexing using the intrinsic non-linearity is still attractive due to its inherent simplicity and cost effectiveness.

1.3.4 Electro-optic response of LCDs

The performance of the display in terms of the contrast, gray shades and response time depends on the electro-optic response of the LCD as well as the addressing technique used to drive the display. A non-zero threshold voltage and a sharp electro-optic characteristic are essential in the case of passive matrix LCDs.

1.3.5 Important display parameters

In addressing a passive matrix display, the intrinsic non-linear characteristics of the electro-optic response are exploited. Sharpness of the electro-optic response, angle of viewing, the selection ratio (of the drive technique) and the response times are the important parameters that decide the performance of the display.

Threshold voltage (V_{th}) is the voltage at which the light transmission through the cell begins to change. The Voltage beyond which there is a negligible change in light transmission is called the saturation voltage V_{sat} ..

Sharpness of the electro-optic characteristic is a measure of the slope of the electro-optic response expressed as $(V_x-V_{10})/V_{10}$. Here, V_x is the voltage necessary to achieve x% (usually x is either 50% or 90%) transmission in the display.

Selection ratio is defined as the ratio of the RMS voltage across an ON pixel (V_{ON}) to that of an OFF pixel (V_{OFF}). Selection ratio together with the sharpness determines the contrast in a passive matrix display.

Contrast is the ratio of the brightness of the ON to that of the OFF pixel. The selection ratio is infinite for the static drive since the OFF pixel gets zero voltage. Hence the sharpness parameter is not important when the display is driven by static drive .It is also not important in active matrix displays since the RMS voltage across any pixel can be controlled independently and the selection ratio is infinite.

Response time of the display is another parameter of interest especially in video applications. The turn ON delay, rise time, turn OFF delay and the fall time determine the response time of the display. Switching times between gray shades should also be considered while displaying graphics. The change in contrast depending on the angle of viewing is another important characteristic of the display. The viewing angle is usually small in a multiplexed display as compared to a display using static drive. The contrast in LCDs also depends upon the quality of polarizers (both transmission as well as the polarization efficiency), reflection of light at the various surfaces in the display cell, light leakage through the area surrounding the pixels and the brightness of the back light if any as well as its uniformity.

1.4 Addressing of the passive matrix LCDs

Passive matrix displays have a simple panel structure. The intersections of the row and column electrodes form the pixels. The electrodes are also called the address lines as they are connected to the row and column drivers. The N row and M column electrodes form N*M pixels with just (N+M) connections to the drivers. The number of connections to the matrix display is a minimum when N=M and the pixels form a square matrix. The techniques used for driving matrix LCDs are similar to multiplexing in communication engineering and hence the matrix addressing is also called multiplexing. The conventional line by line addressing of matrix LCDs is based on time division multiplexing. One set of address lines is used to sequentially select one line at a time, while the other set of address lines is used to multiplex the data (or information) to be displayed in all the pixels in the corresponding address line. The scanned electrodes are often called rows for simplicity. The data electrodes are generally referred to as the column electrodes. The non-linear electro-optic response of the liquid crystal displays is essential for driving a passive matrix LCD.

1.5 Desirable Characteristics of Addressing Techniques

The following characteristics are desired in addressing techniques for driving matrix displays with an rms response.

- The cross talk should be minimized
- The rms voltage across all the ON pixels and similarly across all the OFF pixels should be equal for a uniform appearance of the display

Considering the non-linear transmission characteristics of TNLCDs, ideally the

1) Voltage across the OFF pixels, i.e., $V_{off}(rms) \leq Vth$; and
2) Voltage across the ON pixels, i.e., $V_{on}(rms) \geq Vsat$.

- The selection ratio, i.e., $R = [V_{on}(rms) / V_{off}(rms)]$ should be high. This ensures a good discrimination between the ON and OFF pixels, resulting in a good contrast ratio of the display;
- The addressing technique should lead to a dc-free operation, in order to ensure the long life of the display;
- The supply voltage should be low for the following reasons:-

1) LCDs are mostly used in portable products; and

2) Regular CMOS ICs can be directly used without any need for development of high voltage drivers, leading to considerable economy.

3) The addressing technique should be simple. Apart from the elegance, this leads to a simple control circuit and hence will be reliable and economical.

4) The addressing technique should have the flexibility to match the display characteristics.

Keeping the above details in mind we shall now see the theory behind the addressing technique used by us, viz. Binary Addressing Technique (BAT) in the next chapter.

BINARY ADDRESSING TECHNIQUE (BAT)

Binary Addressing Technique(BAT)

The binary addressing technique follows a totally different approach to multiplex a matrix display as compared to the conventional techniques based on line-by-line addressing. All the lines to be multiplexed are simultaneously selected in *BAT* instead of one line at a time as in the case of line-by-line addressing.

2.1 Background

The following conditions are satisfied in a matrix display used for numeric and alphanumeric applications: -

- Individual pixels are in two states only, i.e., either *ON* or *OFF*, and
- The data to be displayed in a column is a N-bit binary pattern.

Hence, the N rows to be multiplexed in a matrix display can as well be simultaneously selected with voltages corresponding to an N -bit binary pattern. In general, the row select voltages can be $\pm V_r$ and the column voltages can be $\pm V_c$. The voltages across a pixel, for the various combinations of the row and column voltages are given in the table 2.1. Only the voltage amplitudes are considered here since LCDs respond to both positive and negative voltages.
The following conditions are desired in a multiplexed display:

- All the *OFF* pixels should get as low voltage as possible across them, and
- All the *ON* pixels should get as large a voltage as possible across them.

Table 2.1. Pixel voltages for different Row and Column Voltages

Row Voltage	Column Voltage	Resultant Voltage across a pixel
$-V_r$	$-V_c$	$-(V_r - V_c)$
$-V_r$	$+V_c$	$-(V_r + V_c)$
$+V_r$	$-V_c$	$+(V_r + V_c)$
$+V_r$	$+V_c$	$+(V_r - V_c)$

Hence a pixel is said to get a favorable voltage when,

- The *OFF* pixel has a voltage $|V_r - V_c|$ across it ; or
- The *ON* pixel has a voltage $|V_r + V_c|$ across it.

The voltage pattern across the pixel in a column in general corresponds to either,

- The row- select pattern itself, when the sign of the column voltage is same as that of row-select voltage for logic 0, or
- The complement of the row-select pattern, when the sign of the column voltage is same as that of row-select voltage for logic 1, when $|V_r - V_c|$ and $|V_r + V_c|$ are assigned logic 0 and logic 1 respectively.

In general, the data pattern will be different from the row select pattern or its complement. Hence, some of the pixels in a column will get an unfavorable voltage.

The unfavorable voltage or error in this context means, either the voltage is,

- out-of-phase with row-select voltage for an *OFF* pixel, resulting in a voltage of $|V_r + V_c|$ instead of $|V_r - V_c|$ across it, or
- in-phase with the row-select voltage for an ON pixel, resulting in a voltage of $|V_r - V_c|$ instead of $|V_r + V_c|$ across it.

The presence of an unfavorable voltage across a pixel can be tolerated in a multiplexed display for the following reasons:

- TNLCDs respond to the rms voltage rather than the instantaneous voltage, due to their slow response time. Hence, the presence of an unfavorable voltage across n pixel does not turn *ON* or turn *OFF* the pixel, as long as its duration is smaller than the response time of the display, and
- TNLCDs respond to the external electric field, only above a threshold voltage (V_{th}). Hence, the *OFF* pixels can accommodate a voltage beolw V_{th} without being turned *ON.*

However, the presence of an error either,

- increases the rms voltage across the *OFF* pixel, or
- decreases the rms voltage across the *ON* pixel.

This leads to a decrease in the selection ratio from the ideal value, i.e., infinite, A similar situation is encountered in the line-by-line addressing due to the presence of the column voltage across the pixels in the unselected rows. Hence the number of errors should be minimum for a given pixel. The number of errors in a column can be 0-N depending on the data and the row-select patterns. However, this can be reduced to be less than or equal to (N/2) by a proper choice of the sign of the column voltage. The number of errors in each pixel will be different for the following reasons:

- the number of mismatches and hence the error depends on both the row-select and the data patterns, and
- the data pattern is different for each column.

The rms voltage across the pixels in the same state should be equal in order to ensure display uniformity. This is possible only when the number of errors is equal for the pixels in the same state. This can be achieved by selecting rows with, all the 2^N binary patterns one after the other for an equal duration of time. The number of errors for each pixel in the display is the same and it increases with the value of N. This leads to a decrease in the selection ratio as the number of rows (N) in the matrix increases. This is similar to that of the conventional line-by-line addressing techniques, wherein the decrease in selection ratio with the increase in N is due to the increase in the duration of the column voltage appearing across the pixels when the corresponding voltages are unselected.

2.2 Technique

The data to be displayed in a column is an N-bit word and is represented by

$d_1,d_2,d_3,.....d_n$; d_j = 0 or 1

wherein, logic 0 or logic 1 represented *OFF* and *ON* pixels respectively.

Similarly the row-select pattern is an N-bit word and is represented by

$a_1,a_2,a_3,.....a_n$; a_j=0 or 1

The various steps involved in BAT are given below.

1) An N-bit word is chosen as row selected as row-select pattern. The row-select voltages are chosen to be zero for logic 0 and V_s for logic 1;
2) The row-select and data patterns are compared bit-by-bit using digital comparators, viz., exclusive-or gates;
3) The number of mismatches *i* between these two patterns is determined by counting the number of exclusive-or gates with logic 1 output;
4) The column voltage V_c is decided by a majority decision. The column voltage is zero (logic 0) if *i* is less than N/2 and is V_s if *i* is greater than N/2.

The steps (2) – (4) can be summarized as follows: -

$$i = \sum_{j=1}^{N} aj \oplus dj$$

and

V_c = 0 for i < (N/2)

V_s for i > (N/2)

The condition i = (N/2) is avoided in this majority decision by choosing N to be odd;

5) The column voltages for each column in the matrix are determined independently by repeating the steps (2) – (4) ;
6) Both the row-select and the column voltages are applied simultaneously to the matrix display for a time duration T;
7) A new row-select pattern is chosen and the column voltage is determined for this by using steps (2) – (5). The new row and column voltages are applied simultaneously to the matrix display for an equal duration of time at the end of T;
8) A cycle is completed when all the 2^N binary patterns are covered as row selected as row select patterns once; and
9) Repeating this cycle continuously refreshes the display.

The steps involved in BAT are summarized in the following figure2.1.

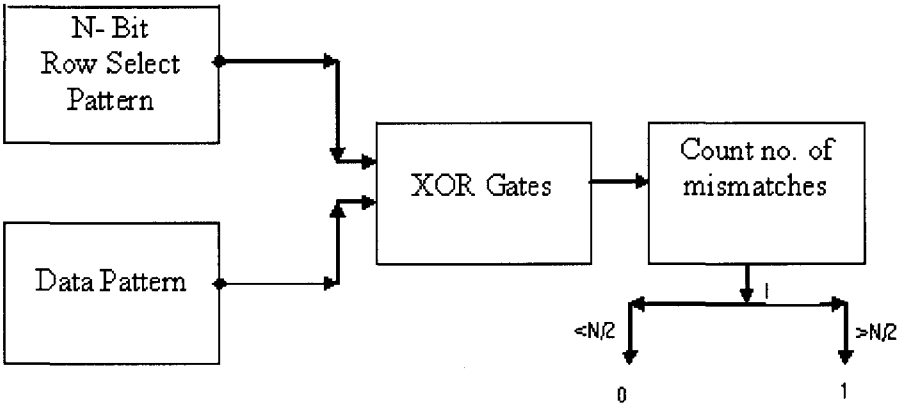


Figure 2.1. Technique employed in BAT

The time duration should be small compared to the response time of the display in order to ensure the rms behavior of the display.

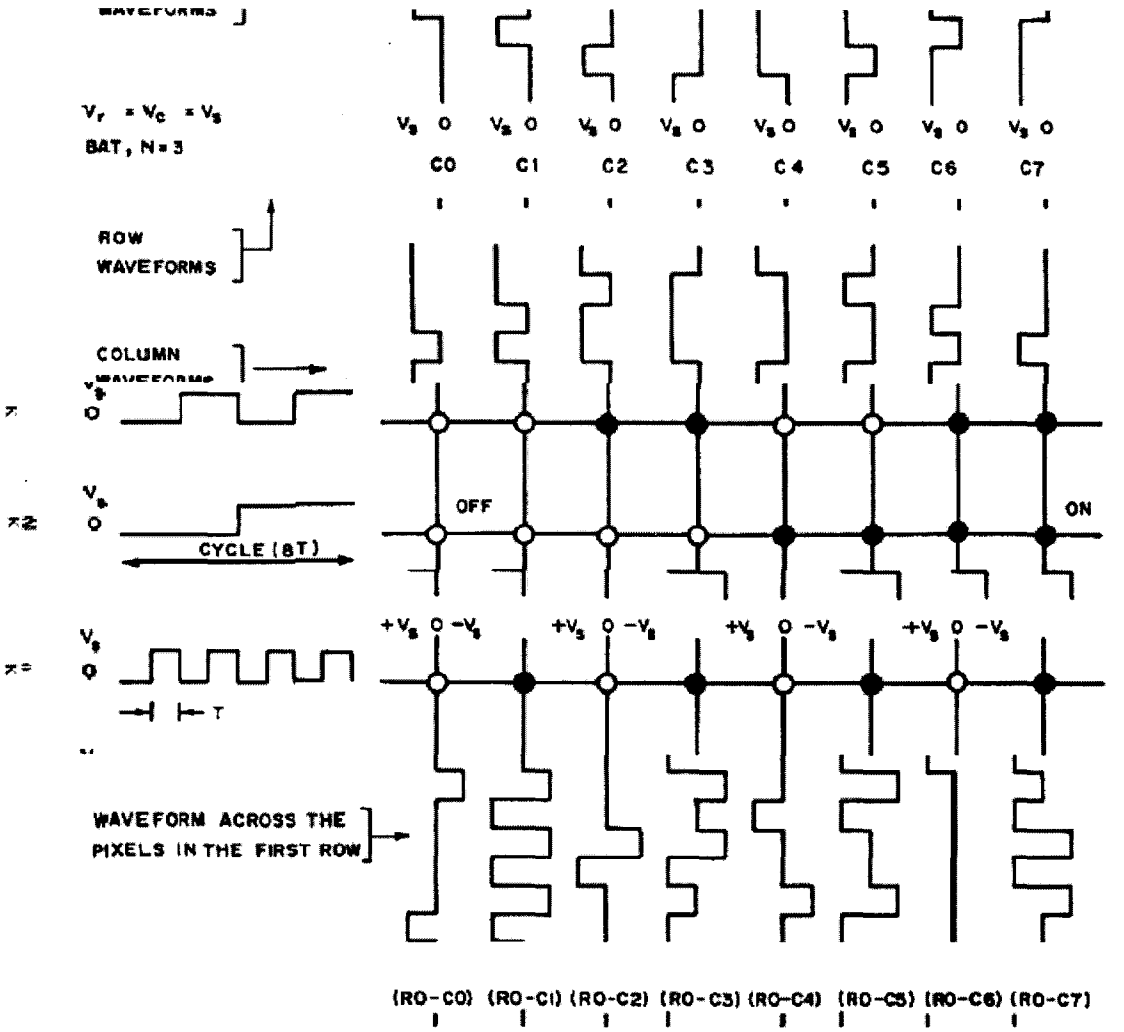
The column voltages for all the combinations of the row-select and data patterns, for N = 5 is shown in table 2.2 as an example. From this table , it is evident that the column voltage is-

- Complemented when either the row-select pattern or the data pattern is complemented; or
- The same when both the row-select and data patterns are complemented.

Typically addressing waveforms of BAT for N =3 are as shown in Figure 2.2.The row waveforms R0-R2 form the eight binary row-select patterns. The column waveforms required to display the eight data patterns (C0 – C2) are shown here. The waveforms across the pixels in the first tow are also included in this figure, to illustrate the inherent dc-free operation of BAT.

Data Patterns / Row Select Voltages	d5	d4	d3	d2	d1
	0	1	1	1	1	1	1
	1	0	0	0	1	0	0
	1	0	0	0	1	0	0
	1	0	0	0	1	0	0
	0	1	1	1	1	1	1
a5 a4 a3 a2 a1							
0 0 0 0 0	1	0	0	0	1	0	0
0 0 0 0 1	1	0	0	0	1	0	0
0 0 0 1 0	0	1	1	1	1	1	1
0 0 1 0 0	0	1	1	1	1	1	1
0 1 0 0 1	1	0	0	0	1	0	0
1 0 0 1 0	1	0	0	0	1	0	0
0 0 1 0 1	1	0	0	0	1	0	0
0 1 0 1 1	0	1	1	1	0	1	1
1 0 1 1 0	0	1	1	1	0	1	1
0 1 1 0 0	0	1	1	1	0	1	1
1 1 0 0 1	1	0	0	0	0	0	0
1 0 0 1 1	1	0	0	0	0	0	0
0 0 1 1 1	0	1	1	1	0	1	1
0 1 1 1 1	0	1	1	1	0	1	1
1 1 1 1 1	0	1	1	1	0	1	1
1 1 1 1 0	0	1	1	1	0	1	1
1 1 1 0 0	0	1	1	1	0	1	1
1 1 0 0 0	1	0	0	0	1	0	0
1 0 0 0 1	1	0	0	0	1	0	0
0 0 0 1 1	1	0	0	0	1	0	0
0 0 1 1 0	0	1	1	1	1	1	1
0 1 1 0 1	0	1	1	1	0	1	1
1 1 0 1 1	1	0	0	0	0	0	0
1 0 1 1 1	1	0	0	0	0	0	0
0 1 1 1 0	0	1	1	1	0	1	1
1 1 1 0 1	1	0	0	0	0	0	0
1 1 0 1 0	0	1	1	1	0	1	1
1 0 1 0 1	1	0	0	0	0	0	0
0 1 0 1 0	0	1	1	1	1	1	1
1 0 1 0 0	1	0	0	0	1	0	0
0 1 0 0 0	0	1	1	1	1	1	1
1 0 0 0 0	1	0	0	0	1	0	0

Figure 2.2 Typical addressing waveform of BAT



2.3 Analysis

Let the number of rows (N) be odd, and the row-select voltage be $-V_r$ for logic 0 and $+V_r$ for logic 1. Only one column need be considered for the purpose of analysis, since the data is multiplexed through the column line. The number of errors per pixel during a cycle is calculated as follows:-

The number of N-bit row-select patterns which differ from the N-bit data pattern by i bits is given by

$$C_i = \frac{N}{i!(N-i)!}$$

In this context, C_i gives the number of row-select patterns with i mismatches. The number of mismatches per pixel when there are i mismatches in the column is given by

$$B_i = \frac{iC_i}{N}$$

The number of times a pixel gets a favorable voltage when the C_i row-select patterns with i mismatches are considered is given by,

$$A_i = \frac{(N-1)!}{i!(N-i-1)!}$$

The summation of Ai and Bi over I ranging from 0 to (N-1)/2 gives the number of times a pixel gets a favorable voltage and error respectively during the $2^{(N-1)}$ time intervals considered. The maximum value of error is $\frac{(N-1)}{2}$ since N is odd here. Hence,

$$A = \sum_{i=0}^{(N-1)/2} \frac{(N-1)!}{i!(N-i-1)!}$$

and

$$B = \sum_{i=0}^{(N-1)/2} \frac{i(N-1)!}{i!(N-i)!}$$

Hence, a pixel will get a favorable voltage during 2A time intervals in a cycle. Similarly a pixel will get an unfavorable voltage or error during 2B time intervals in a complete cycle. The expression for the rms voltage across the ON and OFF pixels are arrived at using the above statistics and the definitions of favorable and unfavorable voltages.

$$V_{ON(rms)} = \sqrt{\frac{[2.A.T(Vr + Vc)2 + 2.B.T(Vr\ \ Vc)\,2\,]}{2N.T}}$$

and

$$V_{OFF(rms)} = \sqrt{\frac{[\,2.A.T(Vr - Vc)2 + 2.B.T(Vr + Vc)\,2\,]}{2N.\,T}}$$

The selection ratio(R) given by V_{ON}(rms)/ V_{OFF} (rms) should be maximum, in order to achieve a good discrimination between the ON and OFF pixels in the display. Here, the selection ratio is a maximum for $\frac{V_r}{V_c} = 1$

Hence, the number of voltage levels in the addressing waveform is just two. A dc-free operation is ensured independent of the polarity of the row and column voltages since every row-select pattern has its compliment within the 2^N combinations. Hence, unipolar addressing waveforms with two voltage levels, i.e., 0 and V_s are sufficient in BAT. The maximum selection ratio is

$$R = \frac{V_{ON(rms)}}{V_{OFF(rms)}} = \sqrt{\frac{A}{B}}$$

The selection ratio can also be expressed in terms of A and B using the relation below.

$$[A+B] = 2^{(N-1)}$$

Hence,

$$R = \sqrt{A/(2^{(N-1)} - A)} = \sqrt{(2^{(N-1)} - B)/B}$$

The OFF pixels are biased close to V_{th} so as to obtain the best contrast ratio in the display. Hence the voltage V_r (= V_c) can be determined in terms of V_{th} as follows.

$$V_{OFF} = V_{th} = \sqrt{\frac{(2^{(N-1)} - A).2^2}{2(N-1)}} .V_c$$

Therefore,

$$V_c = \sqrt{\frac{2^{(N-3)}}{2^{(N-1)} - A}}.V_{th}$$

The maximum swing in the addressing waveforms is $2V_c$ since, the column voltages were assumed to be $+V_c$ and $-V_c$. Hence, the supply voltage for this technique is

$$V_s = 2.V_c = \sqrt{\frac{2^{(N-1)}}{2^{(N-1)} - A}}.V_{th}$$

The supply voltage requirement of BAT can also be expressed in terms of B as follows:

$$V_s = \sqrt{\frac{2^{(N-1)}}{B}}.V_{th}$$

The addressing waveforms of BAT can be made unipolar by shifting them by $+V_c$ (= $+V_r$). Hence, the row and column voltages are 0 for logic 0 and V_s for logic 1.

The supply voltage for BAT is lower when compared to other techniques primarily due to the large duty cycle of this technique. The pixels get a favorable voltage during 2A time intervals in a single cycle. The duty cycle for BAT is thus given by,

$$\text{Duty Cycle} = \frac{2A}{2^N} = \frac{A}{2^{(N-1)}}$$

2.4 Discussion

The merits and demerits of BAT are listed in the table 2.3. This technique is not suitable for displays with a large number of lines (N), since the number of time intervals to complete a cycle ($=2^N$) increases rapidly with N. The lower selection ratio of BAT is not a serious problem from the following considerations: -

- This technique is suitable only for small values of N, and
- The contrast ratio in the display need not be compromised, since NLC mixtures that are suitable for multiplexing more than 64 lines are available at present.

MERITS

- Simple addressing waveforms with just two voltage levels;
- Standard CMOS ICs usable for row and column driving;
- Natural dc-free operation;
- Low supply voltage;
- Large duty cycle;

DEMERITS

- Not suitable for multiplexing displays with large N;
- Selection ratio lower as compared to IAPT;
- N to be odd.

Table 2.3. Merits and Demerits of BAT

This ends the discussion on the theoretical aspects of BAT. The practical implementation of the project will be covered in the next chapter.

IMPLEMENTATION

Implementation

The theoretical background of Binary Addressing Technique (BAT) was explained in the preceding chapter.

The hardware realization of, **"A Scrolling Alphanumeric LCD"** is taken up in this chapter. The BAT will be used to refresh this display. The functional block diagram is explained first to be followed by the details of implementation.

3.1 Block Diagram

The Binary Addressing Technique (BAT) is suitable for alphanumeric displays wherein the number of lines to be multiplexed (N), is small. The Block Diagram of a display system using the BAT is shown below in Figure 3.1.

The character information is stored in the memory using the standard ASCII(American Standard Code for Information Interchange) set for storing alphanumeric characters to be displayed.

The Character Generator(CG) converts the ASCII code to the pixel information.. The 2^N row-select patterns required for BAT are obtained from the Sequence Generator. The Column Signal Generator(CG) compares the data from the CG and the row-select patterns from the Sequence Generator bit-by-bit and generates the data fro the Column Drivers. This requires a majority decision as discussed in the theory of BAT in the preceding chapter. The Row Drivers obtain the row-select pattern from the Sequence Generator. The row-select pattern and the data pattern should be simultaneously applied to the matrix display. This is ensured by providing a buffer and a latch in both the row and column drivers. The Control Logic synchronizes the display refresh, by generating appropriate address and control signals using a clock.

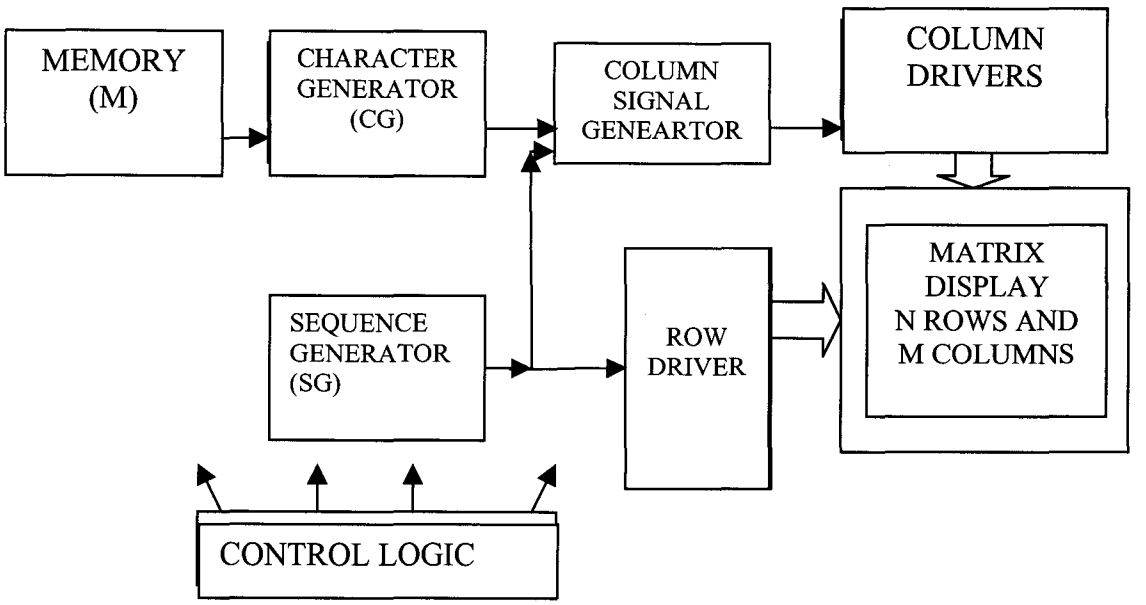


Figure 3.1. Block Diagram of BAT display system.

3.2 Approach to realization

Keeping the above block diagram of the BAT display system in mind, a block diagram for the "Scrolling Alphanumeric LCD" is as shown in Figure 3.2.

This Block Diagram consists of the following blocks:

1) Memory(Text to be displayed / ASCII information)

An EPROM is used here to store the ASCII information of the characters to be displayed. The controller is designed such that it can handle a maximum of 256 characters.

2) Character Generator(CG)

A second EPROM is used to store the pixel information required to display the characters on the LCD. The pixel information has been generated for the 5x7 display font. The upper three bits of the pixel information are "dont care" and hence ignored.An example of the pixel information for the character "A" is shown below in figure 3.3.

3) Sequence Generator (PRBS Generator)

An N-bit binary counter could have been used to generate the row-select pattern required for BAT, but this has a few inherent difficulties in that the frequency of the counter increases from MSB to LSB by a factor of two for each bit. This large variation in the frequency of the row addressing waveforms leads to brightness non-uniformity of the pixels(contrast variation). Though the Gray Code sequence provides a better alternative a PRBS sequence is preferred.

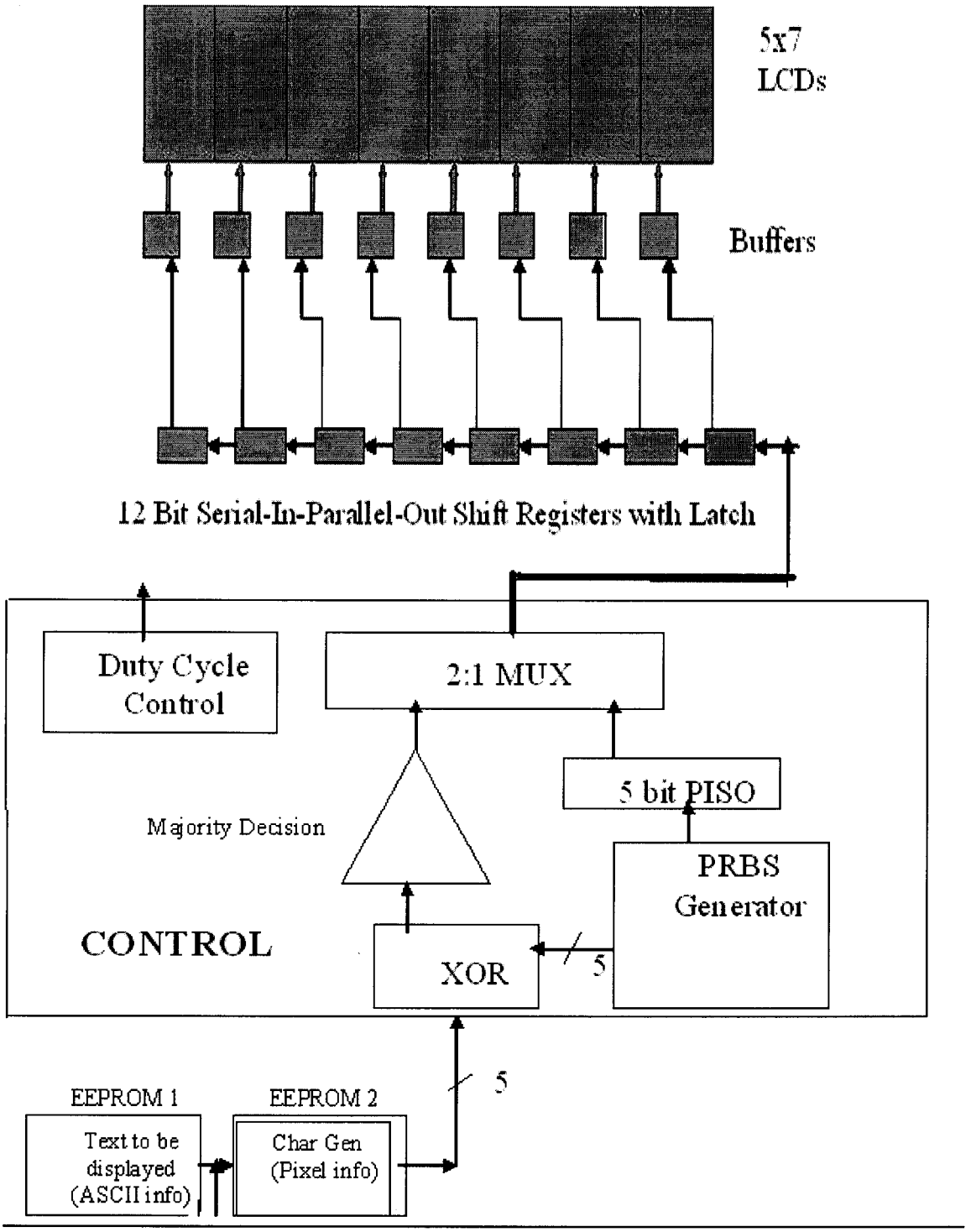


Figure 3.2. Block Diagram of Scrolling Alphanumeric LCD

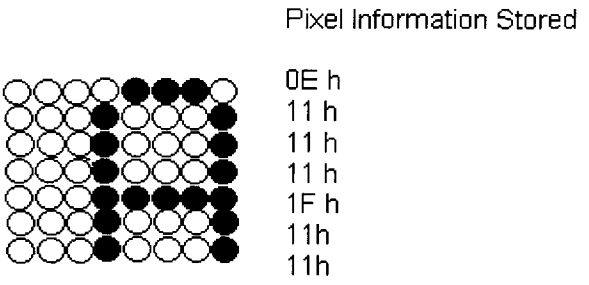


Figure 3.3 Pixel Information for 5 X 7 display

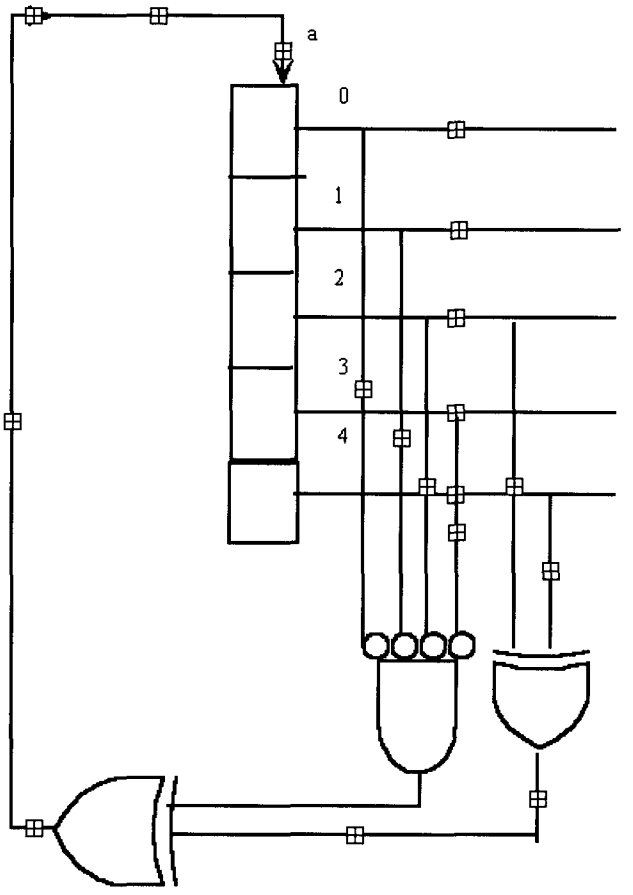


Figure 3.4 PRBS generator to generate maximum length sequence

This is because the PRBS and its delayed versions have identical wave shape and hence identical frequency components. There is however on difficulty in this viz., the PRBS sequence has only $(2^N - 1)$ state as the all zero state does not exist. A sequence generator for all the 2N states can be obtained by inserting the state with N zeros in the PRBS sequence. Such a sequence generator can be designed as shown in figure 3.4. for N=5.

4) Column Signal Generator(CSG)

The data pattern and the row-select pattern are compared bit-by-bit using the Exclusive- OR gates (XOR GATES) and a majority decision is made which is used to decide the column voltage. This method is in accordance with the working of BAT as explained in the preceding chapter. The majority decision block has been implemented using basic logic gates.

5) Five Bit Parallel-In-Serial-Out (PISO) Shift Register

A 5-Bit PISO Shift Register is used in the circuit to convert the parallel output of the PRBS generator to serial form so that it can be easily transmitted to the next blocks which require serial data input.

6) 2:1 Multiplexer

A 2:1 Multiplexer is utilized so that by controlling its select input, it is possible to differentiate between the column data and the row-select pattern being sent to the Drivers.

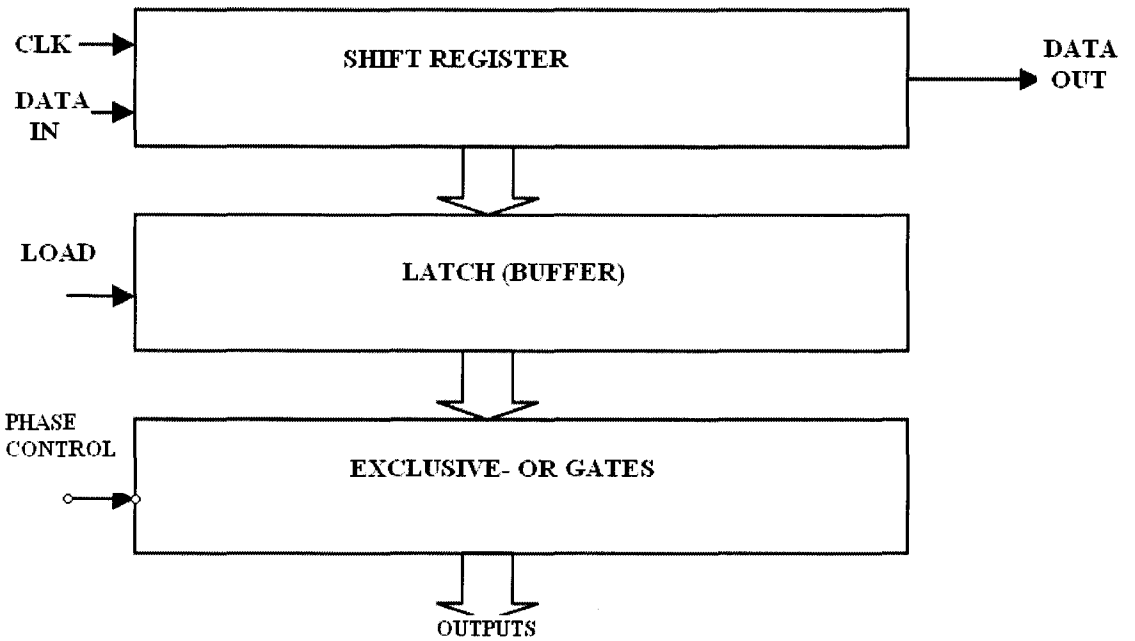


Figure 3.5. Typical Driver IC

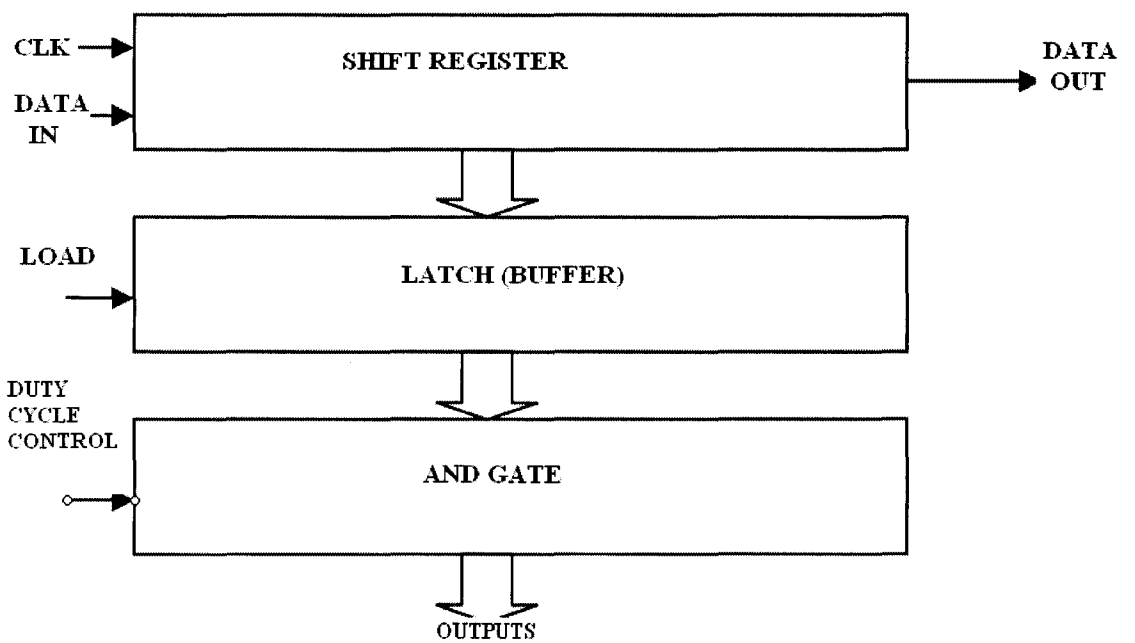


Figure 3.6. 12-Bit Driver designed using VHDL

7) Drivers

The Block Diagram of a generalized driver which is available in IC form is shown below in Figure 3.5.Such ICs are well suited to directly driven displays and also for BAT. The Exclusive- OR block provided in these ICs is to enable phase- reversal, in order to ensure dc-free operation (as discussed in the preceding chapter). However, since the BAT inherently provides a natural dc-free operation, the phase control input to the Exclusive-OR Block can be permanently tied to logic 0 or logic1.

Instead of dong all this we can do away with the regular driver ICs and design a shift-register and latch to accomplish the function of the driver. The length of the shift- register and latch required is equal to the number of row and column address lines respectively, in this case 12 bits (5 rows and 7 columns).

We have designed the drivers using VHDL, and have one 12 bit shift-register and latch (Implemented on EP910 EPLD), instead of two different shift- registers and latches for row and column drivers respectively. By this we have reduced the number of connections required in our circuit. Also, the output of the latch is subjected to the ANDing operation with the Duty Cycle Control waveform in this block itself, thus not requiring additional discrete components. The Block Diagram of the driver designed is as shown in figure 3.6.

8) Duty Cycle Control

This is a new concept and hence requires a detailed explanation. Consider the general form of a pulse wave form as shown in figure 3.7. The equation for V_{rms} for this pulse waveform is given by,

$$Vrms = \sqrt{\frac{1}{T}\left[\int_0^{\tau} V^2 dt\right]}$$ which upon solving

gives,

$$Vrms = V\sqrt{\frac{\tau}{T}}$$

From this equation it can be clearly seen that the V_{rms} can be varied by varying either the input voltage V or by varying the duty cycle of the waveform. However, varying the input voltage itself is not feasible as most circuits work on fixed voltage values such as 5V, 3.3V or 12V. Hence, to vary the value of V_{rms} from 0 to V, just the duty cycle of the input waveform needs to be varied. This variation should be such that the value of V when it is zero, remains at the same level and at other instants it is brought down to zero before the completion of its cycle. This is shown in Figure 3.8.

The OFF region of the waveform will then be known as the "Dead Time", signifying the region where the value of the instantaneous voltage is zero.

Now, we shall consider the situation of the voltage across an LCD pixel as shown in figure 3.8., being applied a row and a column voltage .In this case the instantaneous value of the voltage across the pixel is not a very important

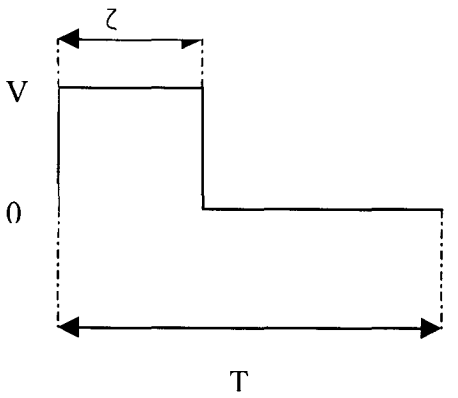


Figure 3.7. Pulse waveform

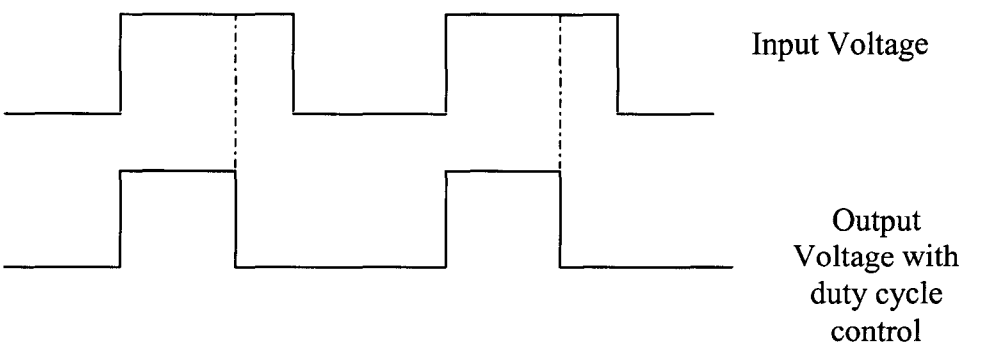


Figure 3.8. Voltage waveforms across an LCD pixel

parameter, while the rms value of the voltage plays a very important role. The situation demands that the voltage V_{OFFrms} of the pixel be equal to or less than V_{th}, the threshold voltage of the liquid used when the applied voltage is V. Thus, by making the duty cycle of the input waveform variable it is possible to vary the voltage V_{OFFrms} to any level between 0 – V . The voltage V itself can be any value either 5V, 3.3V or 12V, but because the rms voltage is being controlled by varying the duty cycle of the input voltage the voltage appearing across the OFF pixel will always be less than or equal to V_{th}, while that across the ON pixel will be greater than V_{th}.

3.3 Devices Used

The following devices have been utilized to implement the "Scrolling Alphanumeric LCD".

1) **EPROM 2732A**

   4K U-V erasable EPROM having 12 address lines and 8 output lines. It has two control functions Chip enable (CE) and Output enable (OE) both of which have to be logically active in order to obtain an output at the output lines.

2) **Clock Generator 4047(Monostable/ Astable Multivibrator)**

   The 4047 is connected in the astable mode of operation to provide for the master clock for the circuit.

3) **EP910 EPLD**

   This EPLD is used as the driver (Shift- register, latch and for the ANDing for the duty- cycle control). It is a 40 pin DIP package with 24 macro- cells. It belongs to the Altera Classic series.

4) **EPM7064LC44- 15**

   This device is utilized for the duty cycle control implementation block. It is a 44 pin device which has 64 macro- cells. It belongs to the Altera MAX 7000A series.

5) **EPM7128ELC84- 20**

   This device is used to implement the control logic block of the circuit. It is a 84 pin device which has 128 macro- cells. It belongs to the Altera MAX 7000E series.

6) **Buffers 4050**

   These are hex- non inverting buffers and are utilized to stabilze the voltage levels reaching the LCDs.

3.4 PCB Layout using OrCAD

The EP910 EPLDs which have been designed to perform the function of the driver for the LCDs have been mounted on PCBs, the design of which was done using OrCAD 386plus. For ease of in-house manufacture of the boards single layered boards (components are mounted on one side of the board and the circuit is etched on the other side) with "jumpers" were preferred to the double layered board. Both Schematic layout and PCB layout were made with the routing for the PCB layout being done using the "Manual Routing" option available in OrCAD. This was done because the "Auto Routing" option generally gives a two layered board output. The photo-plot of the driver board layout made is as shown in Figure 3.9.

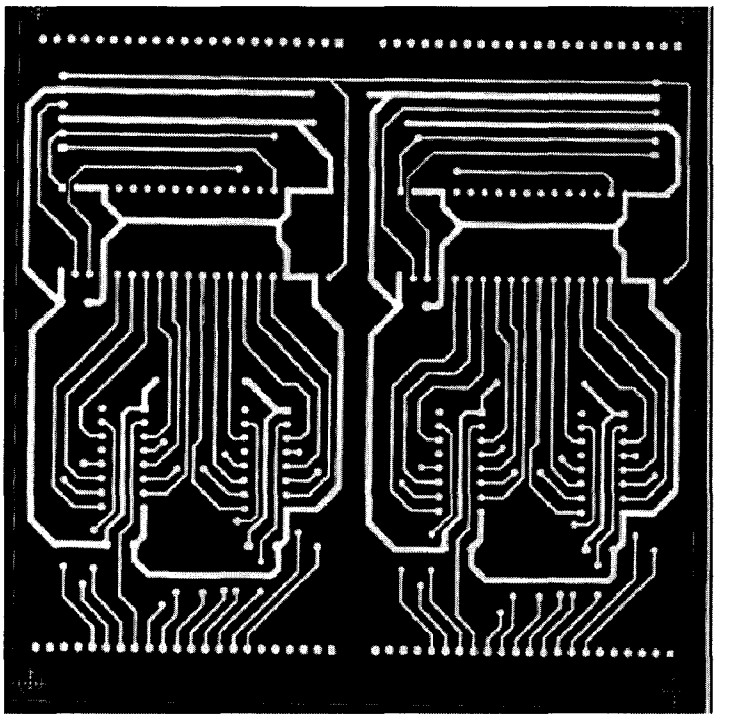


Figure 3.9. PCB Layout of driver board

CONCLUSION

Conclusion

In conclusion, it is seen that the Binary Addressing Technique(BAT) is well suited for Alphanumeric displays in which the value of number of lines to be simultaneously multiplexed N, is low and the supply voltage requirement to drive the display is also very low. This is evident from the Electro- optic response of the liquid used by us, RO- TN- 132 which is as shown in the figure. Referring to the data sheet of the liquid it is seen that the values obtained by us match the values provided.

The EPLDs are very versatile devices and the software MAX PLUS II is a real boon to engineers. The waveforms generated by MAX PLUS II 's Waveform Editor for our controller chip, EPM 7128 is as shown in the attached figure. The Waveform Editor gave us an actual outlook of the outputs that our project would provide when we were in the design stage itself. The outputs obtained tallied with those designed for and the "Scrolling Alphanumeric LCD" was implemented successfully.

Scope for Further Work

Further work that is possible is partly something left unfinished by us due to lack of time. The BAT Controller board made by us right now is on a General Purpose PCB, however we plan to make a PCB for the same. Also the Controller design along with the Duty Cycle Control block implemented using EP7128 and EP7064 respectively can be probably further optimized so that it can entirely fit onto the EP7128.

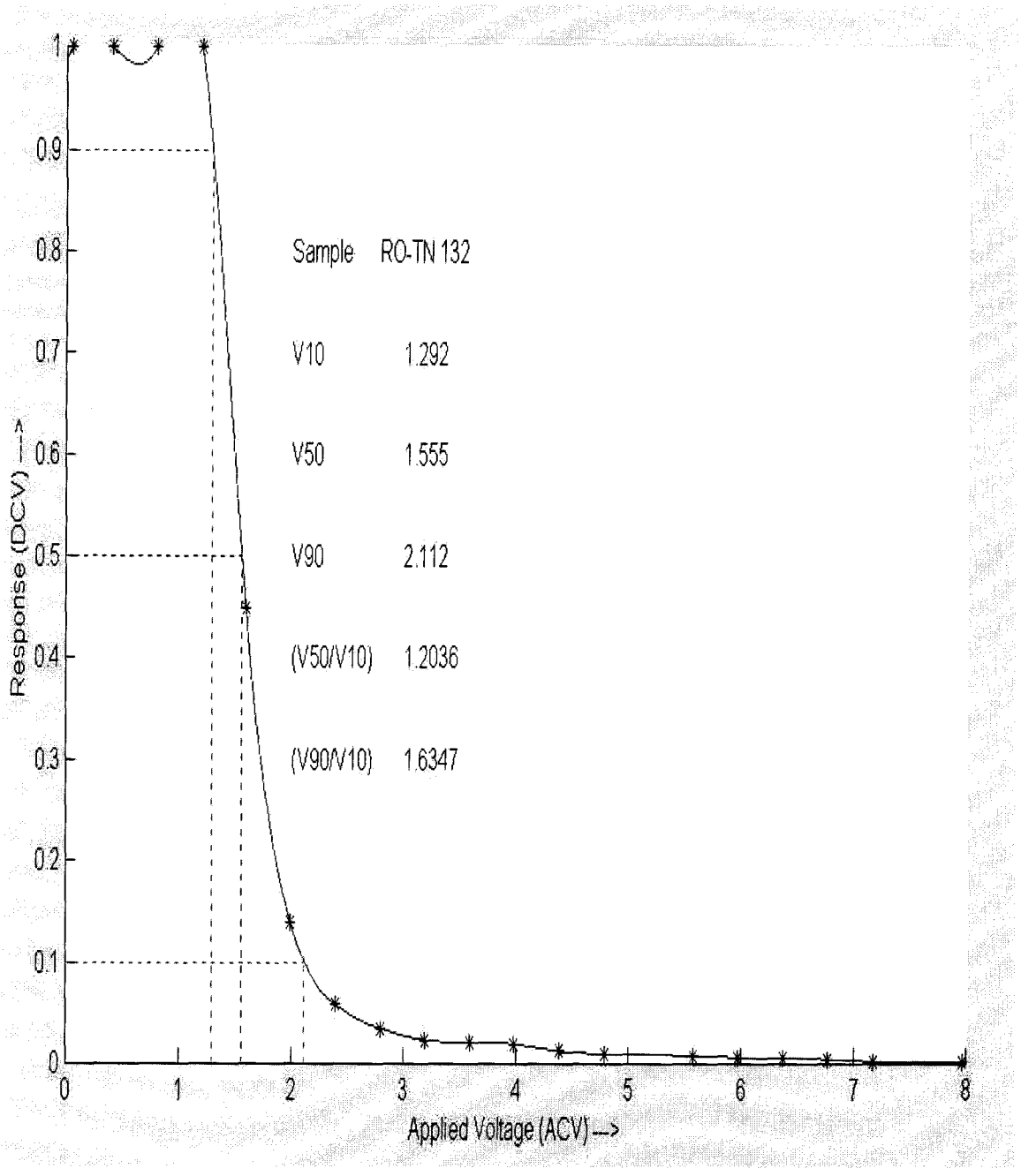
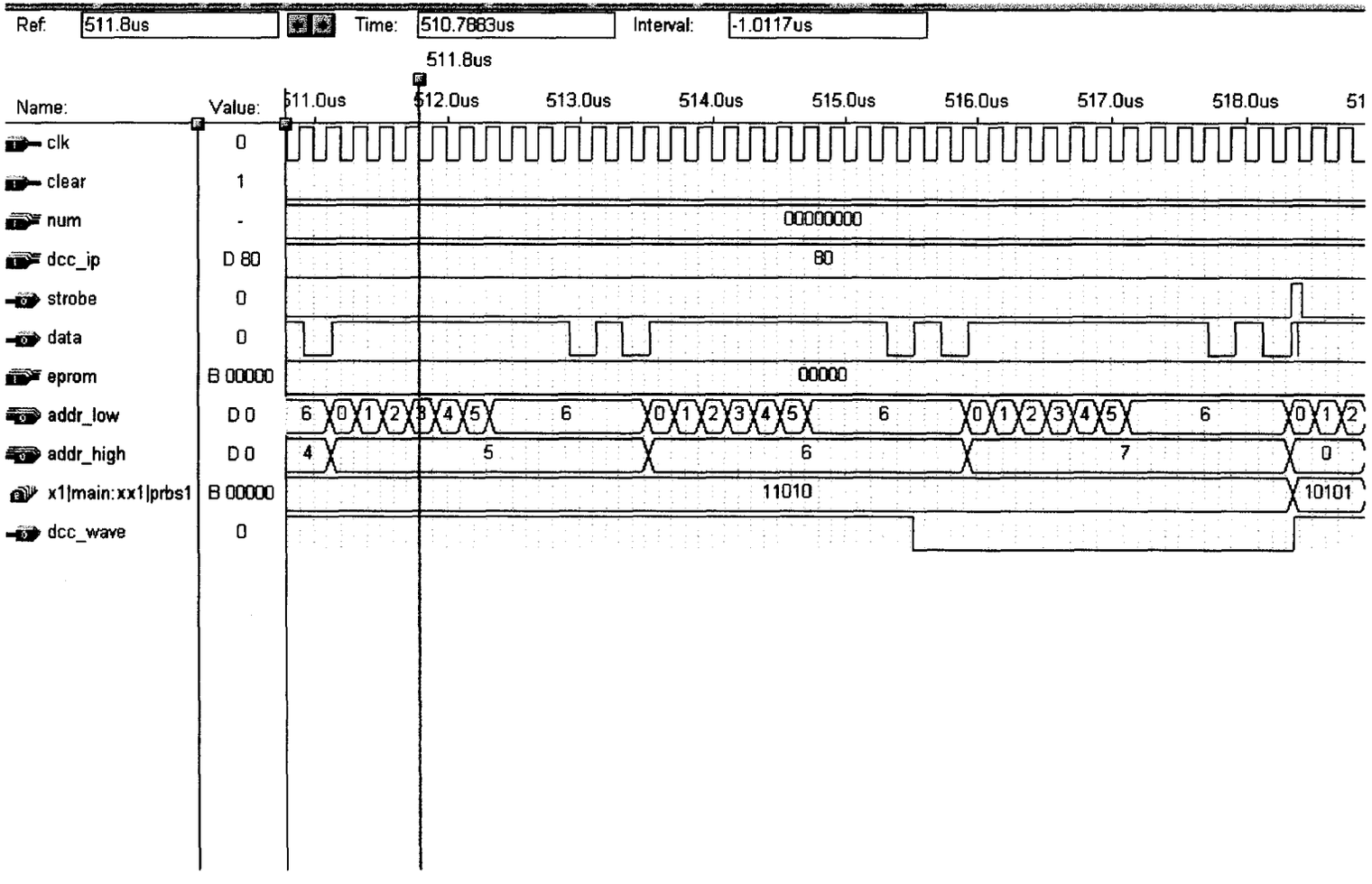


Figure Electro- optic Response of RO- TN- 132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Interval: -1.0117us
511.8us
Name:
Value:
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512.0us
513.0us
514.0us
515.0us
516.0us
517.0us
518.0us
clk
0
clear
1
num
-
00000000
dcc_ip
D 80
80
strobe
0
data
0
eprom
B 00000
00000
addr_low
D 0
addr_high
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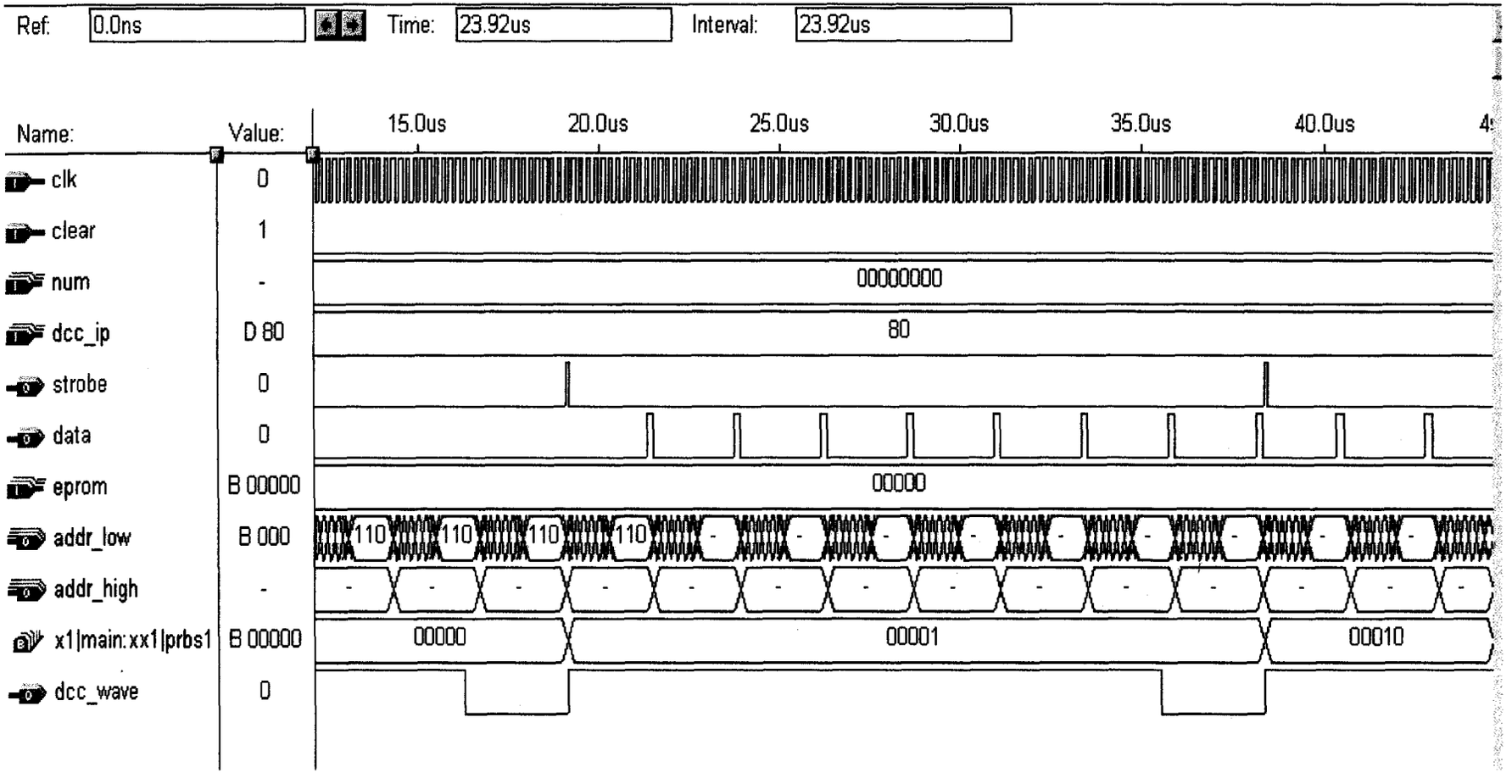
B 00000
11010
10101
dcc_wave
0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30.0us
35.0us
40.0us
clk
0
clear
1
num
-
00000000
dcc_ip
D 80
80
strobe
0
data
0
eprom
B 00000
00000
addr_low
B 000
110
addr_high
-
x1|main:xx1|prbs1
B 00000
00000
00001
00010
dcc_wave
0

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ANNEXURE A :
VHDL &
MAX PLUS II

Software Tool Used : MAX+PLUS® II

The MAX+PLUS® II development software provides a complete design environment that easily adapts to ones specific design needs. Regardless of whether we use a personal computer or a workstation, MAX+PLUS II ensures easy design entry, fast processing, and straightforward device programming.

MAX+PLUS II software is a fully integrated, architecture-independent package for designing logic with Altera programmable logic devices, including Classic™, ACEX 1K, MAX 3000, MAX® 5000, MAX 7000, MAX 9000, FLEX® 6000, FLEX 8000, and FLEX 10K devices. (MAX+PLUS II also allows one to program FLASHlogic™ and APEX devices.)

MAX+PLUS II offers a full spectrum of logic design capabilities: three design entry methods for hierarchical designs; floorplan editing; powerful logic synthesis; design partitioning; functional, timing, and board-level-type linked simulation; detailed timing analysis; automatic error location; and device programming and verification. MAX+PLUS II also reads standard EDIF netlist files, VHDL netlist files, Verilog HDL netlist files, and OrCAD Schematic Files, and writes EDIF, VHDL, and Verilog HDL netlist files, including VITAL-compliant files, for a convenient interface to other industry-standard CAE software.

One can integrate existing designs created with Altera's A+PLUS™, SAM+PLUS™, and MAX+PLUS (DOS) software packages into MAX+PLUS II designs. In addition, MAX+PLUS II for UNIX workstations allows one to run the Synopsys Design Compiler and FPGA Compiler automatically, which allow us to process both VHDL and Verilog HDL designs. The MAX+PLUS II Compiler ensures that a design--called a project in MAX+PLUS II--fits into the device architecture in the most efficient way possible.

MAX+PLUS II Highlights

MAX+PLUS II offers a rich graphical user interface complemented with an illustrated, easy-to-use on-line help system. The complete MAX+PLUS II system includes ten fully integrated applications that take one through every step from design entry to device programming.

Many features and commands are shared by the different MAX+PLUS II applications, so that learning to use one application gives us a head

We can specify resource and device assignments for a VHDL Design File to guide logic synthesis and fitting for our project. We can choose to have the Compiler automatically fit our project into the best combination of devices from a target device family and assign the resources within them. We can also enter specific assignments with the Assign menu commands, the Floorplan Editor, or in the Assignment & Configuration File for our project.

Device Details

For Details of devices used and their architecture please refer to the relevant datasheets attached.

Very High Speed Integrated Circuit (VHSIC) Hardware Description Language (VHDL)

The Very High Speed Integrated Circuit (VHSIC) Hardware Description Language (VHDL) is a high-level, modular language that is completely integrated into the MAX+PLUS II system. One can use the MAX+PLUS II Text Editor or another text editor to create VHDL Design Files (with the .vhd extension) using either VHDL 1987 or VHDL 1993 syntax. We can then compile and simulate the VHDL Design Files and use them to program Altera devices.

VHDL Design Files can contain any combination of MAX+PLUS II-supported constructs. They can also contain Altera-provided logic functions, including primitives, megafunctions, and macrofunctions, and user-defined logic functions.

How Does MAX+PLUS II VHDL Support Work?

VHDL constructs are powerful and versatile. One can create entire hierarchical projects with VHDL, or mix VHDL Design Files with other types of design files in a hierarchical project.

Although we can use any ASCII text editor to create VHDL designs, the MAX+PLUS II Text Editor allows one to take advantage of features available only in MAX+PLUS II while we enter, compile, and debug a VHDL design, including VHDL templates, syntax coloring, error location, and resource and device assignments.

VHDL designs are easily incorporated into a design hierarchy. In the Text Editor, we can automatically create a symbol that represents a VHDL Design File and incorporate it into a GDF. Similarly, we can incorporate custom functions, as well as Altera-provided macrofunctions, megafunctions, and primitives, into any VHDL Design File.

The MAX+PLUS II Compiler allows us to check VHDL syntax quickly or perform a full compilation to debug and process your project. We can use the MAX+PLUS II Message Processor to locate errors automatically and highlight them in the Text Editor window. After the project has compiled successfully, we can perform optional simulation and timing analysis with MAX+PLUS II, and then program one or more Altera devices. We can also create VHDL Output Files or Standard Delay Format (SDF) Output Files for use with third-party simulation tools.

start on learning to use the others. For example, we use identical commands in each MAX+PLUS II application to open files, to assign project devices, and to begin compiling the current project. The design editors in MAX+PLUS II--the Graphic, Text, and Waveform Editors--and the auxiliary editors--the Floorplan and Symbol Editors--also share numerous design entry tools and features. Each editor allows one to perform similar tasks, such as assigning a pin, in the same way.

One can easily combine different types of design files in a hierarchical project, choosing the design entry format that works best for each functional block. Over 300 primitives, megafunctions, and macrofunctions, AHDL™, and the built-in EDIF, VHDL, Verilog HDL, and OrCAD interfaces simplify design entry. Architecture-independent design entry gives us the freedom to create logic without worrying about the final device implementation.

One can work with different MAX+PLUS II applications at the same time. For example, we can open multiple design files and transfer information between them, while simultaneously compiling or simulating another project. We can view an entire hierarchy of design files and move smoothly from one hierarchical level to another. As we open a design file, MAX+PLUS II automatically starts the appropriate design editor.

The MAX+PLUS II Compiler lies at the heart of the MAX+PLUS II system, providing powerful design processing that one can customize to achieve the best possible silicon implementation of your project. Automatic error location and extensive documentation on error and warning messages make design modifications as simple as possible. One can create output files in a variety of formats for simulation, timing analysis, and device programming, including EDIF, Verilog HDL, and VHDL files for use with other industry-standard EDA tools. At every step in the design process, MAX+PLUS II software makes it easy for us to focus on your design--not on how to use the software.

The superb integration of MAX+PLUS II software improves our efficiency and productivity, putting us in control of our logic design environment.

All in all, it is probably one of the best available tools available today.

ASCII CHARACTER SET (5 x 7 MATRIX FONT)

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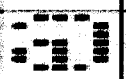
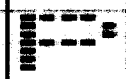
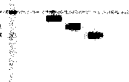
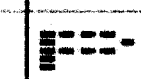
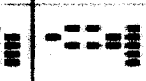
0	CG RAM (1)							
1	CG RAM (2)							
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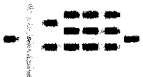
3	CG RAM (4)							
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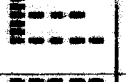
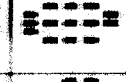
5	CG RAM (6)							
6	CG RAM (7)							
7	CG RAM (8)							
8	CG RAM (1)							
9	CG RAM (2)							
A	CG RAM (3)							
B	CG RAM (4)							
C	CG RAM (5)							
D	CG RAM (6)							
E	CG RAM (7)							
F	CG RAM (8)							

MAX 7000

Programmable Logic Device Family

November 2001, ver. 6.3 | Data Sheet

Features...

- High-performance, EEPROM-based programmable logic devices (PLDs) based on second-generation MAX® architecture
- 5.0-V in-system programmability (ISP) through the built-in IEEE Std. 1149.1 Joint Test Action Group (JTAG) interface available in MAX 7000S devices
  - ISP circuitry compatible with IEEE Std. 1532
- Includes 5.0-V MAX 7000 devices and 5.0-V ISP-based MAX 7000S devices
- Built-in JTAG boundary-scan test (BST) circuitry in MAX 7000S devices with 128 or more macrocells
- Complete EPLD family with logic densities ranging from 600 to 5,000 usable gates (see Tables 1 and 2)
- 5-ns pin-to-pin logic delays with up to 175.4-MHz counter frequencies (including interconnect)
- PCI-compliant devices available

For information on in-system programmable 3.3-V MAX 7000A or 2.5-V MAX 7000B devices, see the *MAX 7000A Programmable Logic Device Family Data Sheet* or the *MAX 7000B Programmable Logic Device Family Data Sheet*.

Table 1. MAX 7000 Device Features

Feature	EPM7032	EPM7064	EPM7096	EPM7128E	EPM7160E	EPM7192E	EPM7256E
Usable gates	600	1,250	1,800	2,500	3,200	3,750	5,000
Macrocells	32	64	96	128	160	192	256
Logic array blocks	2	4	6	8	10	12	16
Maximum user I/O pins	36	68	76	100	104	124	164
t_{PD} (ns)	6	6	7.5	7.5	10	12	12
t_{SU} (ns)	5	5	6	6	7	7	7
t_{FSU} (ns)	2.5	2.5	3	3	3	3	3
t_{CO1} (ns)	4	4	4.5	4.5	5	6	6
f_{CNT} (MHz)	151.5	151.5	125.0	125.0	100.0	90.9	90.9

Table 2. MAX 7000S Device Features

Feature	EPM7032S	EPM7064S	EPM7128S	EPM7160S	EPM7192S	EPM7256S
Usable gates	600	1,250	2,500	3,200	3,750	5,000
Macrocells	32	64	128	160	192	256
Logic array blocks	2	4	8	10	12	16
Maximum user I/O pins	36	68	100	104	124	164
t_{PD} (ns)	5	5	6	6	7.5	7.5
t_{SU} (ns)	2.9	2.9	3.4	3.4	4.1	3.9
t_{FSU} (ns)	2.5	2.5	2.5	2.5	3	3
t_{CO1} (ns)	3.2	3.2	4	3.9	4.7	4.7
f_{CNT} (MHz)	175.4	175.4	147.1	149.3	125.0	128.2

...and More Features

- Open-drain output option in MAX 7000S devices
- Programmable macrocell flipflops with individual clear, preset, clock, and clock enable controls
- Programmable power-saving mode for a reduction of over 50% in each macrocell
- Configurable expander product-term distribution, allowing up to 32 product terms per macrocell
- 44 to 208 pins available in plastic J-lead chip carrier (PLCC), ceramic pin-grid array (PGA), plastic quad flat pack (PQFP), power quad flat pack (RQFP), and 1.0-mm thin quad flat pack (TQFP) packages
- Programmable security bit for protection of proprietary designs
- 3.3-V or 5.0-V operation
  - MultiVolt™ I/O interface operation, allowing devices to interface with 3.3-V or 5.0-V devices (MultiVolt I/O operation is not available in 44-pin packages)
  - Pin compatible with low-voltage MAX 7000A and MAX 7000B devices
- Enhanced features available in MAX 7000E and MAX 7000S devices
  - Six pin- or logic-driven output enable signals
  - Two global clock signals with optional inversion
  - Enhanced interconnect resources for improved routability
  - Fast input setup times provided by a dedicated path from I/O pin to macrocell registers
  - Programmable output slew-rate control
- Software design support and automatic place-and-route provided by Altera's development system for Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800 workstations

- Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, and VeriBest
- Programming support
  - Altera's Master Programming Unit (MPU) and programming hardware from third-party manufacturers program all MAX 7000 devices
  - The BitBlaster™ serial download cable, ByteBlasterMV™ parallel port download cable, and MasterBlaster™ serial/universal serial bus (USB) download cable program MAX 7000S devices

General Description

The MAX 7000 family of high-density, high-performance PLDs is based on Altera's second-generation MAX architecture. Fabricated with advanced CMOS technology, the EEPROM-based MAX 7000 family provides 600 to 5,000 usable gates, ISP, pin-to-pin delays as fast as 5 ns, and counter speeds of up to 175.4 MHz. MAX 7000S devices in the -5, -6, -7, and -10 speed grades as well as MAX 7000 and MAX 7000E devices in -5, -6, -7, -10P, and -12P speed grades comply with the PCI Special Interest Group (PCI SIG) ***PCI Local Bus Specification, Revision 2.2***. See Table 3 for available speed grades.

Table 3. MAX 7000 Speed Grades

Device	Speed Grade									
	-5	-6	-7	-10P	-10	-12P	-12	-15	-15T	-20
EPM7032		✓	✓		✓		✓	✓	✓	
EPM7032S	✓	✓	✓		✓					
EPM7064		✓	✓		✓		✓	✓		
EPM7064S	✓	✓	✓		✓					
EPM7096			✓		✓		✓	✓		
EPM7128E			✓	✓	✓		✓	✓		✓
EPM7128S		✓	✓		✓			✓		
EPM7160E				✓	✓		✓	✓		✓
EPM7160S		✓	✓		✓			✓		
EPM7192E						✓	✓	✓		✓
EPM7192S			✓		✓			✓		
EPM7256E						✓	✓	✓		✓
EPM7256S			✓		✓			✓		

The MAX 7000E devices—including the EPM7128E, EPM7160E, EPM7192E, and EPM7256E devices—have several enhanced features: additional global clocking, additional output enable controls, enhanced interconnect resources, fast input registers, and a programmable slew rate.

In-system programmable MAX 7000 devices—called MAX 7000S devices—include the EPM7032S, EPM7064S, EPM7128S, EPM7160S, EPM7192S, and EPM7256S devices. MAX 7000S devices have the enhanced features of MAX 7000E devices as well as JTAG BST circuitry in devices with 128 or more macrocells, ISP, and an open-drain output option. See Table 4.

Table 4. MAX 7000 Device Features

Feature	EPM7032 EPM7064 EPM7096	All MAX 7000E Devices	All MAX 7000S Devices
ISP via JTAG interface			✓
JTAG BST circuitry			✓ *(1)*
Open-drain output option			✓
Fast input registers		✓	✓
Six global output enables		✓	✓
Two global clocks		✓	✓
Slew-rate control		✓	✓
MultiVolt interface *(2)*	✓	✓	✓
Programmable register	✓	✓	✓
Parallel expanders	✓	✓	✓
Shared expanders	✓	✓	✓
Power-saving mode	✓	✓	✓
Security bit	✓	✓	✓
PCI-compliant devices available	✓	✓	✓

Notes:
(1) Available only in EPM7128S, EPM7160S, EPM7192S, and EPM7256S devices only.
(2) The MultiVolt I/O interface is not available in 44-pin packages.

The MAX 7000 architecture supports 100% TTL emulation and high-density integration of SSI, MSI, and LSI logic functions. The MAX 7000 architecture easily integrates multiple devices ranging from PALs, GALs, and 22V10s to MACH and pLSI devices. MAX 7000 devices are available in a wide range of packages, including PLCC, PGA, PQFP, RQFP, and TQFP packages. See Table 5.

Table 5. MAX 7000 Maximum User I/O Pins *Note (1)*

Device	44-Pin PLCC	44-Pin PQFP	44-Pin TQFP	68-Pin PLCC	84-Pin PLCC	100-Pin PQFP	100-Pin TQFP	160-Pin PQFP	160-Pin PGA	192-Pin PGA	208-Pin PQFP	208-Pin RQFP
EPM7032	36	36	36									
EPM7032S	36		36									
EPM7064	36		36	52	68	68						
EPM7064S	36		36		68		68					
EPM7096				52	64	76						
EPM7128E					68	84		100				
EPM7128S					68	84	84 *(2)*	100				
EPM7160E					64	84		104				
EPM7160S					64		84 *(2)*	104				
EPM7192E								124	124			
EPM7192S								124				
EPM7256E								132 *(2)*		164		164
EPM7256S											164 *(2)*	164

Notes:

(1) When the JTAG interface in MAX 7000S devices is used for either boundary-scan testing or for ISP, four I/O pins become JTAG pins.

(2) Perform a complete thermal analysis before committing a design to this device package. For more information, see the *Operating Requirements for Altera Devices Data Sheet*.

MAX 7000 devices use CMOS EEPROM cells to implement logic functions. The user-configurable MAX 7000 architecture accommodates a variety of independent combinatorial and sequential logic functions. The devices can be reprogrammed for quick and efficient iterations during design development and debug cycles, and can be programmed and erased up to 100 times.

Table 12. MAX 7000 5.0-V Device DC Operating Conditions *Note (8)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage		2.0	V_{CCINT} + 0.5	V
V_{IL}	Low-level input voltage		–0.5 *(7)*	0.8	V
V_{OH}	5.0-V high-level TTL output voltage	I_{OH} = –4 mA DC, V_{CCIO} = 4.75 V *(9)*	2.4		V
	3.3-V high-level TTL output voltage	I_{OH} = –4 mA DC, V_{CCIO} = 3.00 V *(9)*	2.4		V
	3.3-V high-level CMOS output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 3.0 V *(9)*	V_{CCIO} – 0.2		V
V_{OL}	5.0-V low-level TTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 4.75 V *(10)*		0.45	V
	3.3-V low-level TTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 3.00 V *(10)*		0.45	V
	3.3-V low-level CMOS output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 3.0 V *(10)*		0.2	V
I_I	Leakage current of dedicated input pins	V_I = –0.5 to 5.5 V *(10)*	–10	10	µA
I_{OZ}	I/O pin tri-state output off-state current	V_I = –0.5 to 5.5 V *(10)*, *(11)*	–40	40	µA

Table 13. MAX 7000 5.0-V Device Capacitance: EPM7032, EPM7064 & EPM7096 Devices *Note (12)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		12	pF
$C_{I/O}$	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF

Table 14. MAX 7000 5.0-V Device Capacitance: MAX 7000E Devices *Note (12)*

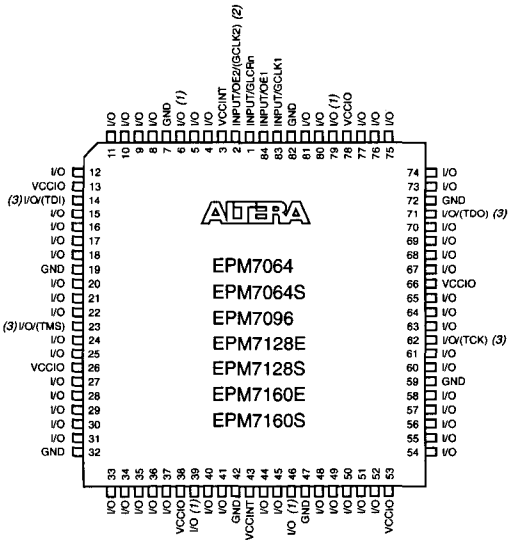
Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		15	pF
$C_{I/O}$	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		15	pF

Table 15. MAX 7000 5.0-V Device Capacitance: MAX 7000S Devices *Note (12)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Dedicated input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
$C_{I/O}$	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10	pF

Figure 18. 84-Pin Package Pin-Out Diagram

Package outline not drawn to scale.



84-Pin PLCC

Notes:
(1) Pins 6, 39, 46, and 79 are no-connect (N.C.) pins on EPM7096, EPM7160E, and EPM7160S devices.
(2) The pin functions shown in parenthesis are only available in MAX 7000E and MAX 7000S devices.
(3) JTAG ports are available in MAX 7000S devices only.

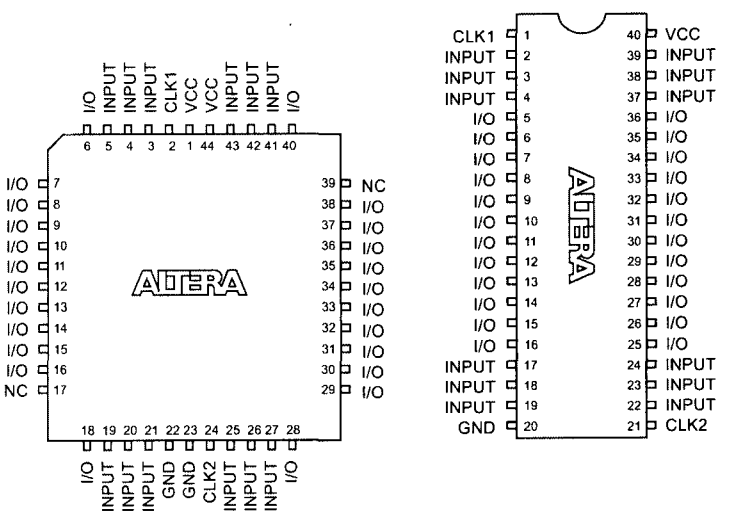
EP910 EPLD

Features

- High-performance, 24-macrocell Classic EPLD
  - Combinatorial speeds with t_{PD} as fast as 12 ns
  - Counter frequencies of up to 76.9 MHz
  - Pipelined data rates of up to 125 MHz
- Programmable I/O architecture with up to 36 inputs or 24 outputs
- EP910 and EP910I devices are pin-, function-, and programming file-compatible
- Programmable clock option for independent clocking of all registers
- Macrocells individually programmable as D, T, JK, or SR flipflops, or for combinatorial operation
- Available in the following packages (see Figure 11)
  - 44-pin plastic J-lead chip carrier (PLCC)
  - 40-pin ceramic and plastic dual in-line packages (CerDIP and PDIP)

Figure 11. EP910 Package Pin-Out Diagrams

Package outlines are not drawn to scale. Windows in ceramic packages only.



44-Pin PLCC

EP910
EP910I

40-Pin DIP

EP910
EP910I

Figure 13 shows the typical supply current (I_{CC}) versus frequency of EP910 devices.

Figure 13. I_{CC} vs. Frequency of EP910 Devices

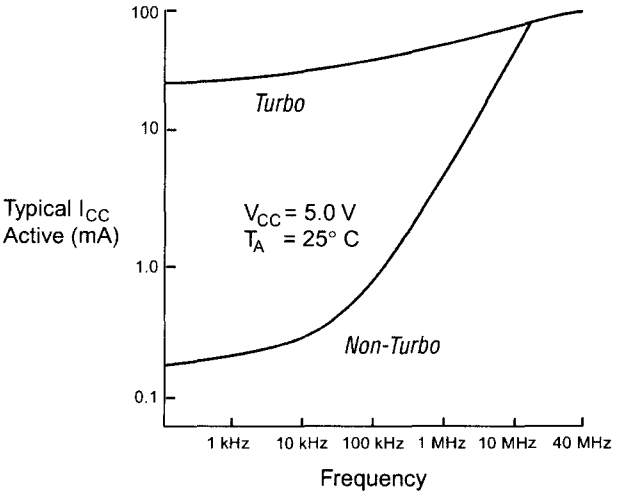
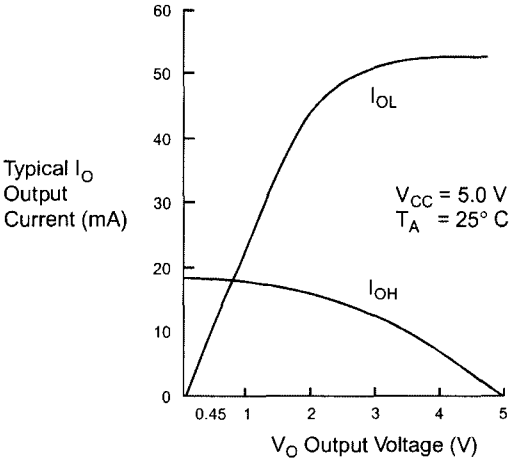


Figure 14 shows the typical output drive characteristics of EP910 devices.

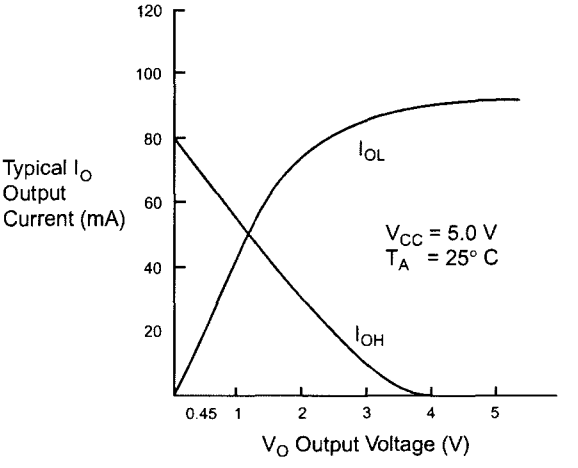
Figure 14. Output Drive Characteristics of EP910 Devices

Drive characteristics may exceed shown curves.

EP910 EPLDs



EP910I EPLDs



Operating Conditions

Tables 14 through 18 provide information on absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for EP910 and EP910I devices.

Table 14. EP910 & EP910I Device Absolute Maximum Ratings *Notes (1), (2)*

Symbol	Parameter	Conditions	EP910		EP910I		Unit
			Min	Max	Min	Max	
V_{CC}	Supply voltage	With respect to ground *(3)*	–2.0	7.0	–2.0	7.0	V
V_I	DC input voltage		–2.0	7.0	–0.5	V_{CC} + 0.5	V
I_{MAX}	DC V_{CC} or ground current		–250	250			mA
I_{OUT}	DC output current, per pin		–25	25			mA
T_{STG}	Storage temperature	No bias	–65	150	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	–65	135	° C
T_J	Junction temperature	Ceramic packages, under bias		150		150	° C
		Plastic packages, under bias		135		135	° C

Table 15. EP910 & EP910I Device Recommended Operating Conditions *Note (2)*

Symbol	Parameter	Conditions	EP910		EP910I		Unit
			Min	Max	Min	Max	
V_{CC}	Supply voltage	*(4)*	4.75 (4.5)	5.25 (5.5)	4.75	5.25	V
V_I	Input voltage		–0.3	V_{CC} + 0.3	–0.3	V_{CC} + 0.3	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	0	70	° C
		For industrial use	–40	85			° C
t_R	Input rise time	*(5)*		100 (50)		500	ns
t_F	Input fall time	*(5)*		100 (50)		500	ns

Table 16. EP910 & EP910I Device DC Operating Conditions *Notes (6), (7)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage		2.0	V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC *(8)*	2.4		V
	High-level CMOS output voltage	I_{OH} = –0.6 mA DC *(8), (9)*	3.84		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC *(8)*		0.45	V
I_I	I/O leakage current of dedicated input pins	V_I = V_{CC} or ground	–10	10	µA
I_{OZ}	Tri-state output leakage current	V_O = V_{CC} or ground	–10	10	µA

Table 17. EP910 & EP910I Device Capacitance *Note (6)*

Symbol	Parameter	Conditions	EP910		EP910I		Unit
			Min	Max	Min	Max	
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		20		8	pF
$C_{I/O}$	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20		8	pF
C_{CLK1}	CLK1 pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		20		10	pF
C_{CLK2}	CLK2 pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		60		12	pF

Table 18. EP910 & EP910I Device I_{CC} Supply Current *Notes (2), (6), (7)*

Symbol	Parameter	Conditions	EP910			EP910I			Unit
			Min	Typ	Max	Min	Typ	Max	
I_{CC1}	V_{CC} supply current (non-Turbo, standby)	V_I = V_{CC} or ground, no load *(10), (11)*		20	150		60	150	µA
I_{CC2}	V_{CC} supply current (non-Turbo, active)	V_I = V_{CC} or ground, no load, f = 1.0 MHz *(10), (11)*		6	20		4	12	mA
I_{CC3}	V_{CC} supply current (Turbo, active)	V_I = V_{CC} or ground, no load, f = 1.0 MHz *(11)*		45	80 (100)		120	150	mA

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet* in this data book.
(2) Numbers in parentheses are for industrial-temperature-range devices.
(3) The minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V (EP910) or –0.5 V (EP910I) or overshoot to 7.0 V (EP910) or V_{CC} + 0.5 V (EP910I) for input currents less than 100 mA and periods less than 20 ns.
(4) Maximum V_{CC} rise time for EP910 devices = 50 ms; for EP910I devices, maximum V_{CC} rise time is unlimited with monotonic rise.
(5) For all clocks: t_R and t_F = 100 ns (50 ns for the industrial-temperature-range version).
(6) These values are specified in Table 15 on page 770.
(7) The device capacitance is measured at 25° C and is sample-tested only.
(8) The I_{OH} parameter refers to high-level TTL or CMOS output current; the I_{OL} parameter refers to low-level TTL output current.
(9) This parameter does not apply to EP910I devices.
(10) When the Turbo Bit option is not set (non-Turbo mode), an EP910 device will enter standby mode if no logic transitions occur for 100 ns after the last transition, and an EP910I device will enter standby mode if no logic transitions occur for 75 ns after the last transition.
(11) Measured with a device programmed as a 24-bit counter.

M2732A
32K (4K x 8) UV ERASABLE PROM

Military

- **250 ns (M2732A-25) Maximum Access Time ... HMOS* -E Technology**
- **Compatible to High Speed 5 MHz MIAPX 86/10 MPU ... Zero Wait State**
- **Military Temperature Range: −55°C to +125°C (T_C)**
- **Industry Standard Pinout ... JEDEC Approved**
- **Two Line Control**
- **Low Standby Current ... 35 mA Max.**

The Intel M2732A is a 5V only, 32,768 bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The standard M2732A's access time is 450 ns with speed selection (M2732A-25) available at 250 ns. The access time is compatible to high performance microprocessors, such as the 5 MHz MiAPX 86/10. In these systems, the M2732A allows the microprocessor to operate without the addition of WAIT states.

An important M2732A feature is the separate output control, Output Enable ($\overline{OE}$), from the Chip Enable control ($\overline{CE}$). The $\overline{OE}$ control eliminates bus contention in multiple bus microprocessor systems. Intel's Application Note AP-72 describes the microprocessor system implementation of the $\overline{OE}$ and $\overline{CE}$ controls on Intel's EPROMs. AP-72 is available from Intel's Literature Department.

The M2732A has a standby mode which reduces the power dissipation without increasing access time. The maximum active current is 115 mA, while the maximum standby current is only 35 mA, a 66% saving. The standby mode is achieved by applying a TTL-high signal to the $\overline{CE}$ input.

The M2732A is fabricated with HMOS-E technology, Intel's high speed N-channel MOS Silicon Gate Technology.

*HMOS is a patented process of Intel Corporation.

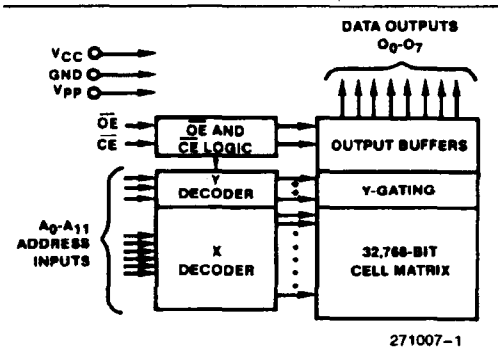


Figure 1. Block Diagram

Mode Selection

Mode \ Pins	CE (18)	OE/V_{PP} (20)	V_{CC} (24)	Outputs (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	High Z
Program	V_{IL}	V_{PP}	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+5	D_{OUT}
Program Inhibit	V_{IH}	V_{PP}	+5	High Z

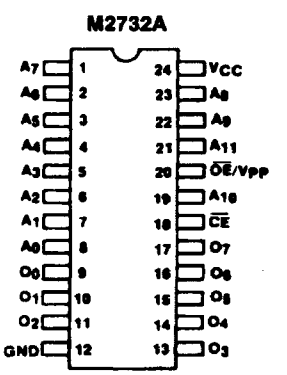


Figure 2. Configuration

Pin Names

A_0-A_{11}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0-O_7	Outputs

October 1986
Order Number: 271007-001

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . −55°C to +135°C
Storage Temperature . . . . . −65°C to +150°C
All Input or Output Voltages with Respect to Ground . . . . . +6V to −0.3V
V_{PP} Supply Voltage with Respect to Ground During Programming . . . . +22V to −0.3V

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. AND A.C. OPERATING CONDITIONS DURING READ

	M2732A-25	M2732A-45
Operating Temperature Range (T_C)	−55°C to +125°C	−55°C to +125°C
V_{CC} Power Supply	5V ±10%	5V ±10%

READ OPERATION

D.C. CHARACTERISTICS

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ(1)	Max		
I_{IL}	Input Load Current			10	μA	V_{IN} = 5.5V
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 5.5V
I_{CC1}	V_{CC} Current (Standby)			35	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}
I_{CC2}	V_{CC} Current (Active)			115	mA	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
V_{IL}	Input Low Voltage	−0.1		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC} + 1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} ±400 μA

NOTE:
1. Typical values are for T_C = 25°C and nominal supply voltages.

7

A.C. CHARACTERISTICS

Symbol	Parameter	M2732A-25			M2732A-45			Unit	Test Conditions
		Min	Typ(1)	Max	Min	Typ(1)	Max		
t_{ACC}	Address to Output Delay			250			450	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
t_{CE}	$\overline{CE}$ to Output Delay			250			450	ns	$\overline{OE}$ = V_{IL}
t_{OE}	Output Enable to Output Delay	10		100	10		150	ns	$\overline{CE}$ = V_{IL}
t_{DF}(2)	Output Enable High to Output Float	0		90	0		130	ns	$\overline{CE}$ = V_{IL}
t_{OH}(2)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	0			0			ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

CAPACITANCE (1), (2)

T_C(5) = 25°C, f = 1 MHz

Symbol	Parameter	Typ	Max	Unit	Conditions
C_{IN}	Input Capacitance Except $\overline{OE}/V_{PP}$	4	6	pF	V_{IN} = 0V
C_{IN}	$\overline{OE}/V_{PP}$ Input Capacitance		20	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance		12	pF	V_{OUT} = 0V

A.C. TEST CONDITIONS

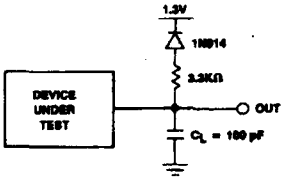
Output Load ..... 1 TTL gate, 100Ω
Resistor and C_L = 100 pF
Input Rise and Fall Times ..... ≤20 ns
Input Pulse Levels ..... 0.45V to 2.4V
Timing Measurement Reference Level
Inputs ..... 0.8V and 2V
Outputs ..... 0.8V and 2V

A.C. TESTING, OUTPUT WAVEFORM

271007-5

A.C. Testing: Inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing Measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

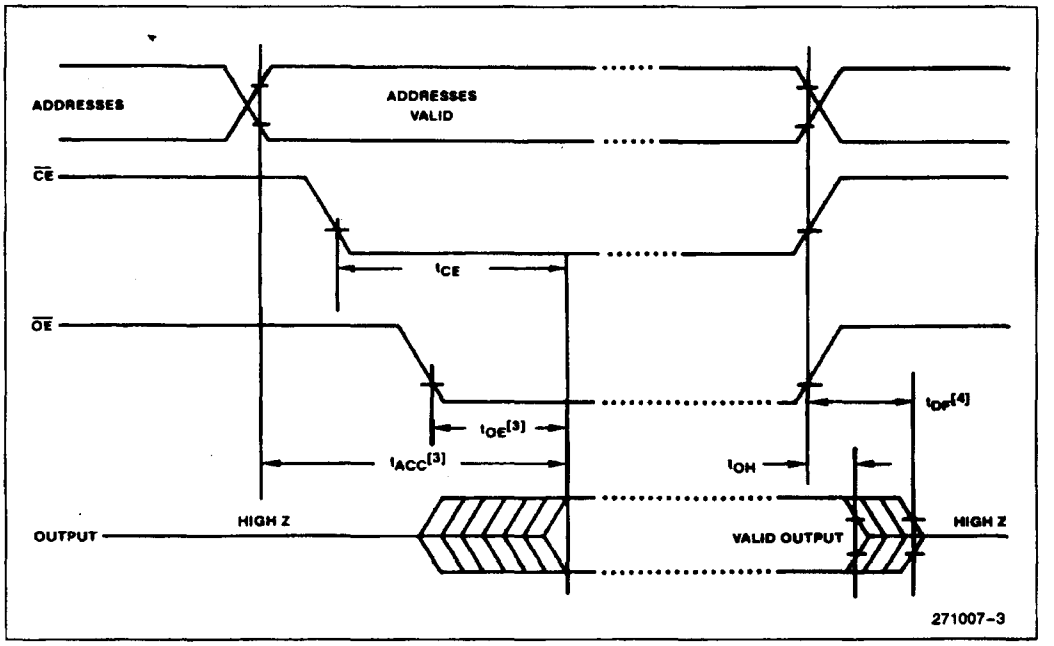
A.C. TESTING LOAD CIRCUIT



C_L = 100 pF
C_L includes Jig Capacitance

271007-6

A.C. WAVEFORMS



271007-3

NOTES:
1. Typical values are for T_C = 25°C and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven.
5. Case temperatures are "instant on".

DEVICE OPERATION

The five modes of operation of the M2732A are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{OE}/V_{PP}$ during programming. In the program mode the $\overline{OE}/V_{PP}$ input is pulsed from a TTL level to 21V.

Table 1. Mode Selection

Mode \ Pins	CE (18)	OE/V_{PP} (20)	V_{CC} (24)	Outputs (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	High Z
Program	V_{IL}	V_{PP}	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+5	D_{OUT}
Program Inhibit	V_{IH}	V_{PP}	+5	High Z

Read Mode

The M2732A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

The M2732A has a standby mode which reduces the active power current by 66%, from 115 mA to 35 mA. The M2732A is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

Because EPROMs are usually used in larger memory arrays, Intel has provided a 2 line control function that accommodates this use of multiple memory connection. The two line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To use these two control lines most efficiently, it is recommended that $\overline{CE}$ (pin 18) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the outputs pins are only active when data is desired from a particular memory device.

Programming

Programming is the same as Intel's M2732 except for the programming voltage. In the program mode the M2732A $\overline{OE}/V_{PP}$ input is pulsed from a TTL low level to 21V (25V for the M2732). ***Exceeding 21.5V will damage the M2732A.***

Initially, and after each erasure, all bits of the M2732A are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The M2732A is in the programming mode when the $\overline{OE}/V_{PP}$ input is at 21V. It is required that a 0.1 μF capacitor be placed across $\overline{OE}/V_{PP}$ and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50 ms, active low, TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed. You can program any location at any time—either individually, sequentially, or at random. The program pulse has a maximum width of 55 ms. The M2732A must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Programming of the multiple M2732As in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled M2732As may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled M2732As.

7

Program Inhibit

Programming of multiple M2732As in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel M2732As may be common. A TTL level program pulse applied to a M2732A's $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at 21V will program that M2732A. A high level $\overline{CE}$ input inhibits the other M2732As from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL}. Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

ERASURE CHARACTERISTICS

The erasure characteristics of the M2732A are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase the typical M2732A in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M2732A is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the M2732A window to prevent unintentional erasure.

The recommended erasure procedure for the M2732A is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 μW/cm^2 power rating. The M2732A should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

PROGRAMMING

D.C. PROGRAMMING CHARACTERISTICS(1)

T_C = 25°C ±5°C; V_{CC} = 5V ±5%; V_{PP} = 21V ±0.5V

Symbol	Parameter	Limits				Test Conditions
		Min	Typ	Max	Unit	
I_{LI}	Input Current (All Inputs)			10	μA	$V_{IN} = V_{IL}$ or V_{IH}
V_{OL}	Output Low Voltage During Verify			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage During Verify	2.4			V	$I_{OH} = -400$ μA
I_{CC}	V_{CC} Supply Current		85	125	mA	
V_{IL}	Input Low Level (All Inputs)	−0.1		0.8	V	
V_{IH}	Input High Level (All Inputs Except OE/V_{PP})	2.0		V_{CC} + 1	V	
I_{PP}	V_{PP} Supply Current			35	mA	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{PP}$

NOTE:
1. When programming the M2732A, a 0.1 μF capacitor is required across $\overline{OE}/V_{PP}$ and ground to suppress spurious voltage transients which may damage the device.

A.C. PROGRAMMING CHARACTERISTICS

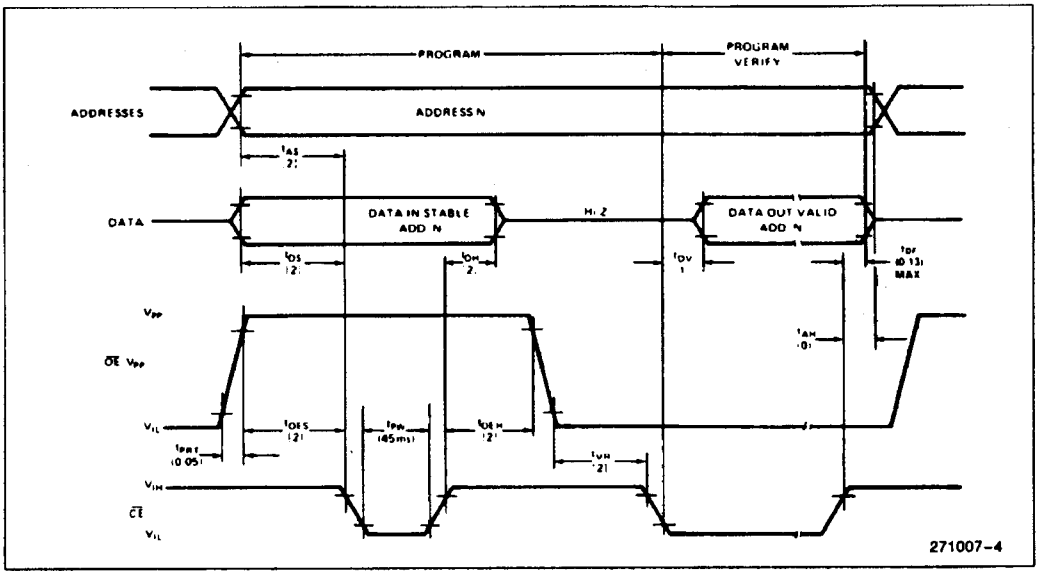
T_C = 25°C ±5°C; V_{CC} = 5V ±5%; V_{PP} = 21V ±0.5V

Symbol	Parameter	Limits				Test Conditions*
		Min	Typ	Max	Unit	
t_{AS}	Address Setup Time	2			µs	
t_{OES}	$\overline{OE}$ Setup Time	2			µs	
t_{DS}	Data Setup Time	2			µs	
t_{AH}	Address Hold Time	0			µs	
t_{OEH}	OE Hold Time	2			µs	
t_{DH}	Data Hold Time	2			µs	
t_{DF}	Chip Enable to Output Float Delay	0		130	ns	
t_{DV}	Data Valid from $\overline{CE}$			1	µs	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IL}
t_{PW}	$\overline{CE}$ Pulse Width During Programming	45	50	55	ms	
t_{PRT}	$\overline{OE}$ Pulse Rise Time During Programming	50			ns	
t_{VR}	V_{PP} Recovery Time	2			µs	

*A.C. TEST CONDITIONS

Input Rise and Fall Times (10% to 90%) ..... 20 ns
Input Pulse Levels ..... 0.45V to 2.4V
Input Timing Reference Level ..... 1.0V and 2.0V
Output Timing Reference Level ..... 0.8V and 2.0V

PROGRAMMING WAVEFORMS



NOTES:
1. All times shown in ( ) are minimum and in µs unless otherwise specified.
2. The input timing reference level is 1V for a V_{IL} and 2V for a V_{IH}.

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4050B
buffers
HEX non-inverting buffers

Product specification
File under Integrated Circuits, IC04

January 1995

Philips
Semiconductors

PHILIPS

HEX non-inverting buffers

HEF4050B buffers

DESCRIPTION

The HEF4050B provides six non-inverting buffers with high current output capability suitable for driving TTL or high capacitive loads. Since input voltages in excess of the buffers' supply voltage are permitted, the buffers may also be used to convert logic levels of up to 15 V to standard TTL levels. Their guaranteed fan-out into common bipolar logic elements is shown in the table below.

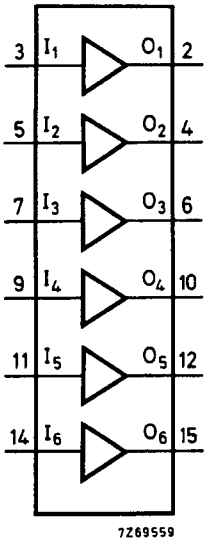


Fig.1 Functional diagram.

Guaranteed fan-out in common logic families

DRIVEN ELEMENT	GUARANTEED FAN-OUT
standard TTL	2
74 LS	9
74 L	16

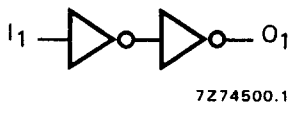


Fig.3 Logic diagram (one gate).

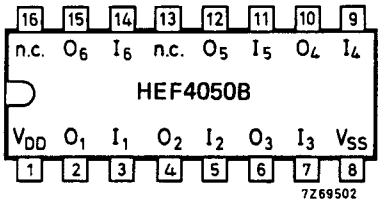


Fig.2 Pinning diagram.

HEF4050BP(N): 16-lead DIL; plastic (SOT38-1)
HEF4050BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
HEF4050BT(D): 16-lead SO; plastic (SOT109-1)
( ): Package Designator North America

APPLICATION INFORMATION

Some examples of applications for the HEF4050B are:

- LOCMOS to DTL/TTL converter
- HIGH sink current for driving 2 TTL loads
- HIGH-to-LOW level logic conversion

Input protection

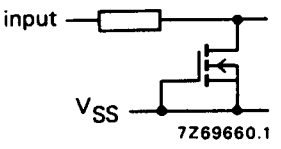


Fig.4 Input protection circuit that allows input voltages in excess of V_{DD}.

FAMILY DATA, I_{DD} LIMITS category BUFFERS

See Family Specifications

DC CHARACTERISTICS

V_{SS} = 0 V; V_I = V_{SS} or V_{DD}

HEF	V_{DD} V	V_O V	SYMBOL	T_{amb} (°C)						
				−40		+25		+85		
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Output (sink)	4,75	0,4		3,5	–	2,9	–	2,3	–	mA
current LOW	10	0,5	I_{OL}	12,0	–	10,0	–	8,0	–	mA
	15	1,5		24,0	–	20,0	–	16,0	–	mA
Output (source)	5	4,6		0,52	–	0,44	–	0,36	–	mA
current HIGH	10	9,5	$-I_{OH}$	1,3	–	1,1	–	0,9	–	mA
	15	13,5		3,6	–	3,0	–	2,4	–	mA
Output (source) current HIGH	5	2,5	$-I_{OH}$	1,7	–	1,4	–	1,1	–	mA

HEC	V_{DD} V	V_O V	SYMBOL	T_{amb} (°C)						
				−55		+25		+125		
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Output (sink)	4,75	0,4		3,6	–	2,9	–	1,9	–	mA
current LOW	10	0,5	I_{OL}	12,5	–	10,0	–	6,7	–	mA
	15	1,5		25,0	–	20,0	–	13,0	–	mA
Output (source)	5	4,6		0,52	–	0,44	–	0,36	–	mA
current HIGH	10	9,5	$-I_{OH}$	1,3	–	1,1	–	0,9	–	mA
	15	13,5		3,6	–	3,0	–	2,4	–	mA

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Propagation delays	5		35	70	ns	26 ns + (0,18 ns/pF) C_L
I_n O_n	10	t_{PHL}	20	35	ns	16 ns + (0,08 ns/pF) C_L
HIGH to LOW	15		15	30	ns	12 ns + (0,05 ns/pF) C_L
	5		55	110	ns	28 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	25	55	ns	14 ns + (0,23 ns/pF) C_L
	15		20	40	ns	12 ns + (0,16 ns/pF) C_L
Output transition	5		25	50	ns	7 ns + (0,35 ns/pF) C_L
times	10	t_{THL}	10	20	ns	3 ns + (0,14 ns/pF) C_L
HIGH to LOW	15		7	14	ns	2 ns + (0,09 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power	5	3 800 $f_i + \Sigma (f_o C_L) \times V_{DD}^2$	where
dissipation per	10	11 600 $f_i + \Sigma (f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
package (P)	15	65 900 $f_i + \Sigma (f_o C_L) \times V_{DD}^2$	f_o = output freq. (MHz)
			C_L = load capacitance (pF)
			$\Sigma (f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4047B
MSI
Monostable/astable multivibrator

Product specification
File under Integrated Circuits, IC04

January 1995

Philips
Semiconductors

PHILIPS

Monostable/astable multivibrator

HEF4047B
MSI

DESCRIPTION

The HEF4047B consists of a gatable astable multivibrator with logic techniques incorporated to permit positive or negative edge-triggered monostable multivibrator action with retriggering and external counting options.

Inputs include + TRIGGER, – TRIGGER, ASTABLE, $\overline{\text{ASTABLE}}$, RETRIGGER and MR (Master Reset). Buffered outputs are O, $\overline{\text{O}}$ and OSCILLATOR OUTPUT. In all modes of operation an external capacitor (C_t) must be connected between C_{TC} and RC_{TC}, and an external resistor (R_t) must be connected between R_{TC} and RC_{TC} (continued on next page).

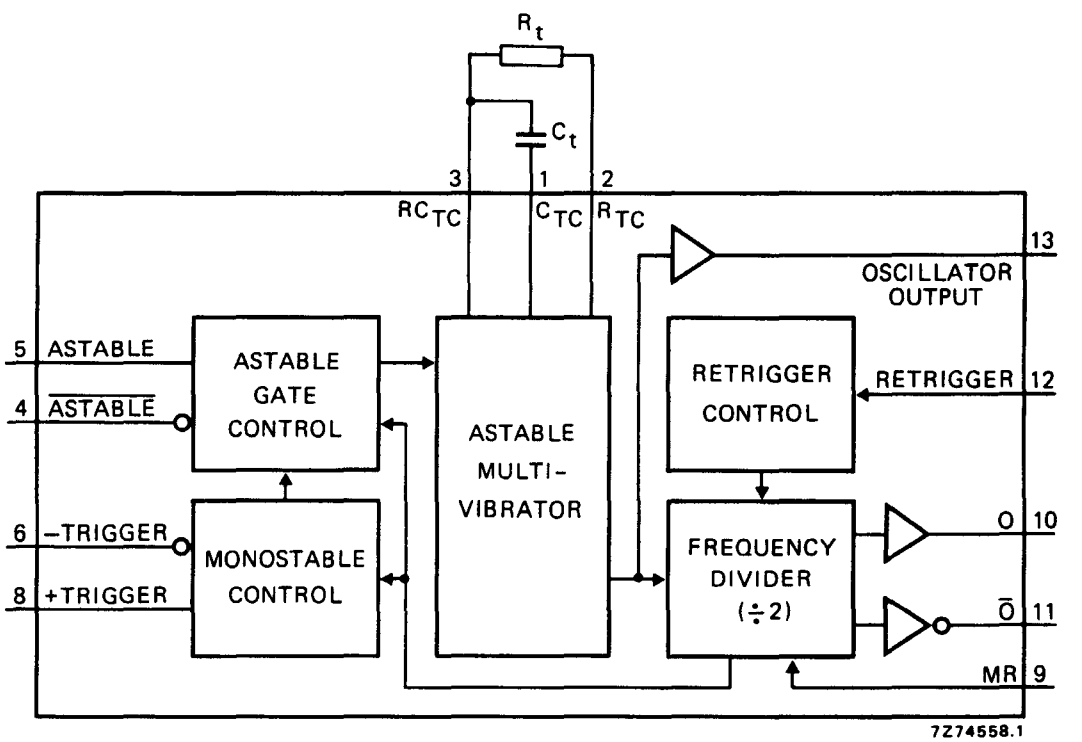


Fig.1 Functional diagram.

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

Astable operation is enabled by a HIGH level on the ASTABLE input. The period of the square wave at O and $\overline{O}$ outputs is a function of the external components employed. 'True' input pulses on the ASTABLE or 'complement' pulses on the $\overline{ASTABLE}$ input, allow the circuit to be used as a gatable multivibrator. The OSCILLATOR OUTPUT period will be half of the O output in the astable mode. However, a 50% duty factor is not guaranteed at this output.

In the monostable mode, positive edge-triggering is accomplished by applying a leading-edge pulse to the + TRIGGER input and a LOW level to the – TRIGGER input. For negative edge-triggering, a trailing-edge pulse is applied to the – TRIGGER and a HIGH level to the + TRIGGER. Input pulses may be of any duration relative to the output pulse. The multivibrator can be retriggered (on the leading-edge only) by applying a common pulse to both the RETRIGGER and + TRIGGER inputs. In this mode the output pulse remains HIGH as long as the input pulse period is shorter than the period determined by the RC components.

An external count down option can be implemented by coupling O to an external 'N' counter and resetting the counter with the trigger pulse. The counter output pulse is fed back to the $\overline{ASTABLE}$ input and has a duration equal to N times the period of the multivibrator. A HIGH level on the MR input assures no output pulse during an ON-power condition. This input can also be activated to terminate the output pulse at any time. In the monostable mode, a HIGH level or power-ON reset pulse must be applied to MR, whenever V_{DD} is applied.

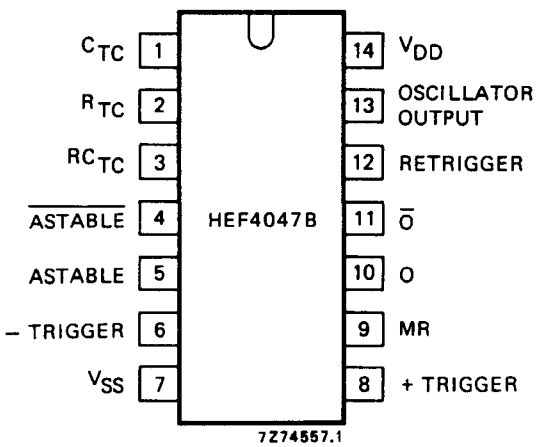
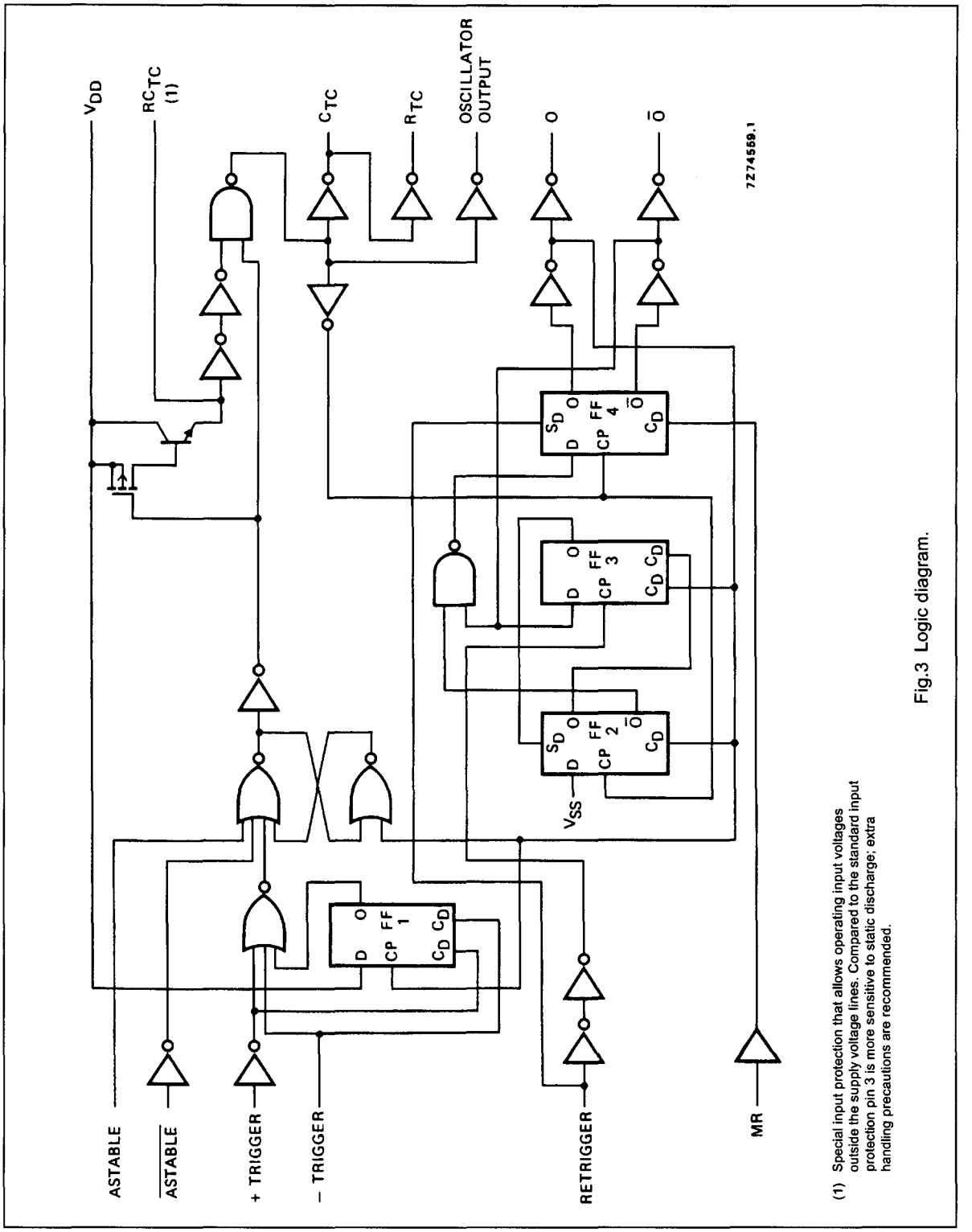


Fig.2 Pinning diagram.

HEF4047BP(N): 14-lead DIL; plastic (SOT27-1)
HEF4047BD(F): 14-lead DIL; ceramic (cerdip) (SOT73)
HEF4047BT(D): 14-lead SO; plastic (SOT108-1)
( ): Package Designator North America



(1) Special input protection that allows operating input voltages outside the supply voltage lines. Compared to the standard input protection pin 3 is more sensitive to static discharge; extra handling precautions are recommended.

Fig.3 Logic diagram.

FUNCTIONAL CONNECTIONS

FUNCTION	PINS CONNECTED TO			OUTPUT PULSE FROM PINS	OUTPUT PERIOD OR PULSE WIDTH
	V_{DD}	V_{SS}	INPUT PULSE		
astable multivibrator					
free running	4, 5, 6, 14	7, 8, 9, 12	–	10, 11, 13	at pins 10, 11:
true gating	4, 6, 14	7, 8, 9, 12	5	10, 11, 13	$t_A = 4{,}40\ R_tC_t$
complement gating	6, 14	5, 7, 8, 9, 12	4	10, 11, 13	at pin 13: $t_A = 2{,}20\ R_tC_t$
monostable multivibrator					
pos. edge-triggering	4, 14	5, 6, 7, 9, 12	8	10, 11	
neg. edge-triggering	4, 8, 14	5, 7, 9, 12	6	10, 11	at pins 10, 11:
retriggerable	4, 14	5, 6, 7, 9	8, 12	10, 11	$t_M = 2{,}48\ R_tC_t$
external count down[1]	14	5, 6, 7, 8, 9, 12	–	10, 11	

Notes

1. Input pulse to RESET of external counting chip; external counting chip output to pin 4.
2. In all cases, external resistor between pins 2 and 3, external capacitor between pins 1 and 3.

DC CHARACTERISTICS

V_{SS} = 0 V; inputs at V_{SS} or V_{DD}

	V_{DD} V	SYMBOL	T_{amb} (°C)					
			–40	+ 25		+ 85		
			MAX.	MIN.	MAX.	MAX.		
Leakage current pin 3; output transistor OFF	15	I_3	0,3	–	0,3	1	µA	pin 3 at V_{DD} or V_{SS}

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Propagation delays						
ASTABLE, $\overline{\text{ASTABLE}}$ → OSC. OUTPUT	5			95	190	68 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		45	90	43 ns + (0,23 ns/pF) C_L
	15			30	60	22 ns + (0,16 ns/pF) C_L
	5			85	170	58 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	80	29 ns + (0,23 ns/pF) C_L
	15			30	60	22 ns + (0,16 ns/pF) C_L
ASTABLE, $\overline{\text{ASTABLE}}$ → O, $\overline{\text{O}}$	5			150	300	123 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		65	130	54 ns + (0,23 ns/pF) C_L
	15			50	100	42 ns + (0,16 ns/pF) C_L
	5			130	260	103 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		60	120	49 ns + (0,23 ns/pF) C_L
	15			45	90	37 ns + (0,16 ns/pF) C_L
+/– TRIGGER → O, $\overline{\text{O}}$	5			160	320	133 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		65	130	54 ns + (0,23 ns/pF) C_L
	15			50	100	42 ns + (0,16 ns/pF) C_L
	5			155	310	128 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		65	130	54 ns + (0,23 ns/pF) C_L
	15			50	100	42 ns + (0,16 ns/pF) C_L
+ TRIGGER, RETRIGGER → $\overline{\text{O}}$	5			65	130	38 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		30	60	19 ns + (0,23 ns/pF) C_L
	15			25	50	17 ns + (0,16 ns/pF) C_L
+ TRIGGER, RETRIGGER → O	5			95	190	68 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	80	29 ns + (0,23 ns/pF) C_L
	15			30	60	22 ns + (0,16 ns/pF) C_L
MR → O	5			100	200	83 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		45	90	34 ns + (0,23 ns/pF) C_L
	15			35	70	27 ns + (0,16 ns/pF) C_L
MR → $\overline{\text{O}}$	5			100	200	83 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		45	90	34 ns + (0,23 ns/pF) C_L
	15			35	70	27 ns + (0,16 ns/pF) C_L
Output transition times	5			60	120	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	9 ns + (0,42 ns/pF) C_L
	15			20	40	6 ns + (0,28 ns/pF) C_L
	5			60	120	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	9 ns + (0,42 ns/pF) C_L
	15			20	40	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Minimum MR pulse width; HIGH	5	t_{WMRH}	60	30		
	10		30	15		
	15		20	10		
Minimum input pulse width; any input exept MR	5	t_W	220	110		
	10		100	50		
	15		70	35		

APPLICATION INFORMATION

General features:

- Monostable (one-shot) or astable (free-running) operation
- True and complemented buffered outputs
- Only one external R and C required

Monostable multivibrator features:

- Positive- or negative-edge triggering
- Output pulse width independent of trigger pulse duration
- Retriggerable option for pulse-width expansion
- Long pulse width possible using small RC components by means of external counter provision
- Fast recovery time essentially independent of pulse width
- Pulse-width accuracy maintained at duty cycles approaching 100%

Astable multivibrator features:

- Free-running or gatable operating modes
- 50% duty cycle
- Oscillator output available

1. Astable mode design information

a. Unit-to-unit transfer-voltage variations

The following analysis presents worst-case variations from unit-to-unit as a function of transfer-voltage (V_{TR}) shift for free running (astable) operation.

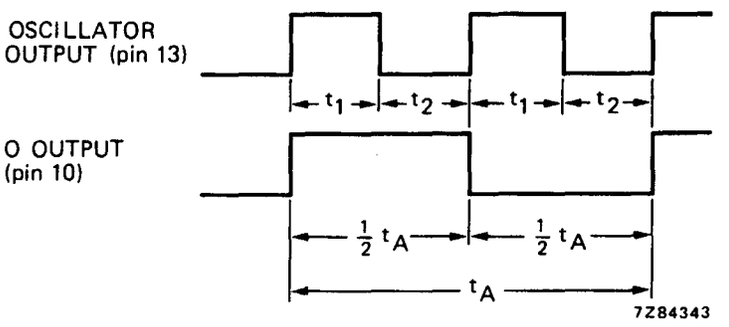


Fig.4 Astable mode waveforms.

$$t_1 = -R_tC_t \ln\frac{V_{TR}}{V_{DD}+V_{TR}}$$

$$t_2 = -R_tC_t \ln\frac{V_{DD}-V_{TR}}{2V_{DD}-V_{TR}}$$

$$t_A = 2(t_1+t_2) = -2R_tC_t \ln\frac{(V_{TR})(V_{DD}-V_{TR})}{(V_{DD}+V_{TR})(2V_{DD}-V_{TR})}$$, where t_A = Astable mode pulse width.

Values for t_A are:

V_{DD} = 5 or 10 V	typ. :	$V_{TR} = 0{,}5\ V_{DD}$;	$t_A = 4{,}40\ R_tC_t$
	min. :	$V_{TR} = 0{,}3\ V_{DD}$;	$t_A = 4{,}71\ R_tC_t$
	max.:	$V_{TR} = 0{,}7\ V_{DD}$;	$t_A = 4{,}71\ R_tC_t$
V_{DD} = 15 V	min. :	V_{TR} = 4 V;	$t_A = 4{,}84\ R_tC_t$
	max.:	V_{TR} = 11 V;	$t_A = 4{,}84\ R_tC_t$

thus if $\mathbf{t_A = 4{,}40\ R_tC_t}$ is used, the maximum variation will be (+ 7,0%; –0,0%) at 10 V.

b. Variations due to changes in V_{DD}

In addition to variations from unit-to-unit, the astable period may vary as a function of frequency with respect to V_{DD}. Typical variations are presented graphically in Figs 5 and 6 with 10 V as a reference.

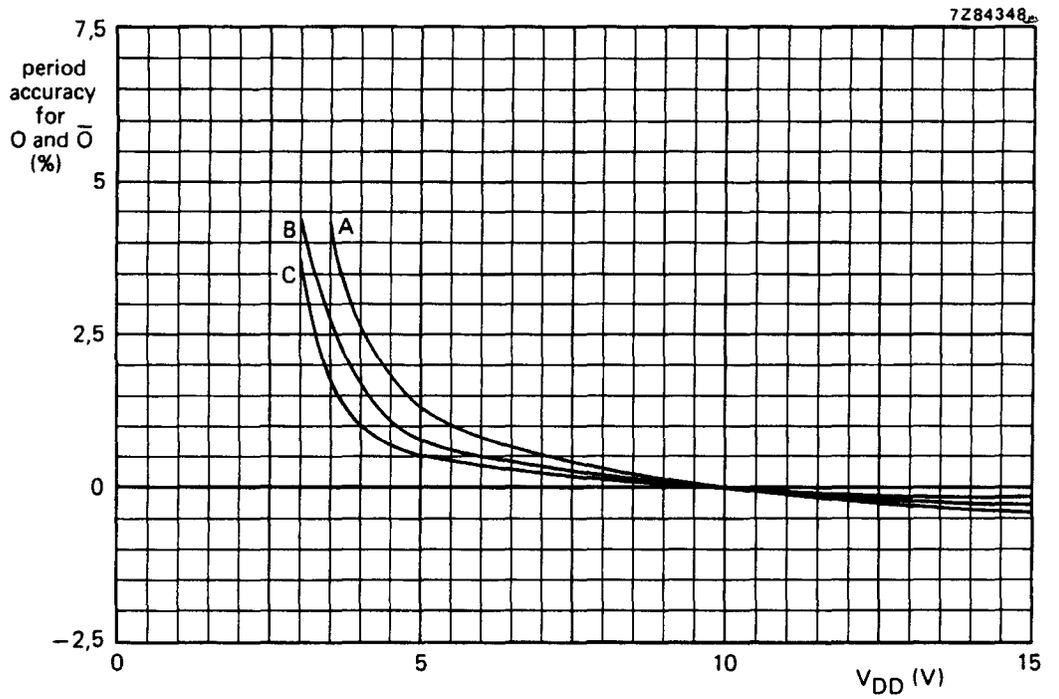


Fig.5 Typical O and $\overline{O}$ period accuracy as a function of supply voltage; astable mode; T_{amb} = 25 °C.

CURVE	f_O kHz	C_t pF	R_t kΩ
A	10	100	220
B	5	100	470
C	1	1000	220

RO - TN -	132	401	403	404	407	430
V_{10} (Θ=0°) [V]	1,15	1,51	1,60	1,78	1,48	1,45
V_{50} (Θ=0°) [V]	1,33	1,73	1,82	1,98	1,72	1,65
p_o (Θ=0°)	0,157	0,146	0,138	0,112	0,162	0,138
N_{max} (Θ=0°)	48	55	61	89	45	61
r_T (Θ=0°) [%/°C]	-0,78	-0,76	-0,50	-0,52	-0,59	-0,69
r_Θ ($V=V_{10}$) [%/°Θ]						
T_{C1} [°C]	61,2	69,4	82,2	104,9	71,0	69,2
T_m [°C]					<-10	
$\varepsilon_{\parallel}$	29,2	25,0	24,8	26,5	24,9	23,4
$\Delta\varepsilon$	+22,3	+19,0	+19,2	+21,4	+19,1	+17,6
n_o	1,515	1,524	1,524	1,519	1,52	1,525
Δn	0,193	0,234	0,258		0,23	0,234
k_{11} [10^{-12}N]						
k_{22} [10^{-12}N]						
k_{33}/k_{11}						
κ [10^{-12}N]						
γ_1 [mPa•s]						
η(+22°C) [mPa•s]	79	58	66	120	50	60
η(-20°C) [mPa•s]						
η(-30°C) [mPa•s]						
$\rho_{\parallel}$ [Ω•m]	$\geq 10^{8}$	$\geq 10^{8}$	$\geq 10^{8}$	$\geq 10^{8}$	$\geq 10^{8}$	$\geq 10^{8}$