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SRI JAGADGURU BALAGANGADHARANATHA SWAMIJI INSTITUTE OF TECHNOLOGY

A

PROJECT REPORT

ON

"An FPGA based Angular Encoder interface for a Radio Telescope"

SUBMITTED IN THE PARTIAL FULFILLMENT OF THE REQUIREMENT FOR THE VIII SEM B.E. CURRICULUM AS PRESCRIBED BY VISVESWARAIAH TECHNOLOGICAL UNIVERSITY

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CERTIFICATE

This is to certify that **RAJESHWARI DIVYA.B** and **SREEHARSHA.K** of 8th semester ECE bearing the register no. **1JB01EC037** and **1JB01EC052** have completed the project on **"AN FPGA BASED ANGULAR ENCODER INTERFACE FOR A RADIO TELESCOPE"** in the partial fulfillment of **Project Work—II (EC8P2)** prescribed by **Visveshwaraiah Technological University (Belgaum)** during the academic year **2004-05.**

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ACKNOWLEDGEMENT

As we discover ourselves at the tail end of this project, we recollect many indispensable events that enabled the proper and smooth completion of this work. Projects are never done in a vacuum. As such, a virtual cast of many is required to pull information together into a semblance of form and fitness. We are undoubtedly thankful to every one of the people who were in the background for such events to materialize, and we wish to recollect and acknowledge every one of them.

We express our gratitude to the following personalities for any and all combination of assistance, support, encouragement, patience, discussions, reassurance and unconditional solace.

We owe our immense gratitude to our project guide Prof.N Udaya Shankar, Raman Research Institute, for pioneering this project and helping us to contribute to this project.

We heartily thank Rishin.P.V and Krishnamurthy, Engineers at the Radio Astronomy and Astrophysics Lab, RRI, for their hard efforts and the full-hearted support in making the physical realization of such a task possible.

We owe our thanks to Girish.B.S, Engineer of the Digital Signal Processing Lab, RRI, for his support, without whose experience and guidance this project would have been unachievable.

We also thank the other friends and staff in the telescope observatory and the DSP lab at RRI for their encouragements and suggestions. Special thanks to Mrs. Mamatha Bai for her kind cooperation and help throughout. We also like to thank the other friends at RRI for giving us sweet moments to cherish.

We thank Mr.G.Madhavan, Executive Secretary of Indian Academy of Sciences for allowing us to use the resources and facilities at the organization.

On the college front we would like to thank Babu.N.V, lecturer and our guide at S.J.B.I.T for his valuable suggestions, encouragement and support.

We express our sincere gratitude to our dearest H.O.D of E& C Dept, S.J.B.I.T, Mr.Natraj.K.R for his patience, encouragement and moral support.

We heartily thank our dear Principal, at S.J.B.I.T, Dr.Puttaraju for his inspiration, support and care.

If all gratitude could be accumulated into one place, it would still be insufficient to repay for the endurance, patience, support, love and care shown by all the staff and our dearest friends at S.J.B.I.T.

If there were someone whom we don't want to thank, then they would be our parents, family members and friends close to our heart, since just thanking them would have no meaning. They are so indispensable for us that we dedicate all our work to them. Their constant support, encouragement, backing, immense love and care have made our dreams a reality.

Divya.B
Sreeharsha.K

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ABSTRACT

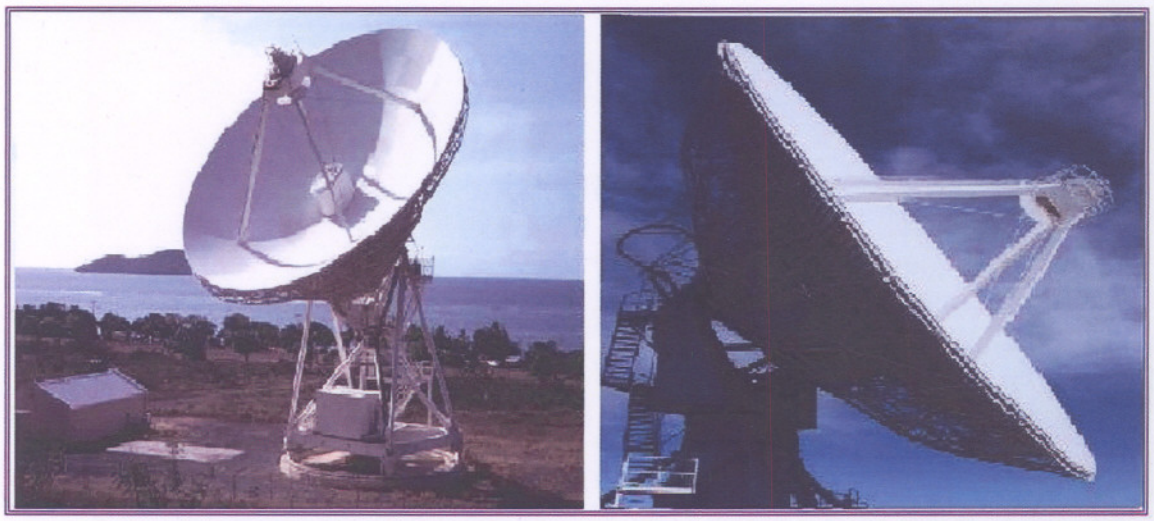
A control system for the 12m radio telescope is under development at the Raman Research Institute. The control system consists of two paths, one using a hardware controller called Programmable Multi Axis Controller (PMAC), and another using a Linux based Personal Computer.

In the Linux-based control system being developed, the system consists of a centralized PC which interfaces to the control system hardware through commercially off-the-shelf available Peripheral Component Interconnect based Data acquisition card and a 144-line Digital Input/Output card. The data acquisition card interfaces with position encoders to identify the direction of pointing of the radio telescope and motor drives for main control.

The software control system involves functions for reading the Encoder Data (EnDat) and Synchronous Serial Interface (SSI) type position encoders, functions for implementing servo algorithms like Proportional Integral Derivative (PID) to interface motor drives for motion control and source tracking programs for astronomical observations.

The feedback system consisting of functions like reading the positional information from the radio telescope involves the task of understanding the EnDat operation completely. The feedback could be achieved through Field Programmable Gate Array (FPGA) based system, that would take the burden of acquiring positional information from the encoders, store them and let the control system to read it as and when it needs it in a stretch. This would consistently save the time of the controller PC.

PREAMBLE



1. PREAMBLE

1.1 General Introduction

Man has been looking at the night sky since the very beginning of his existence on this earth. His view has been limited to the very narrow range of wavelengths that the eyes are capable of detecting.

Radio astronomy is the determination of the nature of celestial sources by the analysis of radio waves intercepted on the earth. The history of this field of research is only 70 years old, with the discovery by Karl Gothe Jansky in 1931 that radio waves from the cosmos reach Earth. Radio telescopes are used to study these naturally occurring radio emissions from galaxies, quasars and other astronomical bodies between wavelengths of about 10 meters (30MHz) and 1 millimeter (300GHz).

Fully steerable radio telescopes are placed on either an equatorial or an altitude - azimuth type mounting. Equatorial mount consists of two axes. One axis, called polar axis, is locked on to the north (or south) celestial pole and is thus parallel to the Earth's axis of rotation. The other, called the declination axis, is at right angles to the polar axis and pivots around it.

With an equatorial mount telescope, one can track a celestial object as it moves through the sky by turning the telescope about a single axis - the right ascension axis. Tracking motion can be easily achieved by countering for the earth's rotation and turning motion can be easily achieved by counteracting for the earth's rotation by turning the telescope about the right ascension axis at the same rate at which the earth rotates (1 degree in 4 minutes). Since the velocity required is a constant, a constant speed motor (synchronous motor) in conjunction with a gearbox can be successfully employed for tracking. Hence it is not mandatory for equatorial mount telescopes to be computer controlled to achieve tracking.

The main disadvantage with equatorial mount telescopes is that, they need careful polar alignment and hence longer setup time. The mounts required are heavier and expensive when used for large diameter radio telescopes, especially for those located away from the equator.

Very large radio telescopes are practically all of alt-azimuth type, because the vertical and horizontal axes allow much easier and inexpensive solutions of the various

mechanical problems in the design. Alt-azimuth mounts are easy to operate, less heavy compared to equatorial mounts. They allow the telescope to be moved in two initiative directions: altitude (vertical with respect to the horizon) and in azimuth (360 degrees of Horizontal motion). Aligning to the celestial pole (as you must equatorial mounts) is not required. You simply put the telescope on the mount with two orthogonal axes and start observing.

Efficient computerized alt-azimuth mount provides the advantage that mount can be placed at any altitude, and after a quick alignment, the telescope accurately tracks and finds objects across the sky. The system can be programmed for complex touring motions. Various control methods can be adopted to obtain enhanced performances.

1.2 Statement of problem

In the present system of radio telescope interfacing, a centralized Linux-based Personal Computer is involved in data acquisition. That involves healthy communication with the Radio Telescope encoders. The Heidenhain EnDat encoder of the 12m Radio Telescope is used to acquire positional information from the telescope. As the present feedback system used to obtain positional information involves direct communication between centralized computer and the angular encoders. This poses problems such as, the computer will have to waste its time in waiting process to acquire positional information, as the operating speed of the angular encoders are much lesser than that of computers used in the controlling system. A requirement for an alternate feedback concept has emerged leading to new idea of developing an FPGA-based system that would do the function of fetching and storing the positional information from the angular encoders so that the controlling computer can read these information in a stretch and save its valuable time.

Hence ***"An FPGA based Angular Encoder interface for A Radio telescope"*** is the project taken up to tackle this problem.

1.3 Objective of study

The objective of the study is to develop an FPGA-based feedback path to the angular encoder control system for the 12m Radio Telescope being built at RRI.

1.4 Scope of study

- The scope of study involves understanding the working of the Radio Telescope control system and the various sub-systems involved in it.
- It also involves understanding of interfacing the computer and the Radio Telescope control system using an FPGA-based system.
- Understanding various co-ordinate systems used in astronomy and calculations.
- Understanding various problems involved in interfacing hardware devices in the system.
- Understanding the concepts of system integration and testing.

1.5 Methodology

The FPGA-based system is used to acquire the positional information from the encoders and store that information in the FPGA so that, the Radio Telescope controller computer can read this information at a stretch and get back to its other operation instead of wasting its time in sending commands to the encoders and waiting for the data.

The steps involved in achieving the target and objective of this project will be:

1. Gathering sufficient information about the encoders used in the position sensing of the angular encoders of Radio telescope.
2. Selection of proper hardware to suit the requirement of the encoder's signal specifications, that includes developing an encoder interface card that could be used to communicate with the EnDat encoders.
3. Selecting the right FPGA system to suit this application.
4. Developing software that would do the required function of communicating with the encoders.
5. Testing these soft wares for correctness in the available simulation packages.
6. Finally, implementation of the design in the selected hardware.

1.6 Limitations of the study

The 12m Radio Telescope is still under construction. The mount or supporting structure for the dish is still under fabrication; hence testing of the system has been done using control system developed in-house.

Due to the time constraint the software developed for the required application were tested successfully in the simulation systems. Also the hardware developed were tested for correctness keeping all the constraints in mind.

RADIO TELESCOPE CONTROL SYSTEM

2. RADIO TELESCOPE CONTROL SYSTEM

2.1 Basic Radio telescope control system

A control system is a combination of elements arranged in a planned manner wherein each element causes an effect to produce a desired output a basic radio telescope control system is as shown in the fig. And consists of the following elements.

1. Position encoders, which gives information regarding the present position of the telescope.
2. A position controller, which gives information regarding the present position of the telescope at each instant, compares with the feedback received from the position encoders and issues a velocity command to the motor drives depending on the error in position.
3. Motor drives which rotate the motors at the commanded velocity issued by the position controller independent of the load
4. Motors, which steer the telescope to the expected position in the sky.

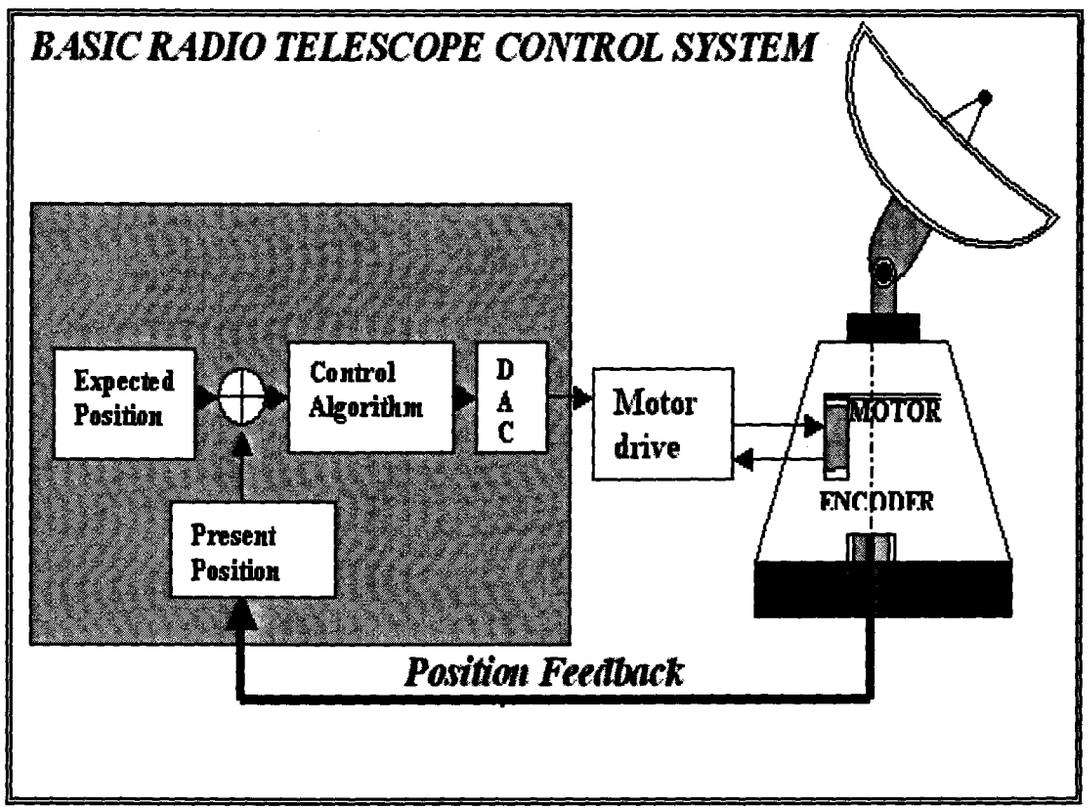


Fig.2.1 Basic Radio Telescope control system

At any instant our aim is to position the telescope continuously so that it tracks some particular source in the sky. For this we need a continuous position correction.

In the 12m Radio telescope control system a DSP based programmable multi axes controller is used as the position controller, PWM based brush less DC drives from Baldor are used for motor driver and four brush less DC motors from Baldor are used to steer the radio telescope, two for each axis. Heidenhain encoders are used for acquiring position of the radio telescope.

The encoders used are Heidenhain EnDat (Encoder Data), which is a bi-directional interface for encoders. Which is capable both of transmitting or updating information stored in t6he encoder, or saving new information. The monitoring of the position refers to keeping track of both elevation and azimuthal positions of the radio telescope.

The task of driving these EnDats is through the master control system. That is required to initialize the EnDats and get the positional information.

2.1.1 Encoder

An encoder is a mechanical device coupled to a rotating shaft that provides a digital representation of the shaft's position. In the control system the encoders are used to obtain the position feedback from the Radio Telescope. Modern encoders almost exclusively use optical techniques to convert the shaft's angle to digital form. The working of an optical encoder is as shown in the figure. A beam of light shines through a disk fixed to the spindle. Photocells detect marks on the disk. Optical encoders are basically classified into two types: 1. Incremental encoders and

2. Absolute encoders.

Incremental encoders generate two channels of pulse trains, which are 90 degrees phase shifted (also called quadrature pulses). Their optical disc consists of a fixed number of equally spaced opaque lines that produce a corresponding number of pulses per revolution. They can only give relative position. A counter in the receiver electronics just counts the number of pulses received from the start of motion to calculate the present

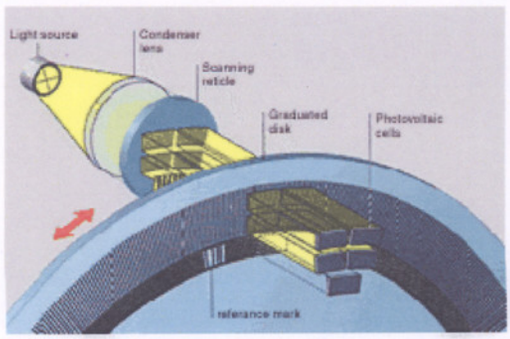


Fig.2.2 Photoelectric Scanning with incremental rotary encoders

position. The direction of rotation is obtained by monitoring the phase relation between the two channels. These encoders cannot store positional information on power off.

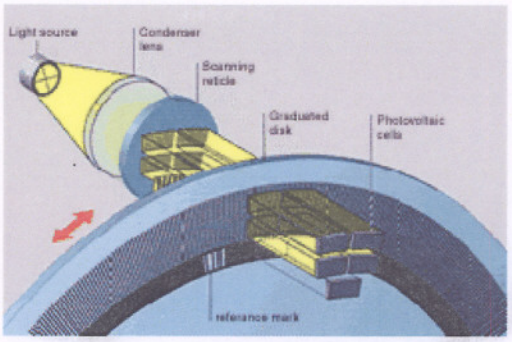


Fig.2.3 ***Photoelectric Scanning with absolute rotary encoders***

Absolute encoders generate a unique word output for each position. In a conventional absolute encoder, the pattern on the disk consists of a series of concentric incremental tracks, with the number of cycles per revolution doubling on each track on increasing radius. Each radius has its own photo detectors, and the tracks are arranged so that reading all the detectors generates a parallel binary word, usually in Gray or Binary code. When powered up from a random position the encoder can immediately tell the present position.

In the 12m Radio Telescope, we are using 17 bit absolute single turn encoders with a resolution of 10 arc sec for position feedback. The encoders are of optical disk type employing the industry standard EnDat protocol.

The EnDat interface is a digital, bi-directional, synchronous serial interface. It is capable of transmitting both the positional values from the encoders as well as transmitting or updating stored information in the encoder. It is also capable of saving information in the encoder memory.

The transmission method uses four signal lines- CLK, /CLK, DATA and /DATA. The signal transmission is at RS422 levels. The data transmitted is in synchronous with the clock signal from the control system.

2.2 Heidenhain EnDat

2.2.1 Serial EnDat

As a bi-directional interface, the EnDat (Encoder Data) interface for absolute encoders is capable of outputting absolute position values as well as requesting or

updating information stored in the encoder. Thanks to the serial data transmission, only four signal lines are required. The type of transmission (i.e., whether position values or

parameters) is selected through mode commands transmitted from the subsequent electronics to the encoder. Data is transmitted in synchronism with a CLOCK signal from the subsequent electronics.

2.2.2 Advantages of EnDat interface

- One interface for all absolute encoders, whereby the subsequent electronics can automatically distinguish between EnDat and SSI.
- Complementary output of incremental signals for highly dynamic control loops.
- Automatic self-configuration during encoder installation, since all information required by the subsequent electronics is already stored in the encoder.
- Reduced wiring cost. For standard applications six lines are sufficient.
- High system security through alarms and messages that can be evaluated in the subsequent electronics for monitoring and diagnosis. No additional lines are required.
- Minimized transmission times through adaptation of the data word length to the resolution of the encoder and through high clock frequencies.
- High reliability of transmission through cyclic redundancy checks
- Datum shift through an offset value in the encoder.
- It is possible to form a redundant system, since the absolute value and incremental signals are output independently from each other.

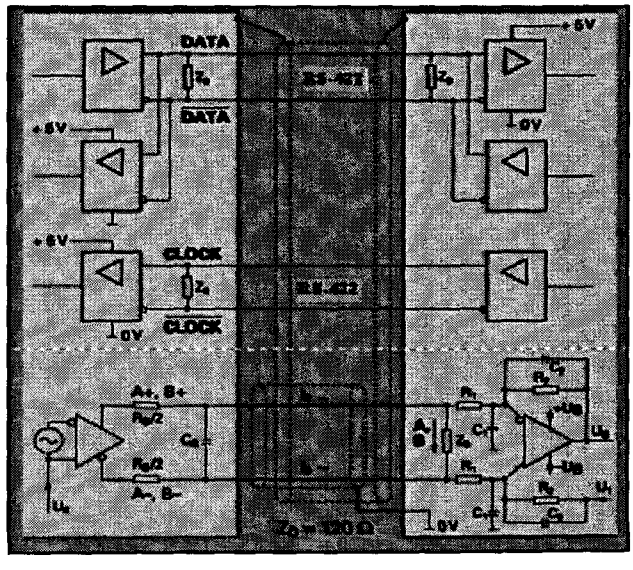


Fig.2.4 Recommended input circuitry of subsequent electronics

2.2.3 Description of function

The EnDat interface transmits position values or additional physical quantities in an unambiguous time sequence and serves to read out from and write to the encoder's internal memory. Position values can be transmitted with or without additional

Information. The additional information types are themselves selectable by the memory area and address. Other functions such as parameter reading and writing can also be called after the memory area has been selected.

2.2.4 Data transmission

A clock pulse (CLOCK) is transmitted by the subsequent electronics to synchronize data transmission. When not transmitting, the clock signal defaults to HIGH.

Without propagation-delay compensation, the clock frequency is variable between 100 kHz and 2 MHz. The maximum permissible clock frequency depends on the cable length between the encoder and subsequent electronics.

The subsequent electronics transmit the mode command Encoder transmit position values without additional information to the encoder. After the encoder has switched to transmission, i.e. after in total 10 clock periods, a counter in the subsequent electronics starts with every rising edge. The subsequent electronics measures the propagation time as the difference between the last rising clock pulse edge and the edge of the start bit.

2.2.5 Selecting transmission type

Transmitted data are distinguished as either position values or parameters. Position values and memory contents are transmitted serially over the data lines (DATA). The type of information to be transmitted is selected by mode commands. Mode commands define the content of the transmitted information. Every mode command consists of three bits. To ensure reliable transmission, every bit is transmitted redundantly (inverted or double). If the encoder detects an erroneous mode transmission, it transmits an error message.

No.	Mode command	Mode bit					
		M2	M1	M0	(M2)	(M1)	(M0)
1	Encoder transmit position values	0	0	0	1	1	1
2	Selection of the memory area	0	0	1	1	1	0
3	Encoder receive parameters	0	1	1	1	0	0
4	Encoder transmit parameters	1	0	0	0	1	1

Fig.2.5 Selecting mode bits

2.2.6 Acquiring positional values

One data packet is sent in synchronism per data transmission. The transmission cycle begins with the first falling clock edge. The measured values are saved and the position value calculated. After two clock pulses (2T), the subsequent electronics transmits the mode command Encoder transmit position value.

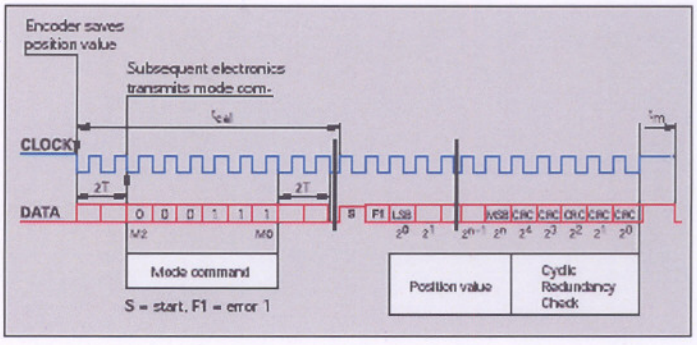


Fig.2.6 Acquiring positional values

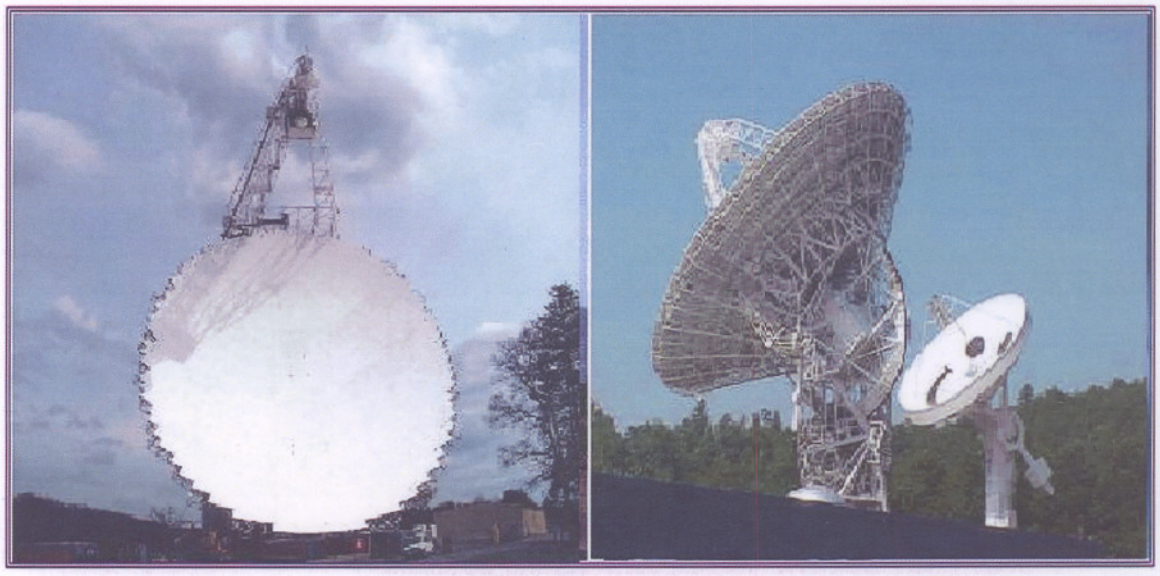
After successful calculation of the absolute position value, the start bit begins the data transmission from the encoder to the subsequent electronics. The subsequent error bit is a signal for all monitored functions and serve for failure monitoring.

The absolute position value is then transmitted, beginning with the LSB. Its length depends on the encoder being used. The number of required clock pulses for transmission of a position value is saved in the parameters of the encoder manufacturer. The data transmission of the position value is completed with the Cyclic Redundancy Check (CRC).

The position value is transmitted as a complete data word whose length depends on the resolution of the encoder. Transmission begins with the LSB (LSB first).

With the end of the data word, the clock must be set to HIGH.

HARDWARE APPLICATION AND SOFTWARE DESIGN



3. HARDWARE APPLICATION DEVELOPMENT

3.1 Design Flow

The project involves acquisition of data from the encoders by the FPGA-based system. This defines a new feedback path to the control system of the Radio Telescope.

Following are the hardware involved in this project:

- Heidenhain encoder, which transmits the positional information.
- An Encoder Interface Card that is used to communicate with the external environment and at the same time providing protection circuitry to the encoder.
- A Signal interface card that will be used to interface the signals from the encoder interface card with the FPGA-based system.
- An FPGA-based system that is used to generate the required signals to drive the encoder, and also to fetch and store the positional values received from the encoder.
- A PCI interface to enable computer to acquire these received positional information from the FPGA so that further processing of the encoder data could be carried out.

The positional information comprises of 17-bit positional value and 5 bits of CRC (Cyclic Redundancy Check) codes. A computer, is used to calculate the exact position of the Radio Telescope, finally receives this information.

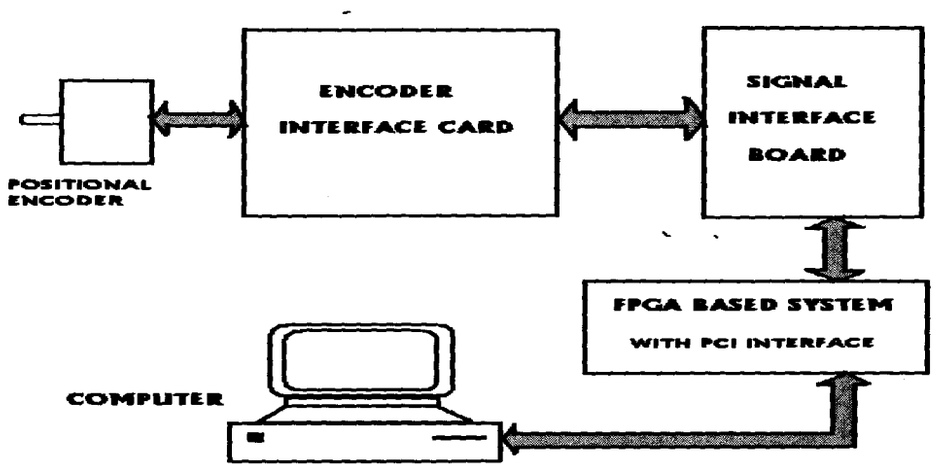


Fig.3.1 Communication path between Encoder and Computer via FPGA based system

3.2 Heidenhain encoder connection requirements

The Heidenhain EnDat encoder can transfer either position value or parameter. The clock signal for transfer of position values are sent by the subsequent electronics to synchronize the data output from the encoder. When not transmitting, the clock line is high. The transmission cycle begins with the first falling edge. The encoder saves the position value and calculates the position value.

The encoder communicates to the outer world (subsequent electronics) through EnDat ports.

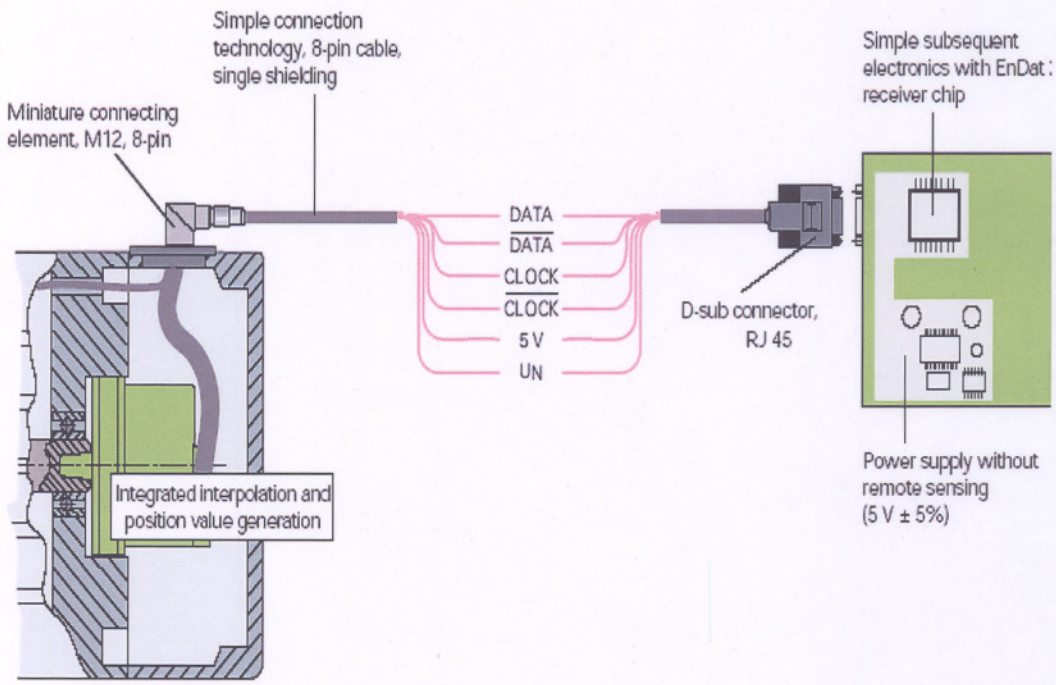


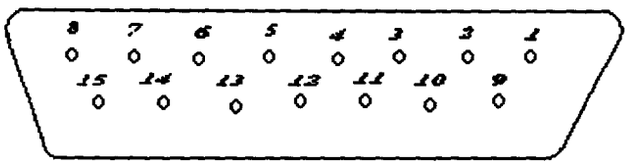
Fig.3.2 Encoder connecting to other electronics

EnDat can communicate with the external world through six lines, which include data, /data, clock, /clock, 5v Vcc and a Ground line. The standard connectors are used for this purpose of connection as shown in the figure above.

The specifications of the connector used in the connection of 12m Radio Telescope developed in RRI are as shown below.

3.2.1 15- PIN D-Sub connector for connecting Heidenhain EnDat to subsequent electronics

It is a female connector that runs from the core of the Heidenhain EnDat encoder. It has 15 pins. The power supply lines are also defined in it along with the grounding terminals.



15- pin D-Sub connector

1	2	3	4	5	6	7	8
HEID_VCC	HEID_GND	NC	NC	DATA	NC	NC	/DATA

9	10	11	12	13	14	15
VCC_ELC	NC	GND_ELC	NC	INT SHLD	CLK	/CLK

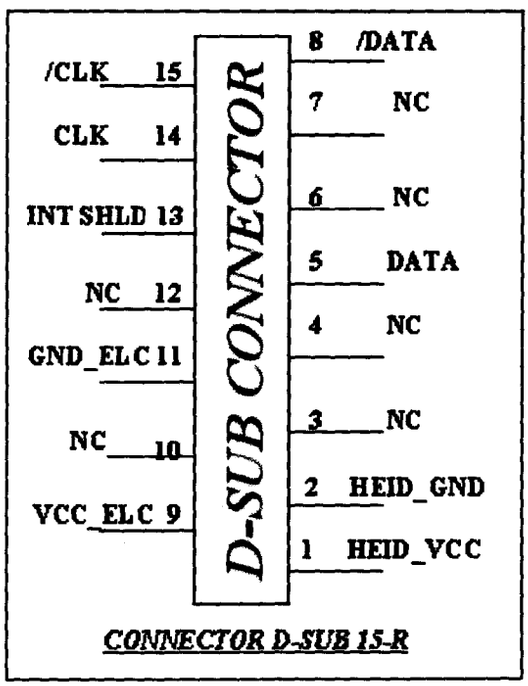


Fig.3.3 A 15-PIN D-Sub connector and its PIN details

3.3 ENCODER INTERFACE SYSTEM

3.3.1 Block Diagram

The real task starts from signal format synchronization of those of encoder and the FPGA based system. We have made use of an existing interface card developed for the 12m radio telescopes. That holds following components in it required for signal conversion n interface.

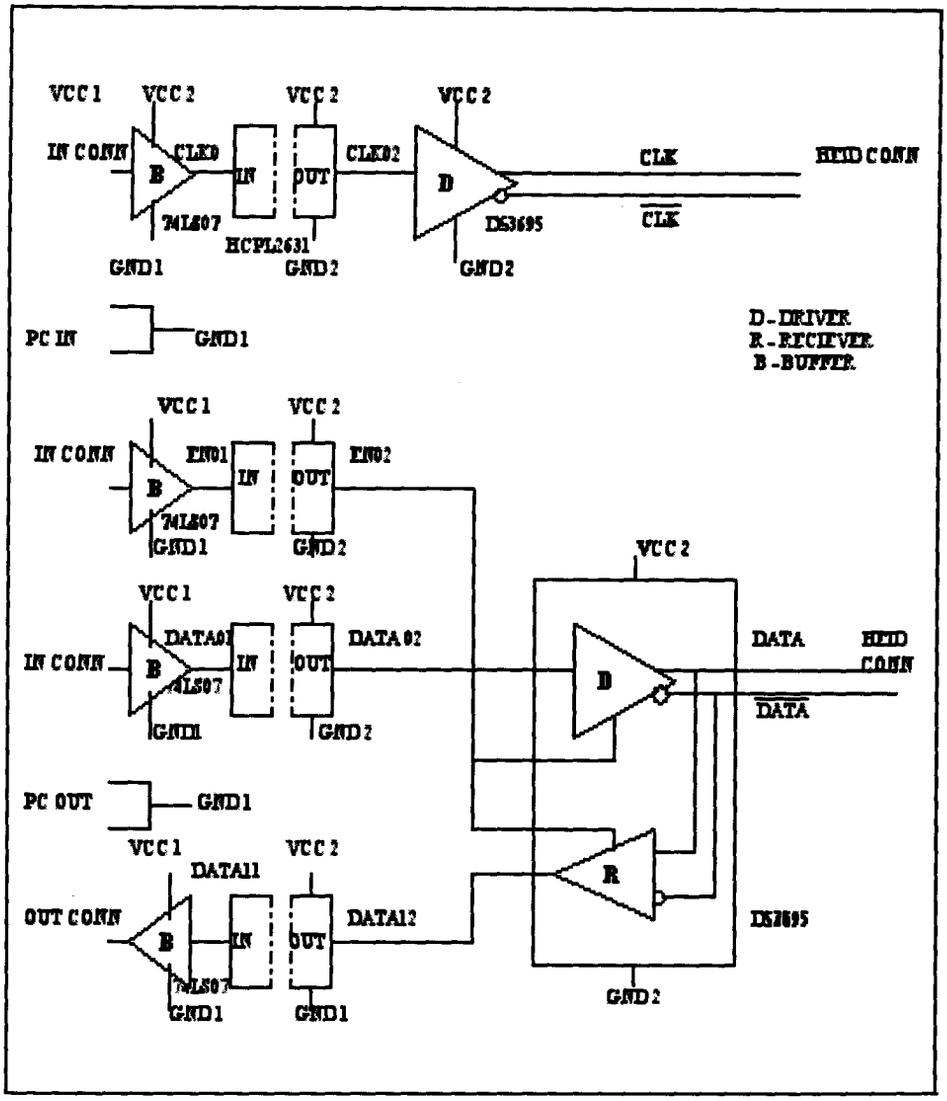
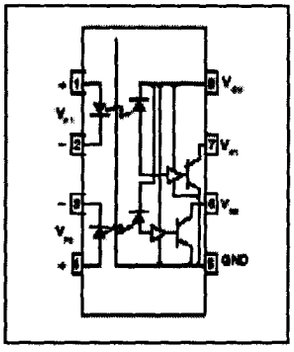


Fig.3.4 Block diagram of encoder interface card

The interface card that is shown in the block diagram consists of hardware required for connecting to the radio telescope encoders, i.e. Heidenhain devices. The interface card is connected to the encoder end used to establish communication with other electronics, which in this project is an FPGA, based system. The optocouplers used will form the barrier between the two parts of the circuit. That helps in ground loop elimination. Communication to the Heidenhain EnDat encoders has to be done only through the encoder interface board.

3.3.1.1 Dual-channel optocouplers (HCPL 2631)

Optocouplers are capable of transferring an electrical signal between two circuits while electrically isolating the circuits from each other. They generally consist of an infrared LED emitting section at the input and a silicon photo detector at the output.



HCPL-2631

Input	Enable	Output
H	H	L
L	H	H
H	L	H
L	L	H
H	NC	L
L	NC	H

Fig.3.5 Optocoupler HCPL 2631

HCPL-2630/2631 is a dual-channel optocouplers consist of an 850 nm AlGaAS LED, optically coupled to a very high-speed integrated photo detector logic gate with a strobable output. This output features an open collector, thereby permitting wired OR outputs. The coupled parameters are guaranteed over the temperature range of -40°C to +85°C. A maximum input signal of 5 mA will provide a minimum output sink current of 13 mA (fan out of 8). An internal noise shield provides superior common mode rejection.

FEATURES

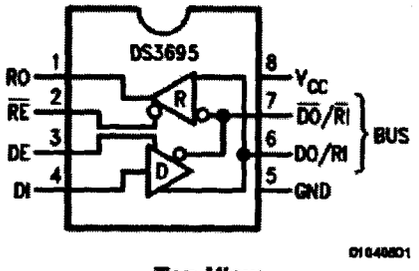
- Very high speed-10 MBit/s
- Superior CMR-10 kV/μs
- Double working voltage-480V
- Fan-out of 8 over -40°C to +85°C
- Logic gate output
- Strobable output
- Wired OR-open collector
- U.L. recognized (File # E90700)

APPLICATIONS

- Ground loop elimination
- LSTTL to TTL, LSTTL or 5-volt CMOS
- Line receiver, data transmission
- Data multiplexing
- Switching power supplies
- Pulse transformer replacement
- Computer-peripheral interface

3.3.1.2 Multipoint RS422 Transceivers/Repeaters (DS 3695)

The DS3695 is a high speed differential TRI-STATE® bus/line transceivers/repeaters designed to meet the requirements of EIA standard RS485. High impedance to bus with driver in TRI-STATE or with power off, over the entire common mode range allows the unused devices on the bus to be powered down.



Top View

Function Tables

DS3695 Transmitting

Inputs			Thermal Shutdown	Outputs	
$\overline{RE}$	DE	DI		$\overline{DO}$	DO
X	1	1	OFF	0	1
X	1	0	OFF	1	0
X	0	X	OFF	Z	Z
X	1	X	ON	Z	Z

DS3695 Receiving

Inputs			Outputs
$\overline{RE}$	DE	RI–$\overline{RI}$	RO
0	0	≥ +0.2V	1
0	0	≤ −0.2V	0
1	0	X	Z

Fig.3.6 DS3695 multipoint RS422 transceiver

3.3.1.3 HEX BUFFERS/DRIVERS

WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

These monolithic hex buffers/drivers feature high-voltage open-collector outputs to interface with high-level circuits or for driving high-current loads. They are also characterized for use as buffers for driving TTL inputs.

SN74LS07:

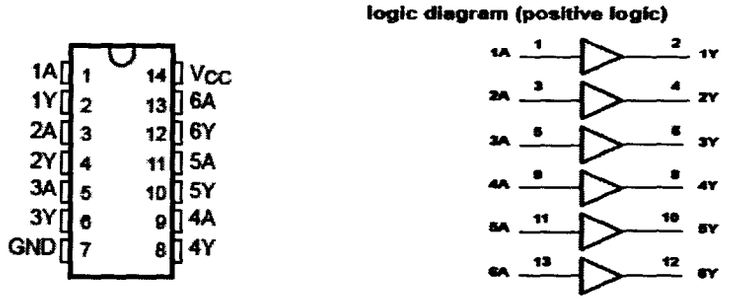


Fig.3.7 SN 74LS07 pin detail and logic diagram

The 4LS07 has a rated output voltage of 30. The maximum sink current is 30 mA. These circuits are compatible with most TTL families. Inputs are diode-clamped to minimize transmission-line effects, which simplifies design. Typical power dissipation is 140 mW and average propagation delay time is 12 ns.

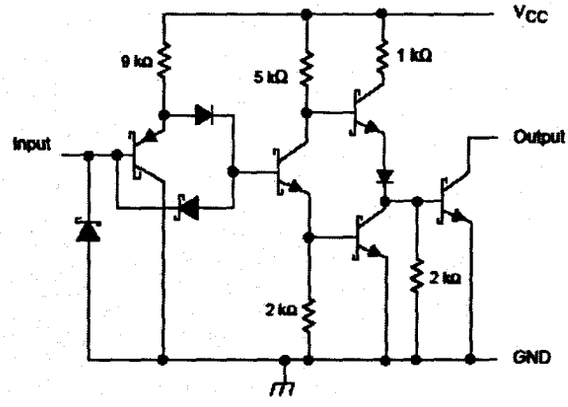


Fig.3.8 Schematic (each gate)

recommended operating conditions

			SN74LS07			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{OH}	High-level output voltage	'LS07			30	
I_{OL}	Low-level output current				40	mA
T_A	Operating free-air temperature		0		70	°C

Fig.3.9 Absolute maximum ratings over operating free-air temperature range

3.3.2 Circuit Diagram of Encoder Interface Card

The circuit connection of the Encoder interface card is as shown in the circuit diagram shown below.

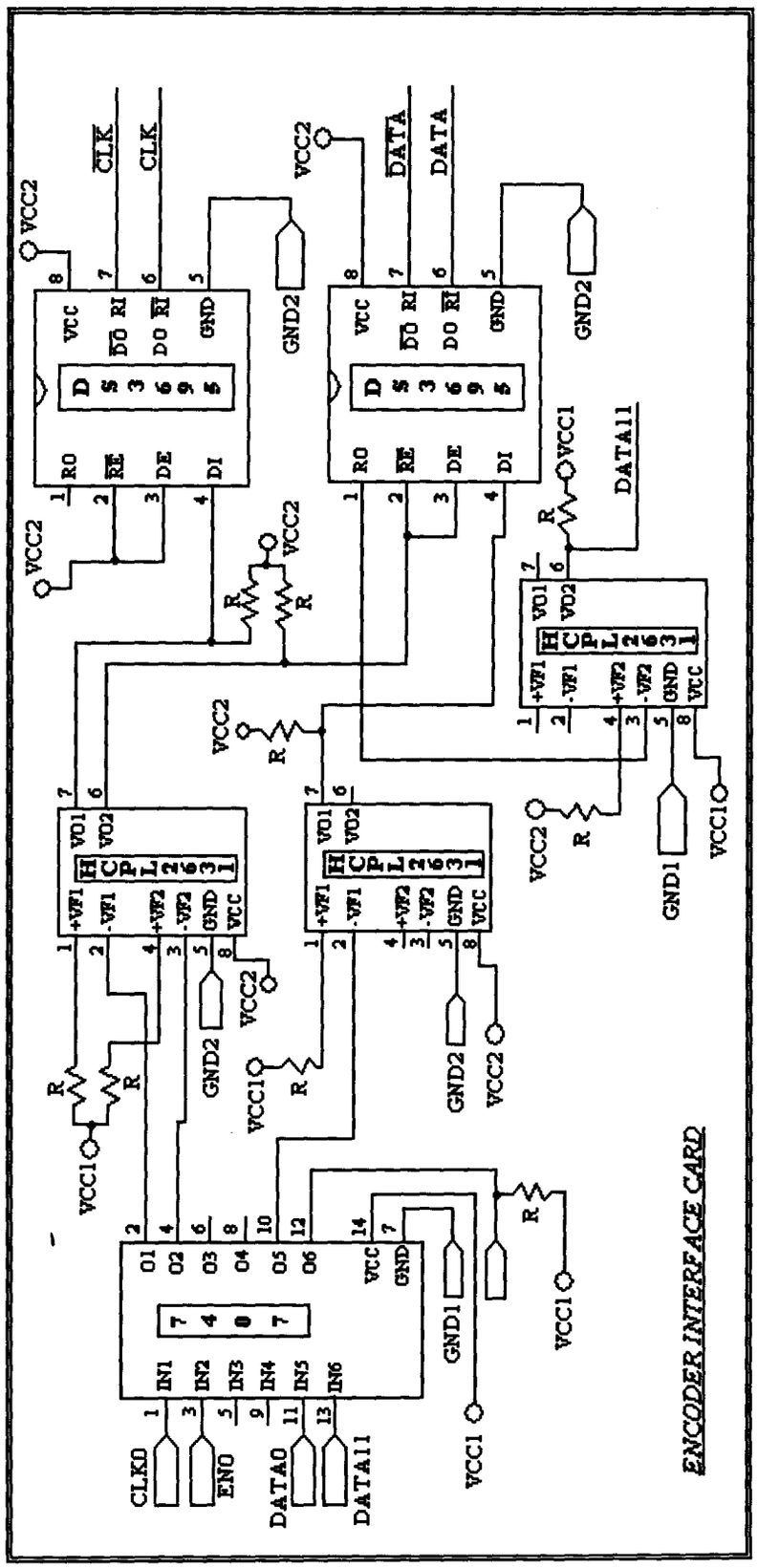


Fig.3.10 Circuit diagram of encoder interface card

Heidenhain EnDat encoder interface card developed is connecter to the female D-Sub connector. This will establish healthy communication path for communication to the Encoder. The encoder interface card has an optocoulper. Where, it is capable of transferring

an electrical signal between two circuits while electrically isolating the circuits from each other.

The interface card is connected to the Encoder end used to establish communication with other electronics, which in this project is an FPGA, based system.

In this card we can find the optocouplers forming the isolation between the two pars for the circuitry (i.e. between the encoder part of system and the other side which has the subsequent electronics to drive the encoder).

The clock and data signals from the EnDat are connected to the encoder interface card where in these differential signals are converted to single ended signals. This is achieved by using IC DS3695.

These signals are fed to the optocouplers. These optocouplers not only gives isolation between two ends of the circuitry system, it also provides safety to the system. Hence the signals are fed to the monolithic hex buffers /drivers. The output of these buffers will be single ended TTL signals.

The signals coming out of the encoder interface card will be characterized by four signals.

- Clock
- Data_in
- Data_out and
- Enable

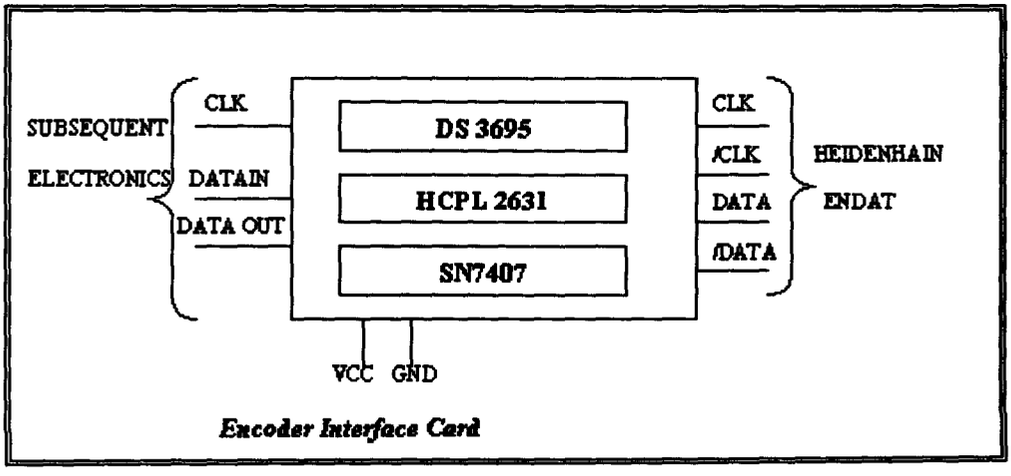


Fig. 3.11 Schematic of Encoder Interface Card with signals

The Heidenhain EnDat encoder data line is a single bi-directional line that carries mode commands as well as positional information on same channel.

Hence in the encoder interface card these lines are separated. This gives rise to Data_in and Data_out lines.

The Data_in is a line that carries the mode bits to the EnDat encoders from the FPGA system that generates it. And Data_out is the line that passes the calculated positional information from the Encoder to the FPGA system.

The enable line the encoder interface card will be used to decide the direction of flow of data in the Encoder data line. If he enable line is kept high then the Encoder data line will accept the mode bits sent through Data_in line of the encoder interface card.

And as the enable line is made low after sending the required mode bits, the Encoder will then start sending the positional values, which will be accepted by the FPGA system trough the Data_out line of the encoder interface card.

It is very much important to carefully connect the ground lines of both the electronics (Heidenhain encoder and Encoder interface card).

3.4 Signal interface board

The signals at the encoder interface card end are single ended and those signals generated from the FPGA based system developed are of differential form. This gives rise to need for development of this signal interface board. Which does the task of inter-conversion of signals between single ended TTL to Differential forms.

This could be achieved by selecting appropriate hardware available in market. That could be called as a differential line driver and receiver.

IC SN65LBC172 used is a differential line driver, and IC SN65LBC173 is a differential line receiver.

3.4.1 Circuit connection of signal interface board

The differential signals from the FPGA board are connected to the differential line driver and receiver. The lines connecting the differential sides are DATA_IN, /DATA_IN, CLK, /CLK, DATA_OUT, /DATA_OUT, ENB and /ENB.

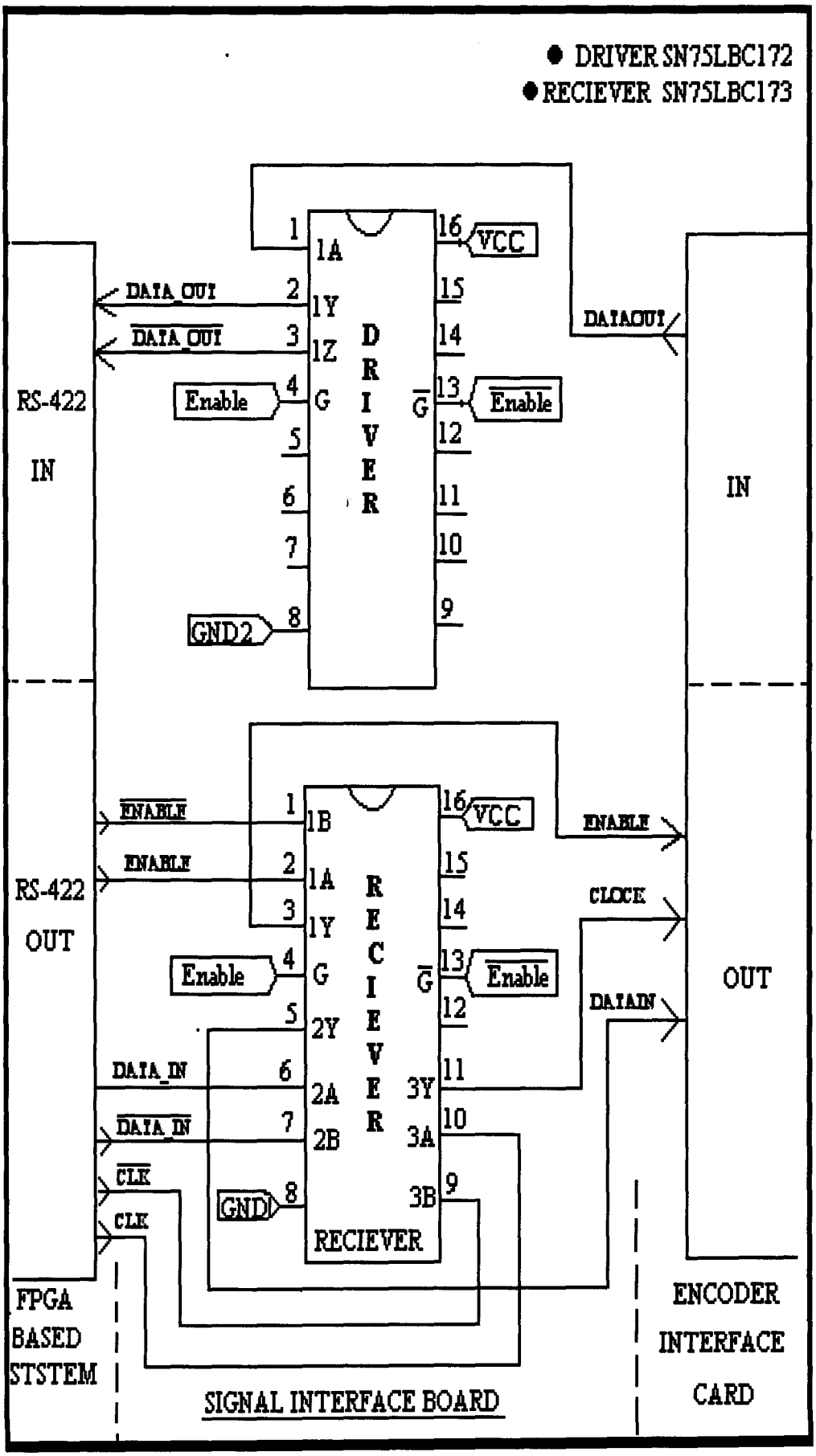
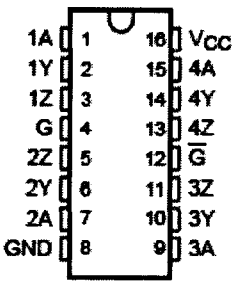


Fig.3.12 Signal interface board circuit diagram

The enable pin of the IC's are connected to the Vcc to maintain logic high to the pin through the pull up register. The IC's work in the range of Vcc-5v.The single ended TTL lines will be connected from the encoder interface card. The driver and the receiver ICs will share same ground base.

3.4.2 Differential line driver SN65LBC172



FUNCTION TABLE
(each driver)

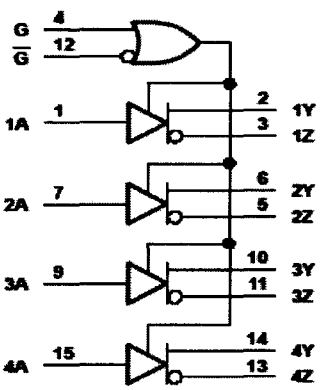
INPUT	ENABLES		OUTPUTS	
A	G	G	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

H = high level, L = low level,
X = irrelevant, Z = high impedance (off)

Fig.3.13 PIN description and function table of SN65LBC172

The SN65LBC172 and SN75LBC172 are monolithic quadruple differential line drivers with 3-state outputs. Designed for High-Speed Multipoint Transmission on Long Bus Lines in Noisy Environments. Support Data Rates up to and Exceeding Ten Million Transfers Per Second.

logic diagram (positive logic)



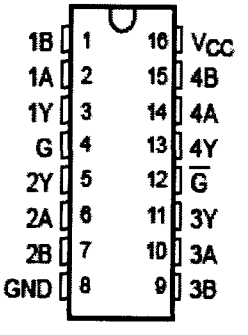
recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
Voltage at any bus terminal (separately or common mode), V_C	Y or Z			12	V
				-7	
High-level output current, I_{OH}	Y or Z			-60	mA
Low-level output current, I_{OL}	Y or Z			60	mA

Fig.3.14 Logic diagram and maximum ratings of operation of SN65LBC172

3.4.3 Differential line receiver SN65LBC173

The SN65LBC173 is a monolithic quadruple differential line receiver with 3-state outputs. Designed to meet the requirements of the ANSI standards EIA/TIA-422-B, EIA/TIA-423-B and RS-485. Receiver features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 mV over a common-mode input voltage range of 12 V to –7 V. The fail-safe design ensures that if the inputs are open circuited, the output is always high.



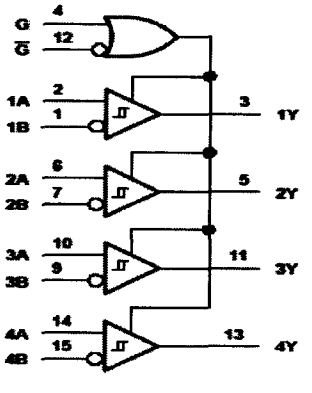
FUNCTION TABLE
(each receiver)

DIFFERENTIAL INPUTS A–B	ENABLES G	ENABLES $\overline{G}$	OUTPUT Y
$V_{ID} \geq 0.2$ V	H	X	H
	X	L	H
-0.2 V $< V_{ID} < 0.2$ V	H	X	?
	X	L	?
$V_{ID} \leq -0.2$ V	H	X	L
	X	L	L
X	L	H	Z
Open Circuit	H	X	H
	X	L	H

H = high level, L = low level, X = irrelevant,
Z = high impedance (off), ? = indeterminate

Fig.3.15 PIN detail and function table of SN65LBC173

logic diagram (positive logic)



recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Common-mode input voltage, V_{IC}		–7		12	V
Differential input voltage, V_{ID}				±6	V
High-level input voltage, V_{IH}	G inputs	2			V
Low-level input voltage, V_{IL}	G inputs			0.8	V
High-level output current, I_{OH}				–8	mA

Fig.3.16 Logic diagram and maximum ratings of operation of SN65LBC173

3.5 FPGA BASED SYSTEM

An FPGA-based system has two Spartan IIE 300K gate FPGA as core element and associated hardware such as pack CPLD for handling large array of Input/Output lines. A PCI chipset (PLX-9054) is used to acquire encoder data into the computer from the transact FPGA.

The FPGA based system is capable of communicating to external hardware using one of the three different ways mentioned below:

- RS-422 with 20 input lines and 8 output lines.
- Serial communication channel.
- Low voltage differential signaling |(LVDS) lines for interfacing high-speed signal (12 input lines and 5 output lines).

In our project we have used RS-422 lines to communicate with the encoder.

The signals coming from the signal interface card are connected to the RS-422 pins of the FPGA-based system board, which is in turn connected to FPGA via the pack CPLD.

The RS-422 input/output system consists of differential line drivers and receivers. Those drivers and receivers are perfectly compatible with the differential line drivers and receivers used in the signal interface board. The RS-422 IN has capability of accepting 20 different at a time. And similarly the RS-422 OUT has capability of handling 8 signals at a time.

3.5.1 Block diagram of FPGA based system

The signals from RS-422 are connected to the pack CPLD XC95144XL. Some programmable logic devices include integrated phase-locked loops (PLLs) and delay-locked loops (DLLs) with clock-frequency-synthesis capabilities so that designers can use CPLDs for system-on-chip applications. PLL and DLL clock multiplication also allows designers to generate a high-speed internal clock for sampling data in digital signal processing (DSP) applications. In addition, PLLs and DLLs provide greater control over the clock frequencies used in integrated designs. This is critical for system integration because different parts of a system operate at different clock frequencies.

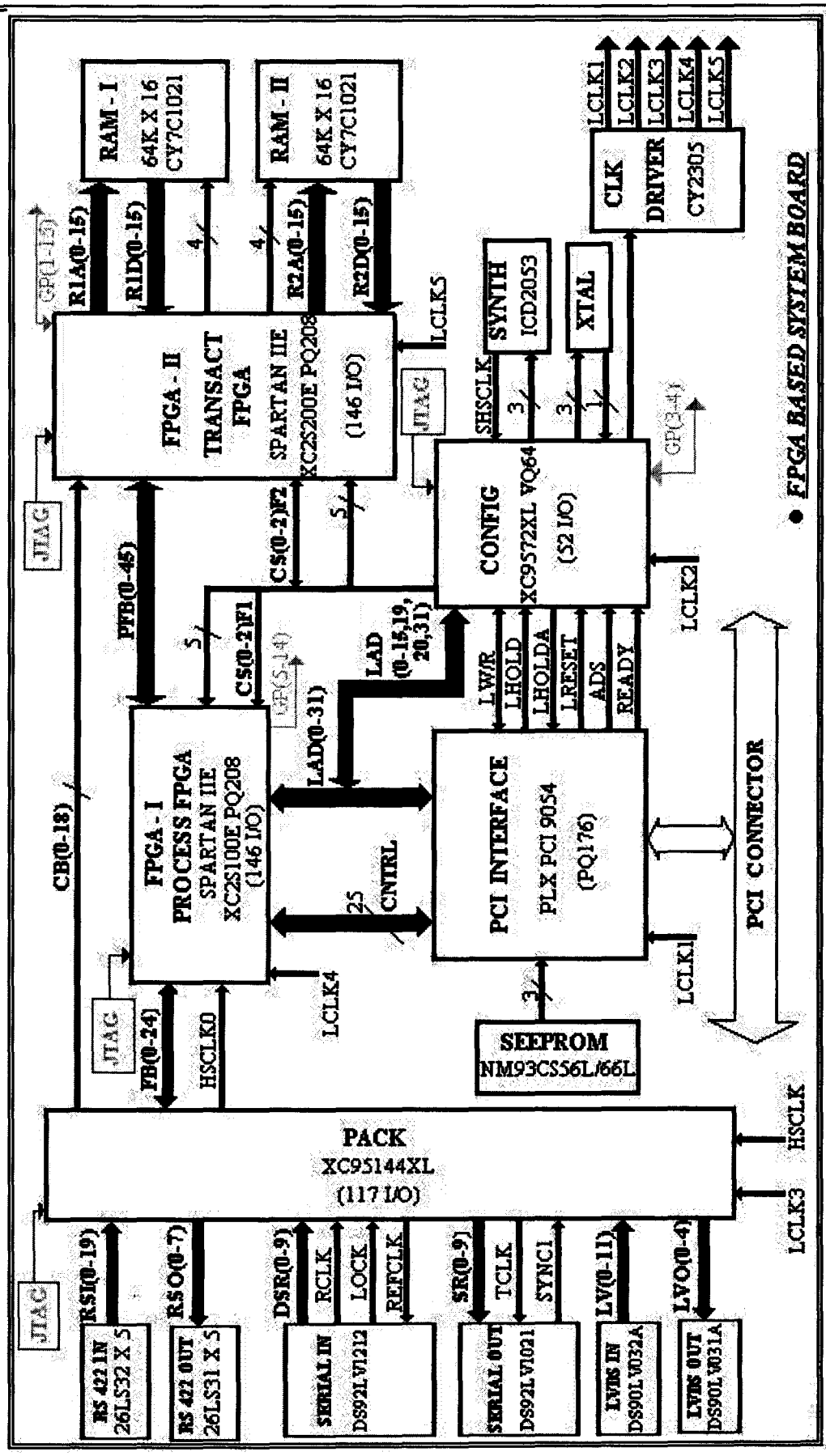


Fig.3.17 Block diagram of FPGA based system

Programming of the CPLD is through the JTAG port. A VHDL code has been developed defining the input/output pins and the operational specifications of it. The simulation package Xilinx Project Navigator was used to develop and test the VHDL codes. Software called Impact is used to program the CPLD.

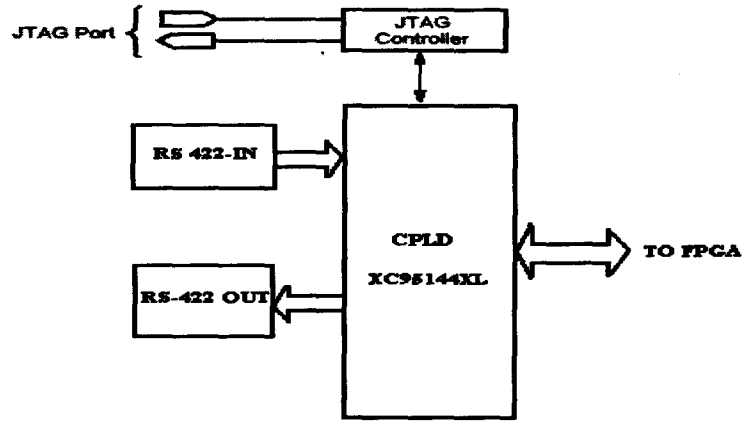


Fig.3.18 CPLD connected with neighboring devices and JTAG

FPGA forms the main core of this system board. It contains the logic required to communicate with the encoder. The VHDL code was developed using Xilinx Project Navigator and tested using ModelSim simulation package.

3.5.2 RS 422 Input / Output

RS422 Converters are devices, which enable connectivity between pieces of equipment, which operate different communications protocols. Protocol Converters are used for a variety of reasons, primarily to connect to specialized equipment, which still uses the older protocol.

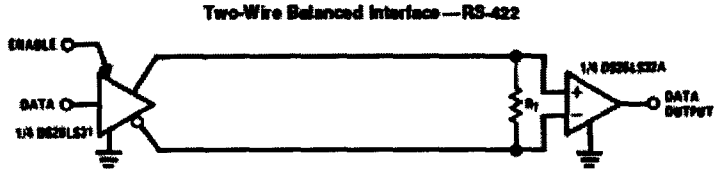


Fig.3.19 Two wire based interface of RS 422

RS 422 IN:

The DS26LS32 is a quad differential line receivers designed to meet the RS-422, RS-423 and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission. DS26LS32 meets all requirements of RS-422 and RS-423. The circuit provides an enable and disable function common to all four drivers.

RS 422 OUT:

The DS26LS31 is a quad differential line driver designed for digital data transmission over balanced lines. The DS26LS31 meets all the requirements of EIA Standard RS- 422 and Federal Standard 1020. It is designed to provide unipolar differential drive to twisted-pair or parallel-wire transmission lines. The circuit provides an enable and disable function common to all four drivers. The DS26LS31 features TRI-STATE outputs and logically ANDed complementary outputs.

3.5.3 Process FPGA (Spartan- IIE)

Process FPGA will communicate with the pack CPLD and the logic residing in the transact FPGA will generate the necessary signals to communicate with the encoder. Three signals are output from the transact FPGA and through the pack CPLD are transmitted to the encoder via the signal interface board and the encoder interface card. The signals are:

- Clock of frequency 100KHz with 50% duty cycle,
- Enable signal which will bifurcate the bi-directional data line of the encoder in to two lines,
- Data_out line that is used to transmit six mode bits to the encoder.

Similarly input to the FPGA will be a data line, i.e.:

- DATA_OUT that carries information serially in to the FPGA from encoder through pack CPLD.

3.5.4 JTAG Connector

FPGA system development board design provides a JTAG port that can be used to configure and/or program various devices on the board and JTAG devices located on the User I/O module.

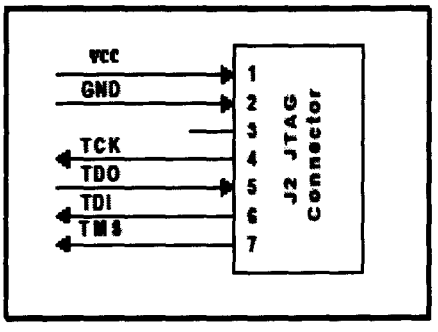


Fig.3.20 JTAG connector

Design Download

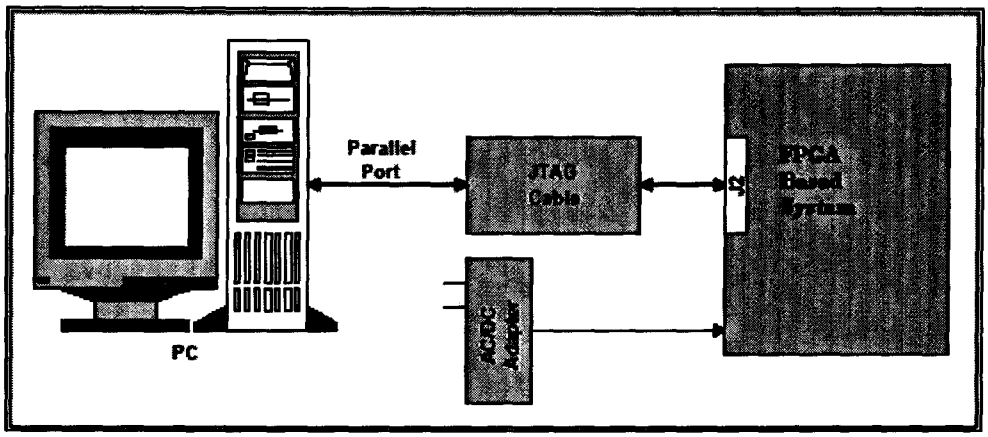


Fig.3.21 Design downloading procedure

The JTAG port on the FPGA based system board can be used to directly configure the Spartan-IIE FPGA. The J2 JTAG connector on the FPGA based system board can be used to configure the Spartan-IIE. The Insight JTAG cable is connected to the FPGA based system board via J2 at one end and to the PC parallel port at the other end.

Configuring the Spartan-IIE FPGA

When the JTAG port is used to configure the Spartan-IIE FPGA,

- Set the Configuration Mode of the Spartan-IIE FPGA to JTAG Mode.
- Use the Xilinx JTAG programmer (iMPACT) utility to load the design bit file into the Spartan-IIE FPGA.

3.5.5 Peripheral Component Interface (PCI) interfacing

The PCI Local Bus is a high performance 32- bit bus with multiplexed address and data lines. This type of internal bus is the most commonly used in today's systems. It is a 32-bit bus that supports data transfer rates at 33 MHz. Many modern expansion boards are connected to PCI slots.

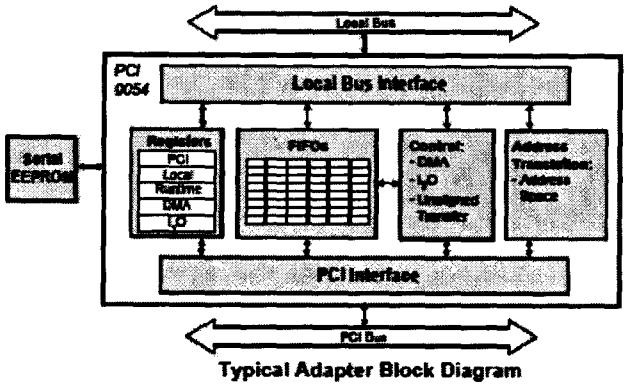


Fig. 3.22 Typical PCI block diagram

3.5.5.1 PLX PCI 9054

The PCI 9054, a 32-bit 33-MHz PCI Bus Master I/O Accelerator, is the most advanced general-purpose bus Master device available.

FEATURES

- PCI Specification version 2.2 (v2.2) compliant 32-bit, 33-MHz Bus Master Interface Controller with PCI Power Management features for adapters and embedded systems.
- General Purpose Bus Master Interface featuring advanced Data Pipe Architectur technology, which includes two DMA engines, programmable Target and Initiator Data Transfer modes and PCI messaging functions.
- 3.3V, 5V tolerant PCI and local signaling support Universal PCI Adapter designs.
- Programmable Local Bus runs up to 50 MHz and supports non-multiplexed 32-bit address/data, multiplexed 32-bit, and slave accesses of 8-, 16-, or 32-bit Local Bus devices.
- Serial EEPROM interface
- Three PCI-to-Local Address spaces

3.6 Software development

While developing the software for the required application, it is necessary to understand the constraints involved. In this project, developing the software needs proper understanding of the working of EnDat Encoder.

As the signals required to be generated by the FPGA system for the encoder to be driven are clock signal of frequency 10KHz and the enable signal that decides the flow

direction of data in the EnDat data line and the data line that carries the mode bits through it to initialize the encoder save the positional information and send it. This would require systematic development of the software design flow.

The EnDat encoder would send its current positional value as and when it receives the mode bits that would instruct it to do so. The mode bits will be sent with reference to the 100KHz clock signal.

The Algorithm to be developed in order to generate the proper signals required to collect data from the encoders would be as follows:

1. Generation of clock signal (CLK) of frequency 100KHz. With the duty cycle of 50 percent. Drive the enable signal to logic low so as to allow transfer of mode bits to the encoder.

2. Send the mode bits (000111 for acquiring the positional information from the encoder) at every falling edges of the clock signal after initial two clock cycles.
3. The encoder would have saved the current positional values in the first high to low transition of the clock signal and would be ready to send the positional information as the sent mode bit instructs it. Hence, pull the enable signal to logic high before that.
4. The encoder will send the positional information serially in synchronous to the clock signal sent to it. One bit at every rising edge of the clock signal will be sent. Hence, wait for the start bit, which is characterized by immediate transition to logic high from logic low on the incoming data line through which positional information is expected to arrive from the EnDat.
5. Once the start bit is sensed, start acquiring the incoming data. Start bit will be followed by an alarm bit or an error bit, then that is followed by 17 bit positional value that starting from LSB (2^0) to the MSB (2^{n-1}). These 17 bits positional values would be followed by 5 CRC (Cyclic Redundancy Check) bits. These information will be stored so as to enable the computer in the control system to read these information in a

stretch when signal is sent to it indication of arrival of complete positional value.

6. With the end of data word the clock signal must be set to logic high. After 30 to 1.25us the data line falls to logic low.

The program flow will start with initialization of the signals. And the signal exchange process follows the format as specified in the algorithm. This program has been developed in VHDL with the help of Xilinx Project Navigator software package.

The important signals to be kept in mind while developing the code are:

- *CLOCK*: Clock signal, is an output signal from the FPGA and is fed to the encoder via encoder interface card and signal interface board. Communication with the EnDat will be done with respect to this signal only.

- *ENABLE*: Enable signal, will be used in the encoder interface card to select between incoming data line and outgoing data line of the card to the side of FPGA based system board from EnDat encoder. This signal will be driven LOW when the FPGA transmits the mode commands to the EnDat and will be set to logic HIGH when the EnDat has to send the positional information.

- *MODEBITS*: It is a DATA line from the FPGA to EnDat encoder that carries the mode bits. The mode bits could be set to request the EnDat to send the positional information, parameter values or set the memory locations. In EnDat 2.2 version it is also possible to request it to send additional information like status information, address or even data.

- *POS_DATA*: This is DATA line coming from EnDat to the FPGA that carries positional information. This carries the start bit followed by en error bit or called alarm bit, then 17 bits of position value and then by 5 bits of CRC.

The clock signal of 100KHz, enable signal and mode bits are the signals generated in the FPGA system and sent to the encoders. The simulation of the software has been successfully carried out and the generation of these signals is as shown in the following waveforms.

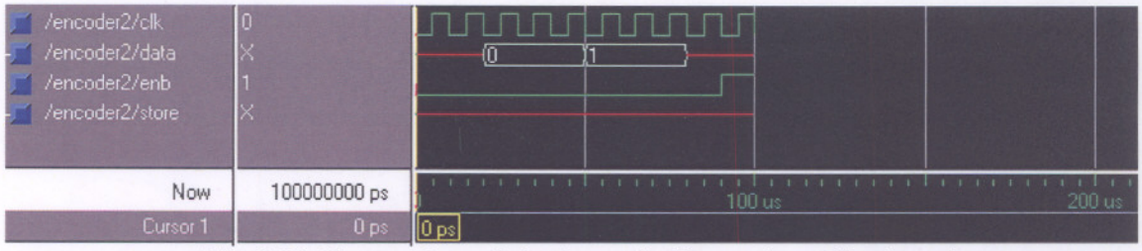


Fig.3.23 Generation of clock, mode bits and enable signal

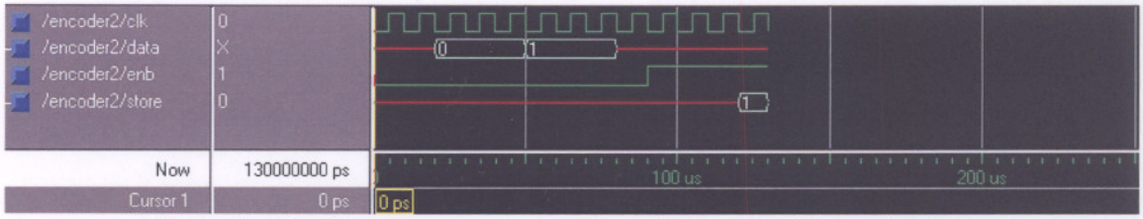
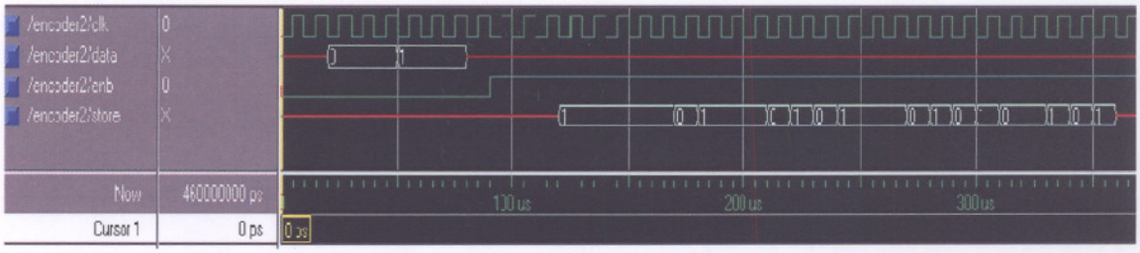
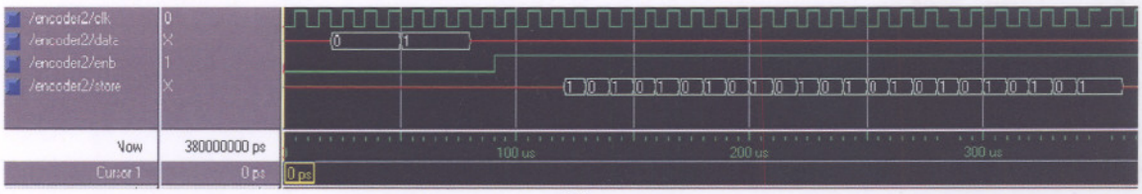


Fig.3.24 The Encoder starts sending information (start bit shown)



(a)



(b)

Fig.3.25 (a) and (b) Received positional information and CRC codes from encoder

The Fig.3.23 shows the generation of the clock pulses and mode bits when the enable signal is pulled down. The enable signal is sat to high after a clock cycle as the FPGA finishes sending mode bits.

The encoder starts sending positional information by sensing mode bits after two clock cycles (min). FPGA will start to store this information starting from the start bit as shown in waveform in Fig.3.24.

Samples of the positional information containing start bit, error bit, positional value and the CRC bits are as shown in fig.3.25 (a) and (b).

The positional value in the case (a) will be: 1101110101110101
Start bit I: 1, and the CRC is: 00101that ends with data line going high.

Similarly in case (b), positional value will be: 01010101010101010
Start bit is: 1, and CRC is: 10101 followed by logic high.

CONCLUSION

4 CONCLUSION

4.1 Summary of the work done

The project was undertaken to develop an FPGA-based angular encoder interface to a radio telescope. Development of intermediate hardware to connect the EnDat encoder to the application based FPGA system led to designing of the encoder interface card and the signal interface board.

The purpose of the development of encoder interface card was to provide proper isolation of the circuitry between EnDat and the FPGA system and also to bifurcate the bi-directional data line in two independent signal lines of opposite flow direction so that further processing of the signals will be easy.

A signal interface board was designed choosing suitable ICs and developed to solving the problem of interfacing the different signal formats. Finally, a VHDL code was developed to acquire the positional information from the encoder.

4.2 Scope for future work

The entire structure of the telescope is not yet ready. It is expected to be in operation soon. It will be an efficient work to connect the developed FPGA based feed back system in the actual telescope. This is the main task ahead. However many improvements can be made in the developed system to make it more versatile and reliable control system.

Further improvement could be made in both software and the hardware to enhance the system to take over complete responsibility of control path. That would not only provide cost effective solution, but also an efficient feedback system.

APPENDIX

Appendix A: Details of the components in the FPGA based system

1 FPGA: Spartan IIE

1.1 Introduction:

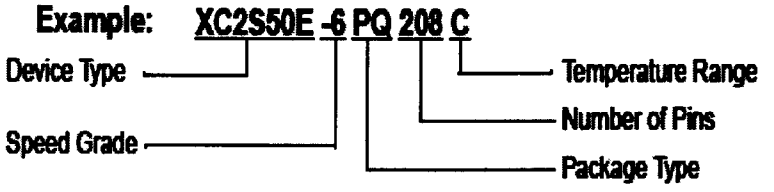
The Spartan-IIE 1.8V Field-Programmable Gate Array family gives users high performance, abundant logic resources, and a rich feature set, all at an exceptionally low price. The seven-member family offers densities ranging from 50,000 to 600,000 system gates. System performance is supported beyond 200 MHz. Spartan-IIE devices deliver more gates, I/Os, and features than other FPGAs by combining advanced process technology with a streamlined architecture. Features include block RAM (to 288K bits), distributed RAM (to 221,184 bits), 19 selectable I/O standards, and four DLLs (Delay-Locked Loops). Fast, predictable interconnect means that successive design iterations continue to meet timing requirements.

The Spartan-IIE family is a superior alternative to mask-programmed ASICs. The FPGA avoids the initial cost, lengthy development cycles, and inherent risk of conventional ASICs. Also, FPGA programmability permits design upgrades in the field with no hardware replacement necessary (impossible with ASICs).

1.2 Spartan-IIE FPGA Family Members:

Device	Logic Cells	Typical System Gate Range (Logic and RAM)	CLB Array (R x C)	Total CLBs	Maximum Available User I/O[1]	Maximum Differential I/O Pairs	Distributed RAM Bits	Block RAM Bits
XC2S50E	1,728	23,000 - 50,000	16 x 24	384	182	83	24,576	32K
XC2S100E	2,700	37,000 - 100,000	20 x 30	600	202	86	38,400	40K
XC2S150E	3,888	52,000 - 150,000	24 x 36	864	265	114	55,296	48K
XC2S200E	5,292	71,000 - 200,000	28 x 42	1,176	289	120	75,264	56K
XC2S300E	6,912	93,000 - 300,000	32 x 48	1,536	329	120	98,304	64K
XC2S400E	10,800	145,000 - 400,000	40 x 60	2,400	410	172	153,600	160K
XC2S600E	15,552	210,000 - 600,000	48 x 72	3,456	514	205	221,184	288K

Ordering Information



Device Part Marking

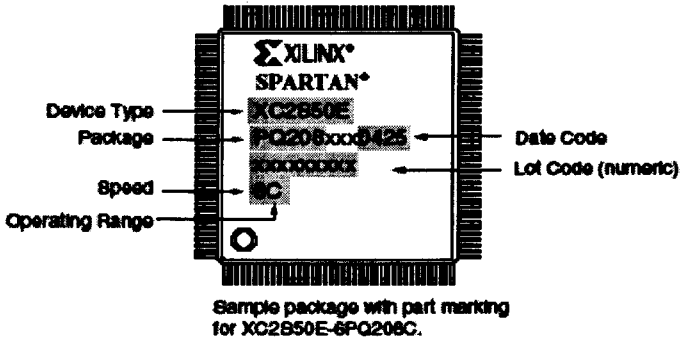


Fig. 1.1 Xilinx FPGA Device part marking and ordering information

The Spartan-IIE family of FPGAs has a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), surrounded by a perimeter of programmable Input/Output Blocks (IOBs). There are four Delay-Locked Loops (DLLs), one at each corner of the die. Two columns of block RAM lie on opposite sides of the die, between the CLBs and the IOB columns. These functional elements are interconnected by a powerful hierarchy of versatile routing channels.

Spartan-IIE FPGAs are customized by loading configuration data into internal static memory cells. Unlimited reprogramming cycles are possible with this approach. Stored values in these cells determine logic functions and interconnections implemented in the FPGA. Configuration data can be read from an external serial PROM (master serial mode), or written into the FPGA in slave serial, slave parallel, or Boundary Scan modes. Spartan-IIE FPGAs achieve high-performance, low-cost operation through advanced architecture and semiconductor technology.

1.3 Basic Spartan-IIE FPGA block diagram:

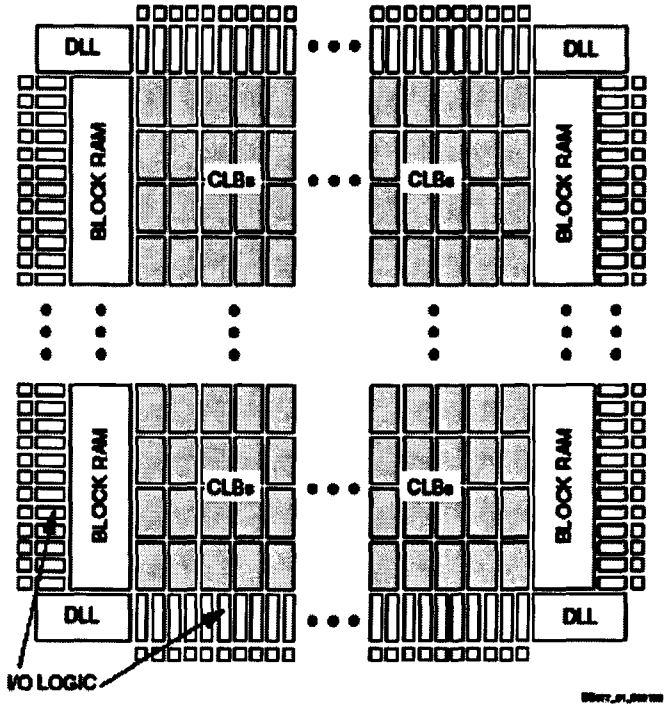


Fig.1.2 Basic Spartan-IIE Family FPGA Block Diagram

1.4 Spartan-IIE Array

The Spartan-IIE user-programmable gate array, shown in Figure, is composed of five major configurable elements:

- IOBs provide the interface between the package pins and the internal logic
- CLBs provide the functional elements for constructing most logic
- Dedicated block RAM memories of 4096 bits each
- Clock DLLs for clock-distribution delay compensation and clock domain control
- Versatile multi-level interconnect structure

1.4.1 Configurable Logic Block (CLB)

The basic building block of the Spartan-IIE CLB is the logic cell (LC). An LC includes a 4-input function generator; carry logic, and storage element. The output from the function generator in each LC drives the CLB output or the D input of the flip-flop. Each Spartan-IIE CLB contains four LCs, organized in two similar slices; a single slice is shown in Figure.

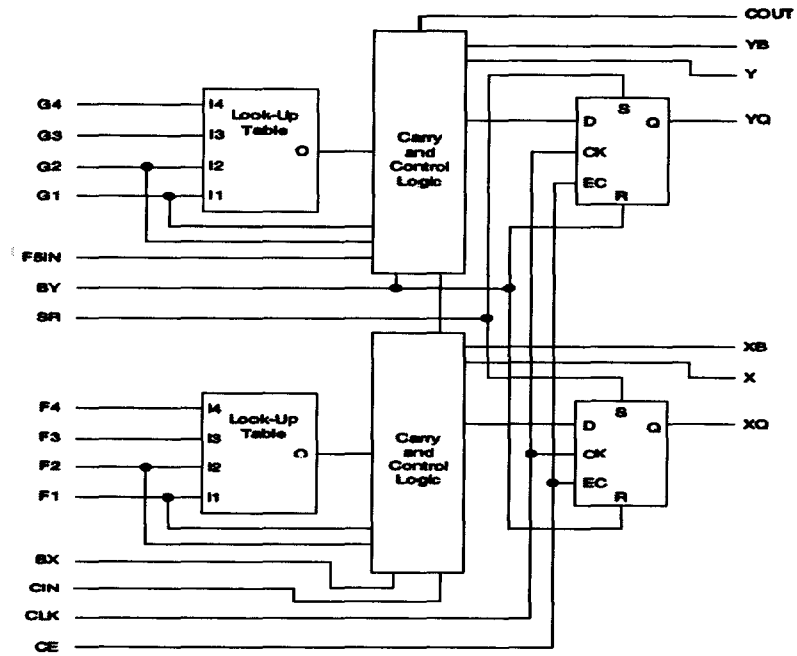


Fig.1.3 Spartan-IIE CLB Slice (two identical slices in each CLB)

In addition to the four basic LCs, the Spartan-IIE CLB contains logic that combines function generators to provide functions of five or six inputs.

Look-Up Tables

Spartan-IIE function generators are implemented as 4-input look-up tables (LUTs). In addition to operating as a function generator, each LUT can provide a 16 x 1-bit synchronous RAM. Furthermore, the two LUTs within a slice can be combined to create a 16 x 2-bit or 32 x 1-bit synchronous RAM, or a 16 x 1-bit dual-port synchronous RAM. The Spartan-IIE LUT can also provide a 16-bit shift register that is ideal for capturing high-speed or burst-mode data. This mode can also be used to store data in applications such as Digital Signal Processing.

Arithmetic Logic

Dedicated carry logic provides fast arithmetic carry capability for high-speed arithmetic functions. The Spartan-IIE CLB supports two separate carry chains, one per slice. The height of the carry chains is two bits per CLB. The arithmetic logic includes an XOR gate that allows a 1-bit full adder to be implemented within an LC. In addition, a dedicated AND gate improves the efficiency of multiplier implementations. The dedicated carry path can also be used to cascade function generators for implementing wide logic functions.

1.4.2 Block RAM

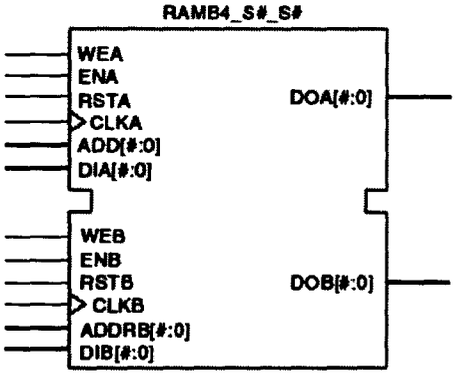


Fig.1.4 Dual-Port Block RAM

Spartan-IIE FPGAs incorporate several large block RAM memories. These complements the distributed RAM Look-Up Tables (LUTs) that provide shallow memory structures implemented in CLBs. Block RAM memory blocks are organized in columns. Most Spartan-IIE devices contain two such columns, one along each vertical edge. Each memory block is four CLBs high, and consequently, a Spartan-IIE device 16 CLBs high will contain four memory blocks per column, and a total of eight blocks.

The Spartan-IIE block RAM also includes dedicated routing to provide an efficient interface with both CLBs and other block RAMs.

1.4.3 Delay-Locked Loop (DLL)

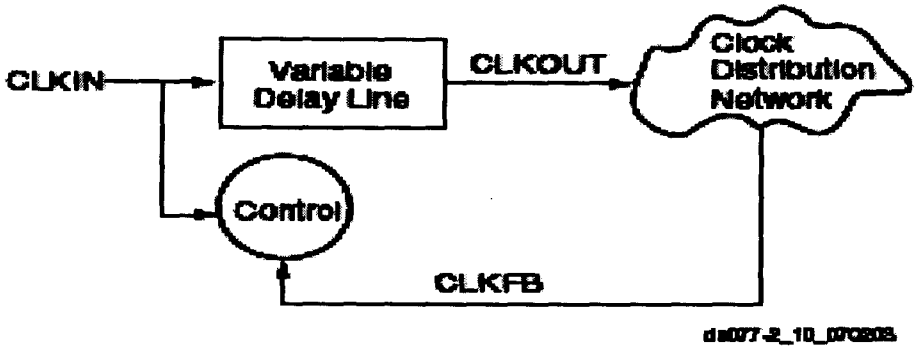


Fig. 1.5 Delay locked loop

Associated with each global clock input buffer is a fully digital Delay-Locked Loop (DLL) that can eliminate skew between the clock input pad and internal clock-input pins throughout the device. Each DLL can drive two global clock networks. The DLL monitors the input clock and the distributed clock, and automatically adjusts a clock delay element. Additional delay is introduced such that clock edges reach internal flip-flops exactly one clock period after they arrive at the input. This closed-loop system effectively eliminates clock-distribution delay by ensuring that clock edges arrive at internal flip-flops in synchronism with clock edges arriving at the input. In addition to eliminating clock-distribution delay, the DLL provides advanced control of multiple clock domains. The DLL provides four quadrature phases of the source clock, can double the clock, or divide the clock by 1.5, 2, 2.5, 3, 4, 5, 8, or 16.

1.4.4 Input /Output Block

The Spartan-IIE IOB, as seen in Figure 2, features inputs and outputs that support a wide variety of I/O signaling standards. These high-speed inputs and outputs are capable of supporting various state of the art memory and bus interfaces. The three IOB registers function either as edge-triggered D-type flip-flops or as level-sensitive latches. Each IOB has a clock signal (CLK) shared by the three registers and independent Clock Enable (CE) signals for each register.

In addition to the CLK and CE control signals, the three registers share a Set/Reset (SR). For each register, this signal can be independently configured as a synchronous Set, a synchronous Reset, an asynchronous Preset, or an asynchronous Clear.

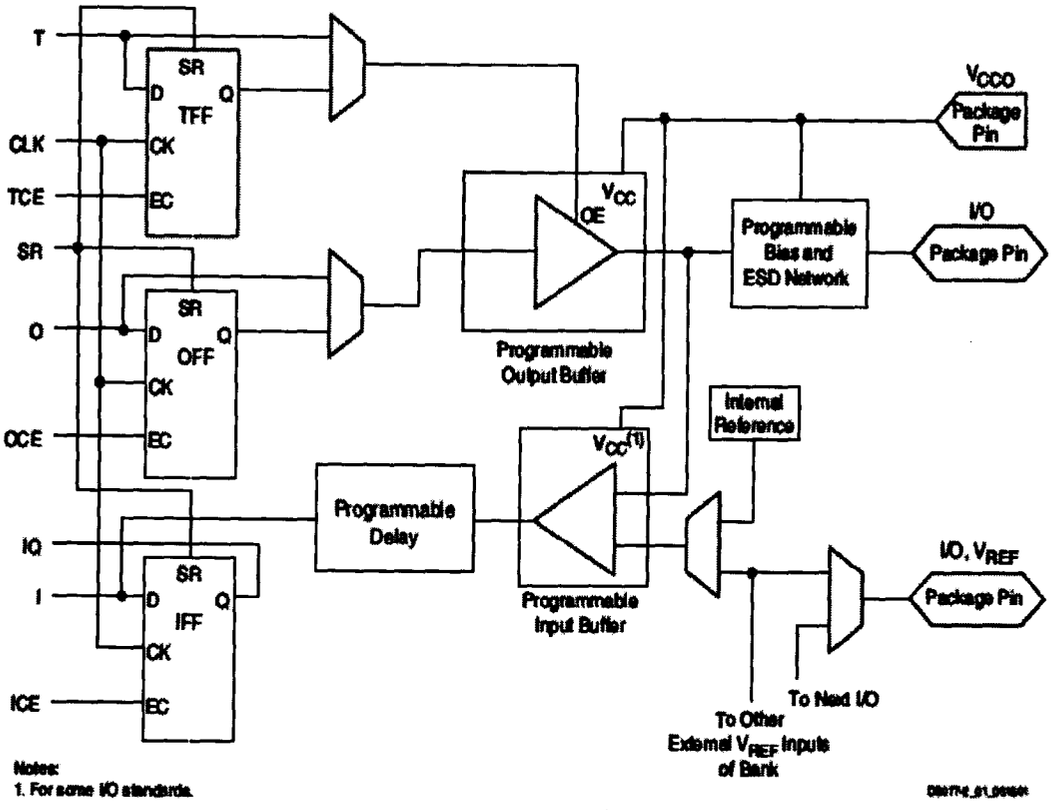


Fig.1.6 Spartan-IIE Input/Output Block (IOB)

All pads are protected against damage from electrostatic discharge (ESD) and from over- voltage transients. After configuration, clamping diodes are connected to VCCO for LVTTL, PCI, HSTL, SSTL, CTT, and AGP standards.

All Spartan-IIE IOBs support IEEE 1149.1-compatible boundary scan testing.

Input Path

A buffer in the Spartan-IIE IOB input path routes the input signal directly to internal logic and through an optional input flip-flop.

Each input buffer can be configured to conform to any of the low-voltage signaling standards supported. There are optional pull-up and pull-down resistors at each input for use after configuration.

Output Path

The output path includes a 3-state output buffer that drives the output signal onto the pad. The output signal can be routed to the buffer directly from the internal logic or through an optional IOB output flip-flop.

I/O Banking

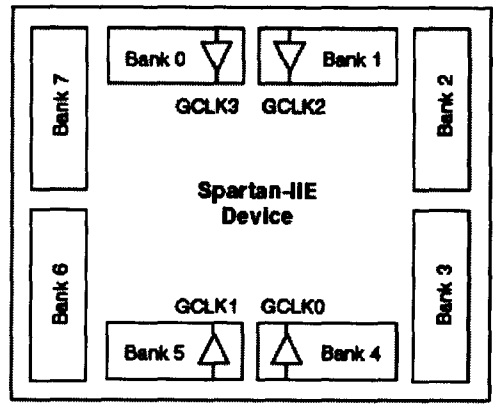


Fig.1.7 Spartan-IIE I/O Banks

Some of the I/O standards described above require VCCO and/or VREF voltages. These voltages are externally supplied and connected to device pins that serve groups of IOBs, called banks. Consequently, restrictions exist about which I/O standards can be combined within a given bank. Eight I/O banks result from separating each edge of the FPGA into two banks In the TQ144 and PQ208 packages, the eight banks have VCCO connected together. Thus, only one VCCO level is allowed in these packages, although different VREF values are allowed in each of the eight banks.

Boundary Scan

Spartan-IIE devices support all the mandatory boundary-scan instructions specified in the IEEE standard 1149.1.

The TAP uses dedicated package pins that always operate using LVTTL. For TDO to operate using LVTTL, the VCCO for Bank 2 must be 3.3V. Otherwise, TDO switches rail-to-rail between ground and VCCO. The boundary-scan input pins (TDI, TMS, TCK) do not have a VCCO requirement and operate with either 2.5V or 3.3V input signaling levels.

Development System

Spartan-IIE FPGAs are supported by the Xilinx ISE Foundation and Alliance CAE tools. The basic methodology for Spartan-IIE design consists of three interrelated steps: design entry, implementation, and verification. Industry-standard tools are used for

design entry and simulation, while Xilinx provides proprietary architecture-specific tools for implementation.

The Xilinx development system is integrated under the Xilinx Project Navigator software, providing designers with a common user interface regardless of their choice of entry and verification tools. The software simplifies the selection of implementation options with pull-down menus and on-line help. Application programs ranging from schematic capture to placement and routing can be accessed through the software. The program command sequence is generated prior to execution, and stored for documentation.

2. Complex programmable logic devices (CPLDs)

Complex programmable logic devices (CPLDs) are integrated circuits (ICs) or chips that application designers configure to implement digital hardware such as mobile phones. CPLDs can handle significantly larger designs than simple programmable logic devices (SPLDs), but provide less logic than field programmable gate arrays (FPGAs). CPLDs contain several logic blocks, each of which includes eight to 16 macro cells. Because each logic block performs a specific function, all of the macro cells within a logic block are fully connected. Depending upon the application, however, logic blocks may or may not be connected to one another.

Most complex programmable logic devices contain macro cells with a sum-of-product combinatorial logic function and an optional flip-flop. Depending on the CPLD, the combinatorial logic function supports from four to sixteen product terms with wide fan-in. Complex programmable logic devices also vary in terms of logic gates and shift registers. For this reason, CPLDs with a large number of logic gates may be used in place of FPGAs. Another CPLD specification denotes the number of product terms that a macro cell can manage. Product terms are the product of digital signals that perform a specific logic function.

2.1 Xilinx XC95144XL CPLD:

Description

The XC95144XL is a 3.3V CPLD targeted for high-performance, low-voltage applications in leading-edge communications and computing systems.

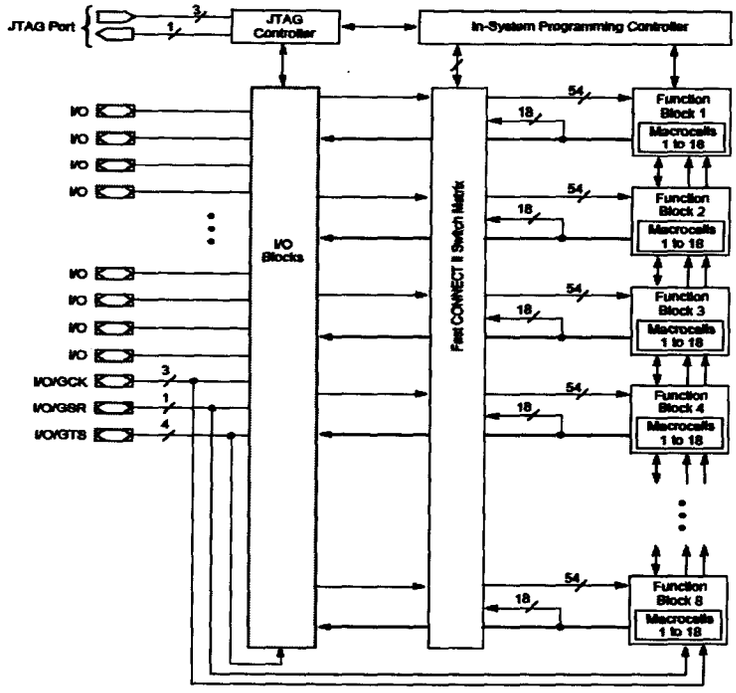


Fig.1.8 XC95144XL Architecture

Features

- 5 ns pin-to-pin logic delays
- System frequency up to 178 MHz
- 144 macrocells with 3,200 usable gates
- Available in small footprint packages
  - 100-pin TQFP (81 user I/O pins)
  - 144-pin TQFP (117 user I/O pins)
  - 144-CSP (117 user I/O pins)
- Advanced system features
  - In-system programmable
  - Full IEEE Standard 1149.1 boundary-scan (JTAG)
- Fast concurrent programming

3 Peripheral Component Interconnect (PCI)

Peripheral Component Interconnect is an interconnection system between a microprocessor and attached devices in which expansion slots are spaced closely for high-speed operation. It is a local bus that supports high-speed connection with peripherals. It plugs into a PCI slot on the motherboard.

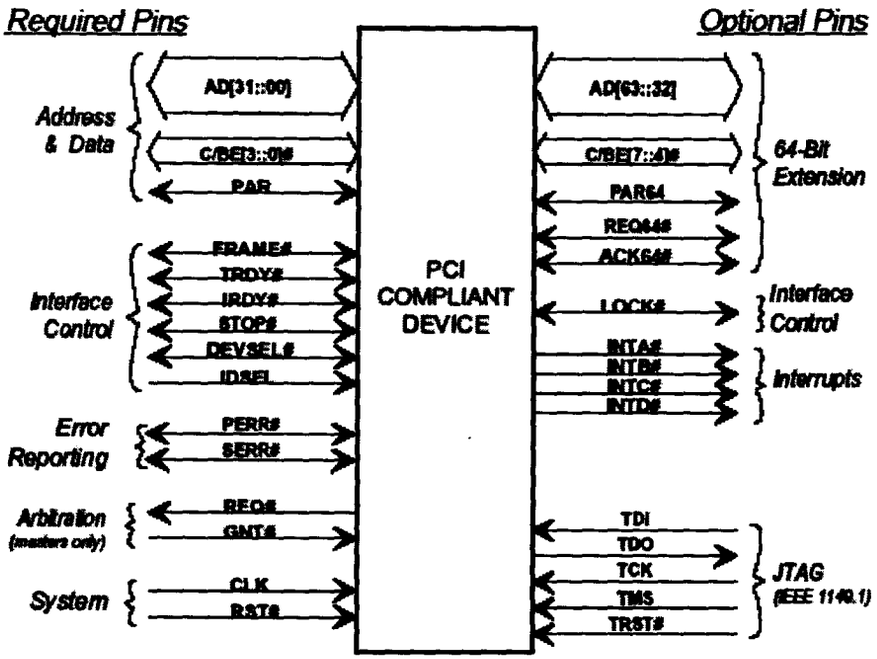


Fig.1.9 PCI pin list

Peripheral Component Interconnect, a local bus that supports high-speed connection with peripherals. It plugs into a PCI slot on the motherboard. The PCI Bus has been defined with the primary goal of establishing the industry standard, high performance local bus architecture that offers low cost and allows differentiation.

3.1 JTAG/Boundary Scan Pins for PCI

The IEEE standard 1149.1 *test access port* and *boundary scan architecture* specifies the rules and permission for designing an 1149.1-complient IC. Inclusion of a Test Access Port (TAP) on a device allows boundary scan to be used for testing of the device and board on which it is installed. The TAP is comprised of four pins that are used to interface serially with a TAP controller within the PCI device.

TCK in *Test Clock* is used to clock state information and test data into and out of the device during operation of the TAP.

- TDI - in - *Test Data Input* is used to serially shift test data and test instructions into the device during TAP operation.
- TDO – out - *Test Output* is used to serially shift test data and test instructions out of the device during TAP operation.
- TMS - in - *Test Mode Select* is used to control the state of the TAP controller in the device.
- TRST# - in - *Test Reset* provides an asynchronous initialization of the TAP controller. This signal is optional in IEEE Standard.

4 Serial EEPROM

NM93CS46L/CS56L/CS66L (2048-/4096-Bit Serial EEPROM)

The CS56L/CS66L devices are 2048/4096 bits, respectively, of non-volatile electrically erasable memory divided into 128/256 x 16-bit registers (addresses). The NM93CSxxL Family functions in an extended voltage operating range, and is fabricated using National Semiconductor's floating gate CMOS technology for high reliability, high endurance and low power consumption.

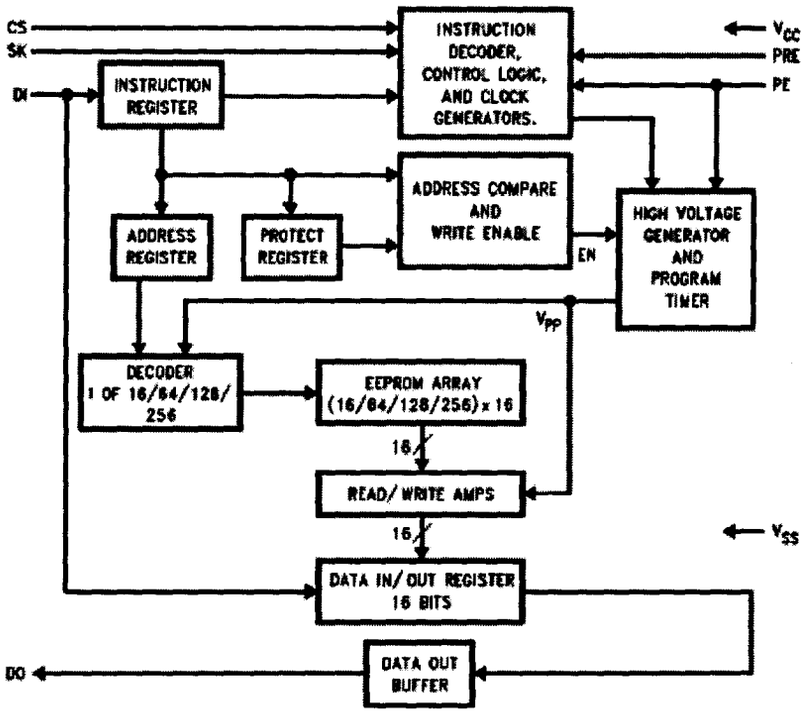
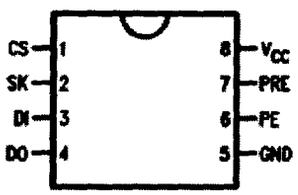


Fig.1.10 Block diagram of NM93CS56L/66L

Features

- Sequential register read
- Write protection in a user defined section of memory
- 2.7V to 5.5V operating range in all modes
- Typical active current of 200 mA; typical standby current of 1 mA
- No erase required before write



PIN Diagram

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
PE	Program Enable
PRE	Protect Register Enable
VCC	Power Supply

Fig.1.11 Pin diagram of NM93CSxxL

Functional Description

The extended voltage EEPROMs of the NM93CSxxL Family have 10 instructions as described below. Note that MSB of any instruction is a ``1" and is viewed as a start bit in the interface sequence. For the CS56 and CS66, the next 10 bits carry the opcode and the 8-bit address for register selection. All Data In signals are clocked into the device on the low-to-high SK transition.

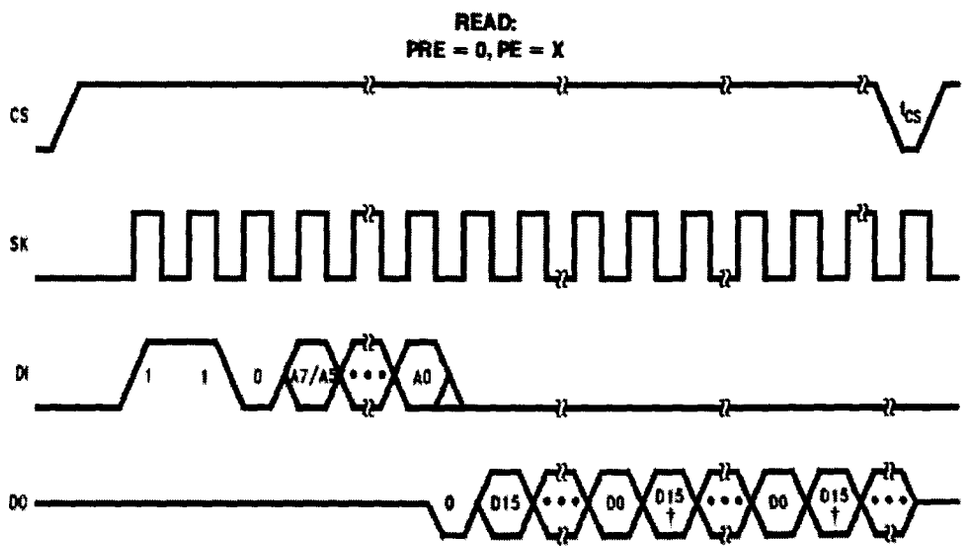


Fig.1.12 Timing Diagram for read operation

Instruction Set for the NM93CS56L and NM93CS66L							
Instruction	SB	Op Code	Address	Data	PRE	PE	Comments
READ	1	10	A7–A0		0	X	Reads data stored in memory, starting at specified address.
WEN	1	00	11XXXXXX		0	1	Enable all programming modes.
WRITE	1	01	A7–A0	D15–D0	0	1	Writes address if unprotected.
WRALL	1	00	01XXXXXX	D15–D0	0	1	Writes all registers. Valid only when Protect Register is cleared.
WDS	1	00	00XXXXXX		0	X	Disables all programming modes.
PRREAD	1	10	XXXXXXXX		1	X	Reads address stored in Protect Register.
PREN	1	00	11XXXXXX		1	1	Must immediately precede PRCLEAR, PRWRITE, and PRDS instructions.
PRCLEAR	1	11	11111111		1	1	Clears the "protect register" so that no registers are protected from WRITE.
PRWRITE	1	01	A7–A0		1	1	Programs address into Protect Register. Thereafter, memory addresses ≥ the address in Protect Register are protected from WRITE.
PRDS	1	00	00000000		1	1	ONE TIME ONLY instruction after which the address in the Protect Register cannot be altered.

Fig.1.13 Instruction set of EEPROM

5 JTAG Boundary Scan Interface

One of the difficult areas in the development of any modern hardware system is the production testing of the Printed Circuit Boards (PCBs). This is the problem addressed by the IEEE standard number 1149 "Standard Test Access Port and Boundary-Scan Architecture". This standard defines a 5-pin serial protocol for accessing and controlling the signal-levels on the pins of a digital circuit, and has some extensions for testing the internal circuitry on the chip itself (which will not be discussed here). The standard was written by the Joint Test Action Group (JTAG) and the architecture defined by it is known as "JTAG boundary scan" or as "IEEE 1149".

All the signals between the chip's core logic and the pins are intercepted by a serial scan path known as the "*Boundary Scan Register*" (*BSR*), and shown as cells "C0", "C1", "C2", "C3", and "C4" in the figure above. In normal system operation this path can transparently connect the core-logic signals to the pins and effectively become invisible. In external-test mode, it can disconnect the core-logic from the pins, drive the output pins ("Pin1", and "Pin2" in the figure above) by itself, and read and latch the states of the input pins (figure: "Pin0", and "Pin2"). In internal-test mode, it can disconnect the core-logic

from the pins, drive the core-logic input signals by it, and read and latch the states of the core-logic output signals.

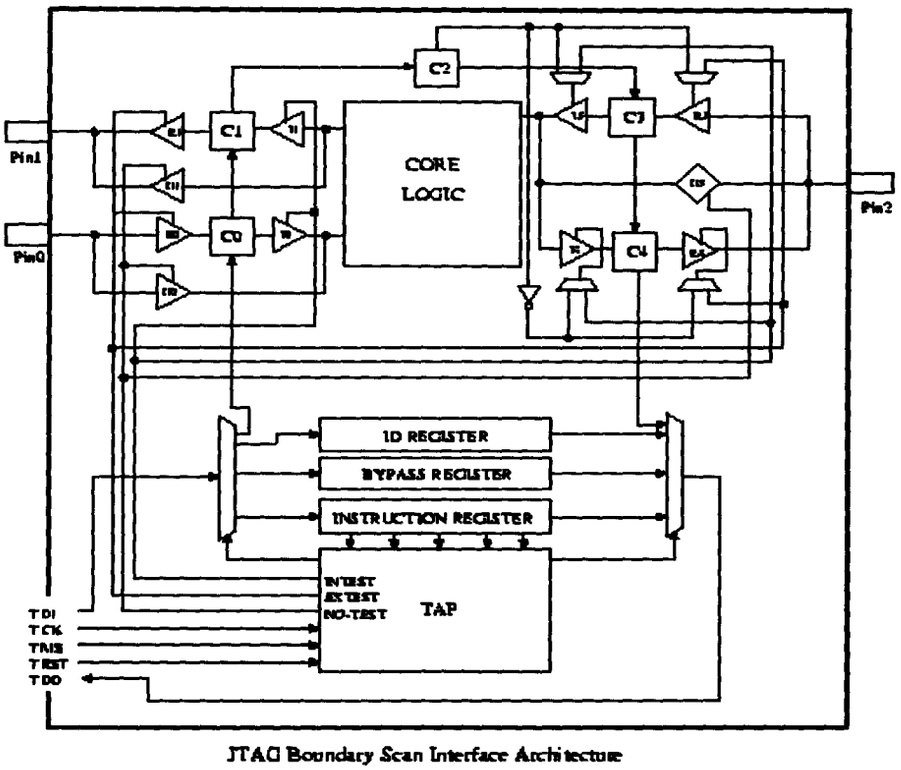


Fig.1.14 JTAG Boundary Scan Interface Architecture

In the figure above, and assuming that the JTAG interface is in external-test mode, C0 is the BSR cell capturing the state of the input pin 0. C1 is the BSR cell driving the output pin 1. C2 does not itself correspond to any specific pin, but it is the "enable" BSR cell that controls the "direction" of the bidirectional pin 2. C3 is the input BSR cell capturing the state of the bidirectional pin 2, and C4 is the output BSR cell driving the bidirectional pin 2. Summarizing we can identify three times of BSR cells:

Input Cells like C0, and C3. They are always associated with a specific pin whose state they capture when the JTAG interface is in external test mode.

Output Cells like C1, and C4. They are always associated with a specific pin, which they drive when the JTAG interface is in external test mode.

Enable Cells like C2. They are not associated with any pin per-se, but they either control the direction of bi-directional pins, or enable and disable certain input or output pins.

Gates E0, E3, and E4 operate under the control of the TAP (and probably also under the control of "enable" cells, like C2) and capture, or apply, the states (contents) of

the respective input, or output, cells to, or from, the chip's pins. The state capture, or application, takes place during certain transitions of the TAP state-machine, and only if the IR (instruction register) has been previously loaded with, and contains, the proper opcode (e.g. EXTEST).

Gates I0, I3, and I4 operate under the control of the TAP (and probably also under the control of "enable" cells, like C2) and capture, or apply, the states (contents) of the respective input, or output, cells to, or from, the chip's internal-logic signal lines. The capture, or application, takes place during certain transitions of the TAP state-machine, and only if the IR (instruction register) has been previously loaded with, and contains, the proper opcode (e.g. INTEST).

Gates N0, N1, and N3, come into operation only when the system is in normal-operation mode (i.e. when the JTAG test apparatus is inactive) and connect the chip's pins to the internal core-logic signals, as if the Boundary Scan Path was not present.

The contents of the BSR register can be written and read bit-after-bit, in a serial fashion, using the TDI and TDO JTAG signals. Actually the BSR "read" and "write" (set) operations take place at the same time, with the new "value" shifted in from TDI, while the previous value is shifted out from TDO. The same technique is used to read and write the values of the other JTAG registers too, by having the TAP controller connect them between the TDI and TDO pins, in place of the BSR.

Interface signals

The JTAG interface uses the following five dedicated signals, which must be provided on each chip that supports the standard:

TRST* is a Test-ReSeT input which initializes and disables the test interface.

TCK is the Test CLocK input, which controls the timing of the test interface independently from any system clocks. TCK is pulsed by the equipment controlling the test and not by the tested device. It can be pulsed at any frequency (up to a maximum of some MHz). It can be even pulsed at varying rates.

TMS is the Test Mode Select input, which controls the transitions of the test interface state machine.

TDI is the Test Data Input line, which supplies the data to the JTAG registers (Boundary Scan Register, Instruction Register, or other data registers).

TDO is the Test Data Output line, which is used to serially output the data from the JTAG registers to the equipment controlling the test. It carries the sampled values

Appendix B: Details of components in Signal Interface Board

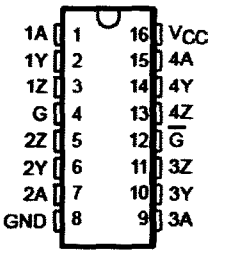
1. Differential line driver SN65LBC172 data sheets

SN65LBC172, SN75LBC172
QUADRUPLE LOW-POWER DIFFERENTIAL LINE DRIVER

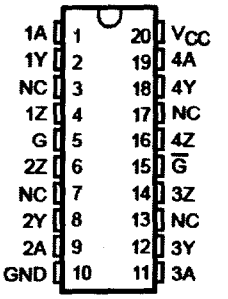
SLLS163B – JULY 1993 – REVISED JANUARY 2000

- **Meet or Exceed EIA Standard RS-485**
- **Designed for High-Speed Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **Support Data Rates up to and Exceeding Ten Million Transfers Per Second**
- **Common-Mode Output Voltage Range of –7 V to 12 V**
- **Positive- and Negative-Current Limiting**
- **Low Power Consumption . . . 1.5 mA Max (Output Disabled)**
- **Functionally Interchangeable With SN75172**

N PACKAGE
(TOP VIEW)



DW PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE
(each driver)

INPUT	ENABLES		OUTPUTS	
A	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

H = high level, L = low level,
X = irrelevant, Z = high impedance (off)

description

The SN65LBC172 and SN75LBC172 are monolithic quadruple differential line drivers with 3-state outputs. Both devices are designed to meet the requirements of EIA Standard RS-485. These devices are optimized for balanced multipoint bus transmission at data rates up to and exceeding 10 million bits per second. Each driver features wide positive and negative common-mode output voltage ranges, current limiting, and thermal-shutdown circuitry making it suitable for party-line applications in noisy environments. Both devices are designed using LinBiCMOS™, facilitating ultra-low power consumption and inherent robustness.

Both the SN65LBC172 and SN75LBC172 provide positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. These devices offer optimum performance when used with the SN75LBC173 or SN75LBC175 quadruple line receivers. The SN65LBC172 and SN75LBC172 are available in the 16-pin DIP package (N) and the 20-pin wide-body small-outline inline-circuit (SOIC) package (DW).

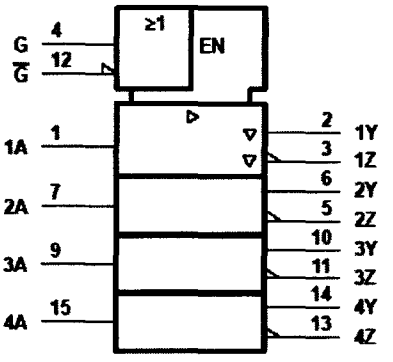
The SN75LBC172 is characterized for operation over the commercial temperature range of 0°C to 70°C. The SN65LBC172 is characterized over the industrial temperature range of –40°C to 85°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN65LBC172, SN75LBC172
QUADRUPLE LOW-POWER DIFFERENTIAL LINE DRIVER

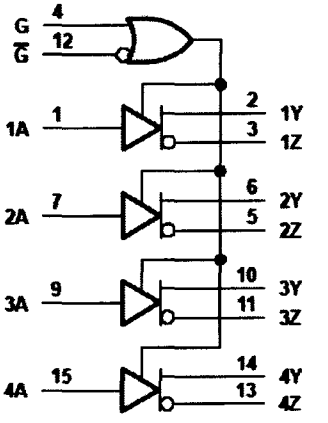
SLLS163B – JULY 1993 – REVISED JANUARY 2000

logic symbol†

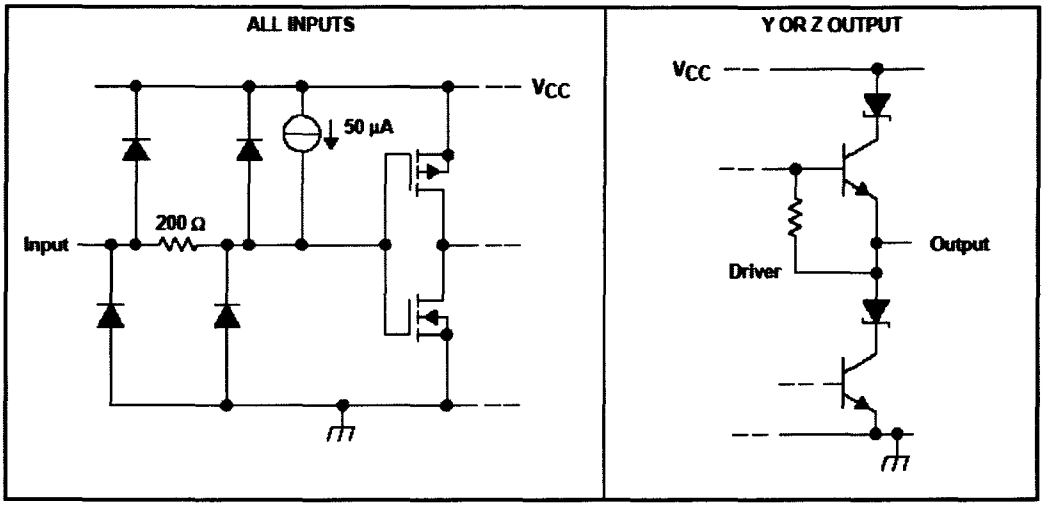


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the N package.

logic diagram (positive logic)



schematic diagrams of inputs and outputs



TEXAS INSTRUMENTS
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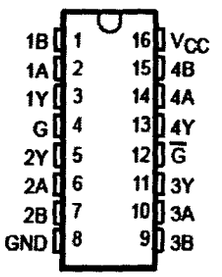
2. Differential line receiver SN65LBC173 data sheets

SN65LBC173, SN75LBC173
QUADRUPLE LOW-POWER DIFFERENTIAL LINE RECEIVERS

SLLS170C – OCTOBER 1993 – REVISED JANUARY 2000

- **Meets or Exceeds the Requirements of ANSI Standards EIA/TIA-422-B, EIA/TIA-423-B, RS-485, and ITU Recommendations V.10 and V.11.**
- **Designed to Operate With Pulse Durations as Short as 20 ns**
- **Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments**
- **Input Sensitivity . . . ±200 mV**
- **Low-Power Consumption . . . 20 mA Max**
- **Open-Circuit Fail-Safe Design**
- **Pin Compatible With SN75173 and AM26LS32**

D OR N PACKAGE
(TOP VIEW)



description

The SN65LBC173 and SN75LBC173 are monolithic quadruple differential line receivers with 3-state outputs. Both are designed to meet the requirements of the ANSI standards EIA/TIA-422-B, EIA/TIA-423-B, RS-485, and ITU Recommendations V.10 and V.11. The devices are optimized for balanced multipoint bus transmission at data rates up to and exceeding 10 million bits per second. The four receivers share two ORed enable inputs, one active when high, the other active when low.

Each receiver features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 mV over a common-mode input voltage range of 12 V to –7 V. Fail-safe design ensures that if the inputs are open circuited, the output is always high. Both devices are designed using the Texas Instruments proprietary LinBiCMOS™ technology that provides low power consumption, high switching speeds, and robustness.

These devices offer optimum performance when used with the SN75LBC172 or SN75LBC174 quadruple line drivers. The SN65LBC173 and SN75LBC173 are available in the 16-pin DIP (N) and SOIC (D) packages.

The SN65LBC173 is characterized over the industrial temperature range of –40°C to 85°C. The SN75LBC173 is characterized for operation over the commercial temperature range of 0°C to 70°C.

FUNCTION TABLE
(each receiver)

DIFFERENTIAL INPUTS A–B	ENABLES G	ENABLES $\overline{G}$	OUTPUT Y
$V_{ID} \geq 0.2$ V	H	X	H
	X	L	H
$-0.2\text{ V} < V_{ID} < 0.2$ V	H	X	?
	X	L	?
$V_{ID} \leq -0.2$ V	H	X	L
	X	L	L
X	L	H	Z
Open Circuit	H	X	H
	X	L	H

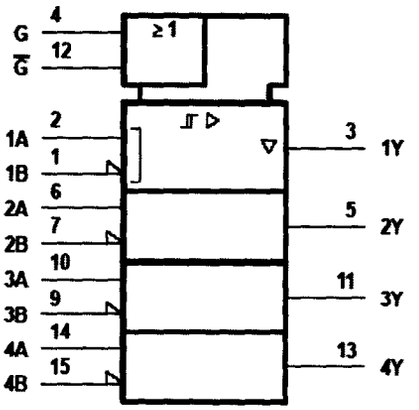
H = high level, L = low level, X = irrelevant,
Z = high impedance (off), ? = indeterminate

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN65LBC173, SN75LBC173
QUADRUPLE LOW-POWER DIFFERENTIAL LINE RECEIVERS

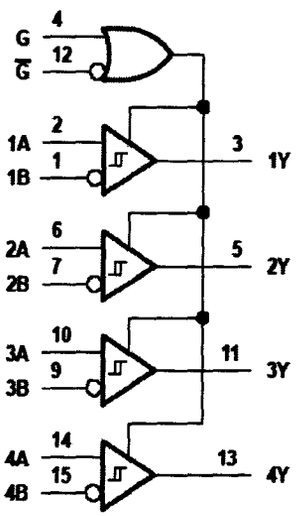
SLLS170C – OCTOBER 1993 – REVISED JANUARY 2000

logic symbol†

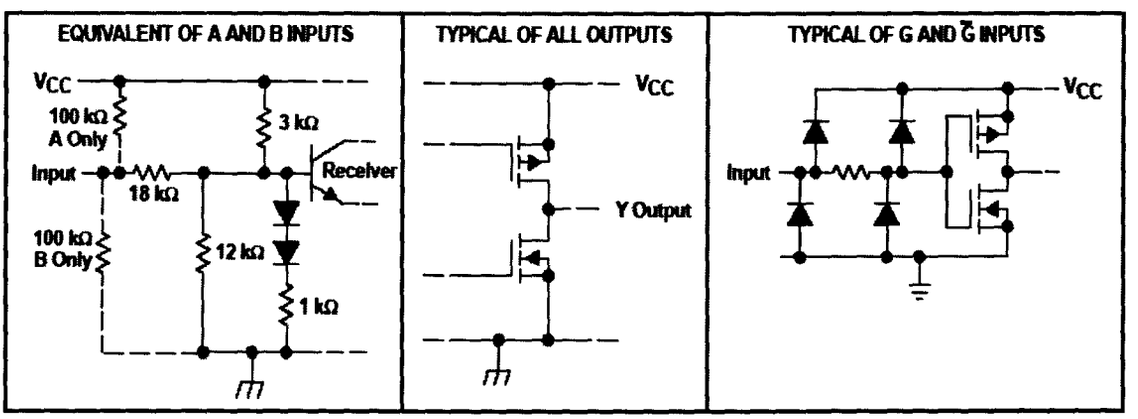


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



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Appendix C: Details of PCI 9054

1.PCI 9054 data sheets

PCI 9054

PCI I/O Accelerator

I_2O Compatible, CompactPCI Hot Swap Friendly
PCI Bus Master Interface Chip
for Adapters and Embedded Systems

January 2000
Version 2.1

1 INTRODUCTION

1.1 FEATURES

- PCI Specification version 2.2 (v2.2) compliant 32-bit, 33-MHz Bus Master Interface Controller with PCI Power Management features for adapters and embedded systems
- General Purpose Bus Master Interface featuring advanced Data Pipe Architecture™ technology, which includes two DMA engines, programmable Target and Initiator Data Transfer modes and PCI messaging functions
- PCI v2.2 Vital Product Data (VPD) configuration support
- PCI Dual Address Cycle (DAC) support
- PCI Hot Plug and CompactPCI Hot Swap compliant
- I_2O™ v1.5-Ready Messaging Unit
- Two independent DMA channels for Local Bus memory to and from PCI Host Bus Data transfers
- Supports Type 0 and Type 1 Configuration cycles
- Programmable Burst Management
- Programmable Interrupt Generator
- Six programmable FIFOs for zero wait state burst operation
- PCI ↔ Local Data transfers up to 132 MB/s
- 3.3V, 5V tolerant PCI and Local signaling supports Universal PCI Adapter designs, 3.3V core, low-power CMOS in 176-pin PQFP and 225-pin PBGA
- Supports Local Bus Direct-Connect to the Motorola® MPC850 or MPC860 PowerQUICC™, Intel® i960 family and IBM® PPC401 CPUs and similar bus protocol devices
- Programmable Local Bus runs up to 50 MHz and supports non-multiplexed 32-bit address/data, multiplexed 32-bit, and slave accesses of 8-, 16-, or 32-bit Local Bus devices
- Serial EEPROM interface
- Three PCI-to-Local Address spaces
- Programmable Local Bus wait states
- Programmable prefetch counter
- Local Bus runs asynchronously to the PCI Bus
- Eight 32-bit Mailbox and two 32-bit Doorbell registers
- Performs Big Endian ↔ Little Endian conversion
- PCI-to-Local Delayed Read mode
- Local-to-PCI Deferred Read mode (M mode only)
- Flexible 3.3V, 5V Tolerant Local Bus operation up to 50 MHz
- Industrial Temp Range operation

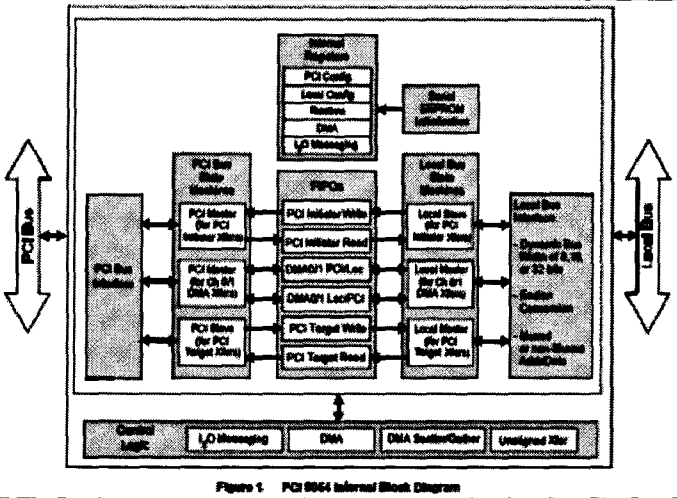

Figure 1. PCI 9054 Internal Block Diagram

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- "10.4-meter radio telescope control system user manual", telescope observatory, RRI.
- "PLX PCI 9054 user manual", digital signal processing lab, RRI.
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