Low Power LCD with Low Supply Voltage

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ABSTRACT

Low power dissipation and low voltage operation are achieved by combining the best features of several addressing techniques. A large number of gray shades are displayed with simple drivers and controller to reduce cost.

1. INTRODUCTION

Low power consumption, low voltage operation, capability to display a large number of gray shades without flicker, low hardware complexity of circuit in drivers, cross talk free images and full utilization of the standard drivers are some important attributes of a well designed display. Methods to achieve these goals are discussed in this paper.

2. TECHNIQUE

Hardware complexity of drivers is low (is almost same as that of bi-level displays) for the successive approximation technique (SAT) [1]. A large number of gray shades can be displayed without flicker by using SAT and low power can be achieved by modifying the waveforms as proposed in IDRC'08 [2]. Supply voltage is high for SAT that is based on line-by-line addressing. SAT can also be combined with Multi-line addressing (MLA) to reduce the supply voltage [3]. Either the hardware utilization of column drivers is poor or the address generation in the controller to fetch the image from the buffer memory is complex when MLA is used. MLA based on sparse matrices [4] can be used to achieve full utilization of the circuit in the standard column drivers that can apply one-of-eight voltages to column electrodes. A sparse orthogonal matrix of order 8 shown in equation (1) is chosen for this purpose.

$$\begin{bmatrix} +V_r & +V_r & +V_r & +V_r & +V_r & +V_r & +V_r & 0 \\ +V_r & 0 & +V_r & +V_r & -V_r & -V_r & -V_r & -V_r \\ +V_r & +V_r & 0 & -V_r & -V_r & -V_r & +V_r & +V_r \\ +V_r & +V_r & -V_r & -V_r & +V_r & 0 & -V_r & -V_r \\ +V_r & -V_r & -V_r & +V_r & +V_r & -V_r & 0 & +V_r \\ +V_r & -V_r & -V_r & 0 & -V_r & +V_r & +V_r & -V_r \\ +V_r & -V_r & +V_r & -V_r & 0 & +V_r & -V_r & +V_r \\ 0 & -V_r & +V_r & -V_r & +V_r & -V_r & +V_r & -V_r \end{bmatrix} \quad (1)$$

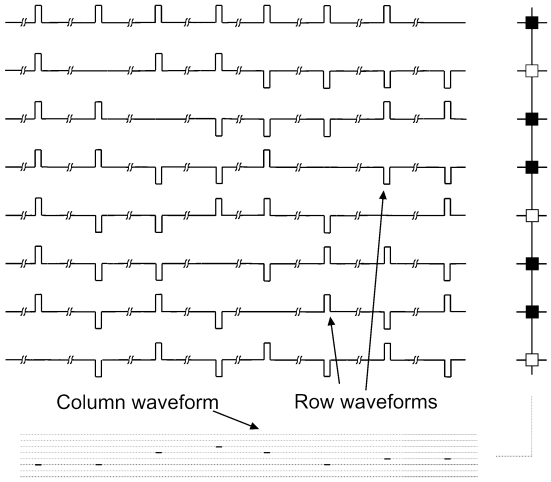

Fig. 1 Waveforms of MLA that are based on sparse matrix in equation (1) with distributed select pulses.

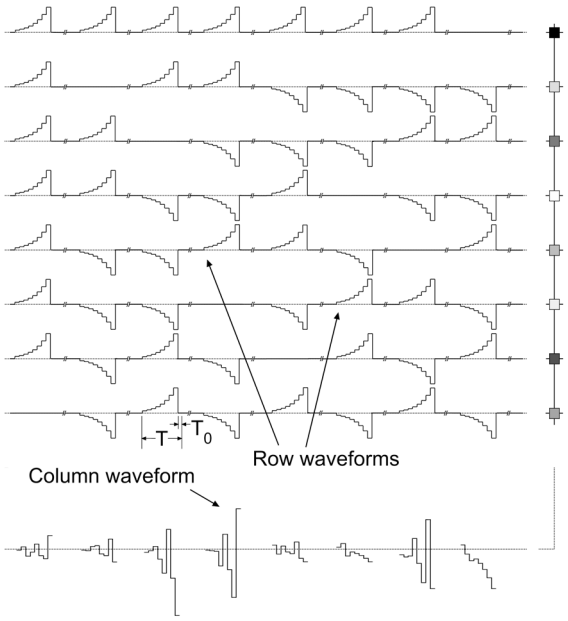

Fig. 2 Each pulse in Figure 1 is substituted with discrete version of ramp waveform to display a large number of gray shades by using SAT and to reduce power dissipation in row drivers.

Distributed select pulses are useful to suppress frame response [5] and flicker. Typical waveforms of distributed select pulses for displaying bi-level images is shown in Figure 1. Low power

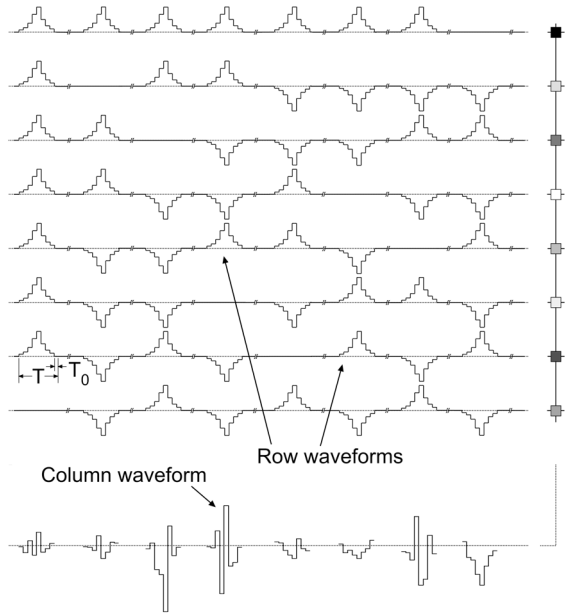

Fig. 3 Each pulse in Figure 1 is substituted with discrete version of triangular waveform to reduce power dissipation in drivers when a large number of gray shades are displayed using SAT.

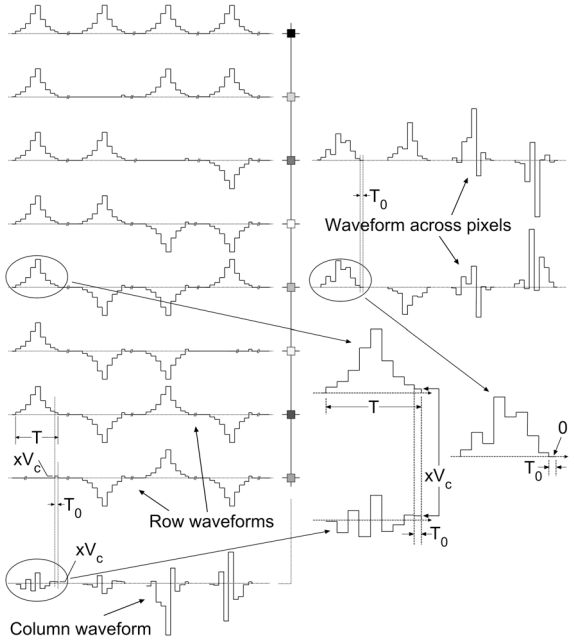

Fig. 4 One of the eight data voltages is introduced as the fourth voltage in the row waveform and the same voltage is applied to all columns to achieve zero voltage across all pixels during the 'dead time (T_0)' to achieve full utilization of hardware in the row and column drivers.

consumption can be achieved by adapting multi-step waveform profiles of reference [2], [6] as shown in Figures 2 and 3. Voltage across all pixels is brought to zero during the dead time (T_0), to avoid brightness non-uniformity arising from distortion in the addressing waveforms due to large time constant. The multi-step waveform profile that is obtained by arranging the select pulses of alternate bits so that resulting waveform has ascending and descending steps (discrete version of triangular waveform) is useful to reduce power dissipation [6]. These profiles are universal in the sense that it can be combined with any addressing technique [2]. We have adopted the same waveform here for the multi-line addressing. The multi-step waveform profile in Figure 3 is more efficient than that in Figure 2 and achieves lower power consumption [6]. Duty cycle control [7] is useful to reduce cross talk among pixels when the time constant of driver circuit is large. However, addition of one more voltage in the column waveform will increase the number of voltages to 9 and the standard drivers cannot be used. Hardware utilization will be poor even in case one opts for custom designed drivers. A sparse orthogonal matrix of equation (2) with six non-zero elements in each column could be used but the reduction in supply voltage will be better (for large matrices; N>49) with sparse matrix of equation (1) that has seven non-zero elements in each column.

$$\begin{bmatrix} 0 & +V_r & +V_r & +V_r & 0 & +V_r & +V_r & +V_r \\ +V_r & +V_r & -V_r & 0 & +V_r & +V_r & -V_r & 0 \\ +V_r & -V_r & 0 & +V_r & +V_r & -V_r & 0 & +V_r \\ +V_r & 0 & +V_r & -V_r & +V_r & 0 & +V_r & -V_r \\ 0 & +V_r & +V_r & +V_r & 0 & -V_r & -V_r & -V_r \\ +V_r & +V_r & -V_r & 0 & -V_r & -V_r & +V_r & 0 \\ +V_r & -V_r & 0 & +V_r & -V_r & +V_r & 0 & -V_r \\ +V_r & 0 & +V_r & -V_r & -V_r & 0 & -V_r & +V_r \end{bmatrix} \quad (2)$$

Hardware utilization of row drivers is poor in all the multi-line addressing techniques because there are three voltages in the row waveform and an additional voltage can be easily incorporated without increasing the hardware complexity. Three level voltage drivers will have 2-bit shift register and 2-bit latch in each stage (row in the display). The shift registers and latches will be better utilized to select one-of-four voltages than one-of-three voltages. We have solved this problem by modifying the addressing waveforms and have achieved full utilization of both row and column drivers by introducing one of the data (column) voltages as an additional voltage in the row waveform and the same voltage is applied to the columns to achieve zero voltage across all pixels ('dead time') as shown in Figure 4. Any one of the data voltages (say 'xV_c') can be applied to all the rows and columns of the display and the difference will be zero. No additional voltages have to be accommodated in the data drivers and the sparse matrices with seven non-zero elements in each column can be used to drive the display. Such an improvement is significant because the number of column drivers is large and is equal to

Table 1 Comparison of average power dissipation in the drivers.

Number of gray shades	Ratio of average power dissipation of discrete ramp based waveform to that of SAT with distributed pulses (in %)	Ratio of average power dissipation of discrete triangular based waveform to that of SAT with distributed pulses (in %)
4	76.43	-
8	69.70	65.51
16	67.00	61.14
32	65.79	59.17
64	65.21	58.23
128	64.92	57.77
256	64.78	57.54

the number of columns in the display. Reduction in power dissipation is about the same as that of the select waveforms in Figure 3. Average power dissipation of successive approximation technique with discrete versions of ramp and triangular select waveforms are compared with that of distributed waveform of SAT in Table 1. It is important to note that the reduction in power dissipation is more for large number of gray shades. Supply voltage of the driver circuit is equal to that of SAT based MLA wherein 7 rows are selected simultaneously [3] when sparse matrix of order eight is used to scan the display. The technique is demonstrated with a 32x32 matrix LCD. Details of implementation are discussed in the following section.

3. IMPLEMENTATION

The technique is demonstrated with a 32x32 matrix LCD by displaying 256 gray shades. The controller has been implemented with simple binary counter and Look-up Tables on a Complex Programmable Logic Device (CPLD) (XCR3256XL), by utilizing about 96 macro cells that includes 63 registers and 255 product terms. Photograph of the prototype is shown in Figure 5. Typical addressing waveforms are shown in Figure 6. Some additional details of hardware are as follows:

Hadamard, Walsh, and diagonal matrices of order 8 are stored in the form of a Look-Up Table (LUT) and the second LUT contains the mask elements to introduce zeros to obtain the sparse matrices. The combined out of the two LUTs is used as data for the row drivers and to generate the column signal. Ex-OR gates are used to compare the sign of elements of rows in a column of the orthogonal matrix with corresponding data bits and a counter is used to obtain the column signal.

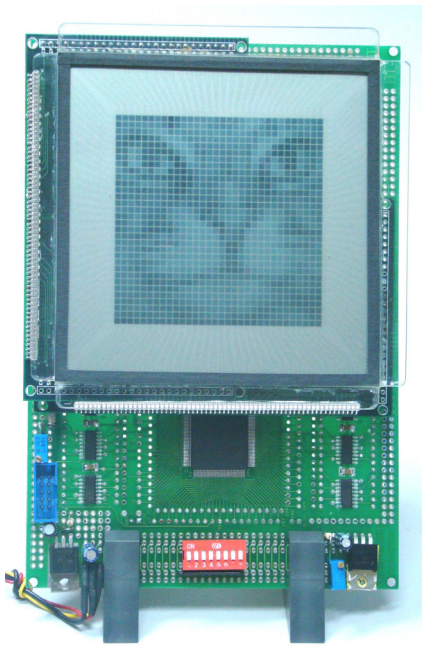

Fig. 5 Photograph of the prototype capable of displaying 256 gray shades with low supply voltage and low power dissipation.

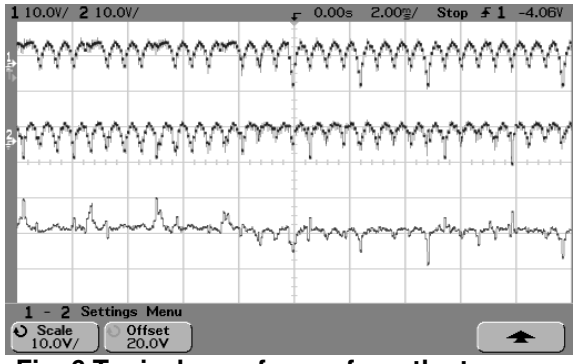

Fig. 6 Typical waveforms, from the top: row waveform, column waveform, and the waveform across a pixel in that order.

Image is stored in a bit-mapped memory (BMM). A binary counter is used in generating the control signals and addresses. Lower order 3 bits of the counter are used as row address of LUT and BMM; the next 5 bits are used as column address of BMM. Eight time intervals are necessary to select each subgroup to display 256 gray shades and a 3-bit counter is used for this purpose. An eight-bit counter is used to control the duration of dead time. It is controlled in 256 steps and the maximum duration could be equal to the duration of one select pulse. Two of higher order bits are used to select one of the four subgroups and 3-bits are used to choose the select vectors (columns of sparse matrix). Polarity reversal for DC free operation is done at the end of one frame. Two voltage level generators are used alternately to stabilize the voltages that are fed to the drivers as in reference [8].

Table 2 Response times (ms) when pixels are switched from one gray shade to another.

Gray data	0	31	63	95	127	159	191	223	255
0	X	68	70	66	65	63	60	60	60
31	74	X	70	65	64	62	63	63	61
63	74	69	X	65	63	64	64	62	61
95	70	65	66	X	60	64	63	63	60
127	67	68	64	60	X	50	57	62	56
159	68	66	64	64	55	X	49	58	55
191	65	65	62	61	63	53	X	48	50
223	62	64	60	61	60	62	50	X	48
255	64	59	59	58	59	58	58	45	X

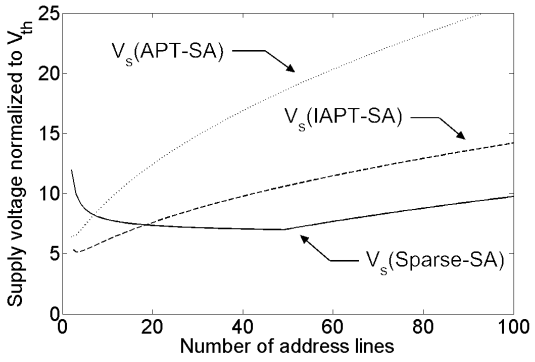

Fig. 7 Plot of normalized supply voltage.

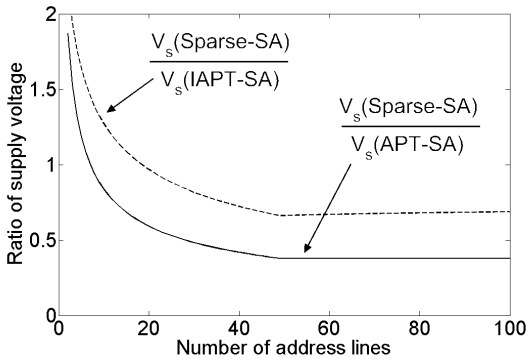

Fig. 8 Ratios of supply voltage showing the reduction in supply voltage of the technique.

4. RESULTS

Power dissipation in the analog part of drivers is reduced by 42% when 256 gray shades are displayed by using discrete version of triangular waveform. Switching times, i.e. the time taken to switch from one gray scale to another were measured using a twisted nematic cell filled with liquid crystal mixture: RO TN 623 and the response times are shown in Table 2. The cell thickness is 5.6 μm and the threshold voltage is 1.66 Volt; the cell is not optimized for short response times but it is important to note that the spread in response times is not high (standard deviation of 5.8 about the mean of 61ms). Note that the values above the diagonal are the rise times and values below the diagonal are fall times. Supply voltage of this technique is compared with that of SAT based on line-by-line addressing in Figures 7 and 8. It is lower by 62% (when the number of lines multiplexed is greater than 49) as compared to successive approximation technique that is based on line-by-line addressing (APT-SA). About 32% reduction in supply voltage is achieved as compared to the successive approximation based on line-by-line addressing and improved Alt and Pleshko technique (IAPT- SA).

5. IMPACT

Reduction in power dissipation (42% reduction for 256 gray shades), low supply voltage (32% reduction in supply voltage), low hardware complexity of drivers, efficient utilization of hardware in the row as well as column drivers, simple controller make it very attractive for portable devices viz. mobile phones, personal digital assistant (PDA), digital cameras etc where in low power consumption is essential.

6. REFERENCES

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