
Chapter 4

4. Displaying Gray Shades In Passive Matrix LCDs

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Displaying Gray Shades In Passive Matrix LCDs

4.1. Introduction

In LCDs gray shades are displayed by varying the rms voltage across the pixel between the threshold and saturation voltage levels. The existing techniques for displaying gray shades in passive matrix LCDs were reviewed in chapter 2 (section 2.7). Successive approximation technique to display gray shades using multi-line addressing is discussed in this chapter.

4.2. Approach

A successive approximation analog-to-digital converter (ADC) uses a digital-to-analog converter (DAC) and a comparator to perform binary search to find a digital value, which is approximately equal to the input voltage. The search tree starts with most significant bit (MSB) and ends with least significant bit (LSB). In successive approximation ADC, g comparisons are necessary in the binary search to achieve a g -bit resolution. For example, Figure 4-1 shows the binary search tree used in successive approximation ADC.

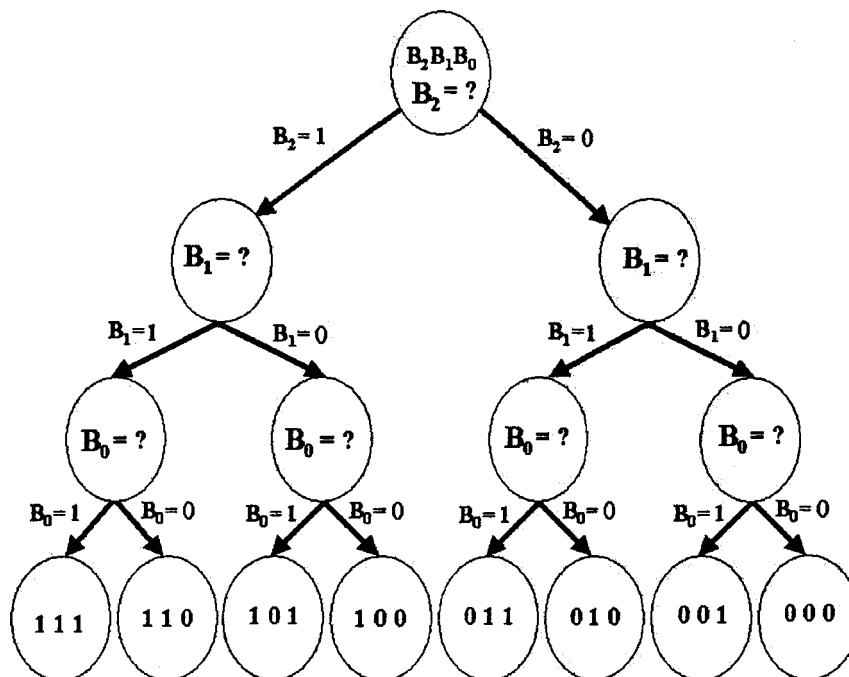


Figure 4-1 Binary search tree used in successive approximation approach ADC.

A similar approach is used for displaying gray shades in matrix LCDs as explained in the following text. To display 2^g gray shades, g frames are used and in each frame both row and column voltages are multiplied by a factor $\kappa_f (= \sqrt{2^f})$. Wherein f corresponds to f^{th} bit and ranges from $0 \dots (g - 1)$. One of the 2^g gray shades is displayed using g successive frames by modulating the amplitude of the row and column waveforms. In each frame the data is considered to be +1 or -1 for logic 0 or logic 1 respectively of the gray shade bit used for scanning the frame as shown in Figure 4-2. Here, three bits are used to represent each pixel and are mapped into three bi-level images as shown in the figure. In this case, 8 gray shades can be displayed using the three frames. Technique for displaying gray shades based on successive approximation using multi-line addressing is discussed in the next section.

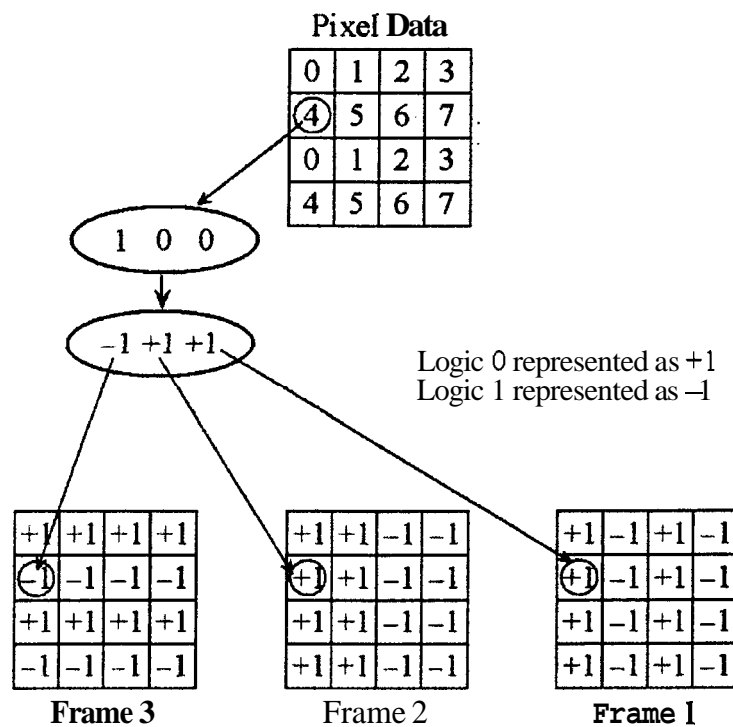


Figure 4-2 Pixel gray shade data

4.3. Technique

The multi-line addressing technique reviewed in chapter 2 (section 2.5.2) is modified to display gray shades based on the principle of successive approximation as described here.

The N rows in the matrix are divided into $\left(\frac{N}{s}\right)$ non-intersecting subgroups, with each subgroup consisting of s rows. A subgroup is selected at a time while the rows in the unselected subgroups are grounded. Here, g frames are necessary to display 2^g gray shades. Gray shade value of a pixel may be represented by

$$\sum_{f=0}^{g-1} d_f 2^f \quad (4.1)$$

The data to be displayed in each frame in the selected subgroup in any column is represented as $d_{f,ks+i}$. This is f^{th} bit of the i^{th} pixel in the k^{th} subgroup, wherein f ranges from 0 to $(g-1)$. The value of k ranges from 0 to $\left(\frac{N}{s}-1\right)$ and corresponds to the selected subgroup. The data $d_{f,ks+i} = -1$ or $+1$ corresponds to logic 1 or logic 0 respectively. The amplitude of the row voltage is $\kappa_f V_r$ instead of V_r . Column voltage is the dot product of the row select pattern and the data vector (see equation 2.21). This can be mathematically represented as

$$C_{f,k}(j) = \sum_{i=1}^s O(i,j) d_{f,ks+i} \quad (4.2)$$

where $C_{f,k}(j)$ is the column voltage (normalized to V_c) of the f^{th} frame which corresponds to j^{th} row select pattern for the k^{th} subgroup and $O(i,j)$ is the element of the orthogonal matrix. The column voltages are multiplied by κ_f which corresponds to the bit f of the gray shade data for the f^{th} frame. Both the row and column voltages are applied simultaneously to the matrix display for a time duration τ . A frame is complete when all the subgroups are selected with all the row select patterns once. The entire process is repeated using another bit of the gray shade data with the corresponding multiplication factor κ_f for the row and column voltages. A cycle consists of g frames corresponding to

the g bits of the gray shade data. The display is refreshed continuously with a frame frequency high enough to avoid any flicker. The rms voltage across the pixel is independent of the sequence in which the bits are selected in g frames. The scanning of the sequence in which row select patterns are selected while scanning the matrix can be done in a number of ways as discussed for multi-line addressing in chapter 2. The subgroup may be selected with all the row select pattern once before selecting another subgroup. The typical addressing waveforms with $s = 3$ are shown in Figure 4-3.

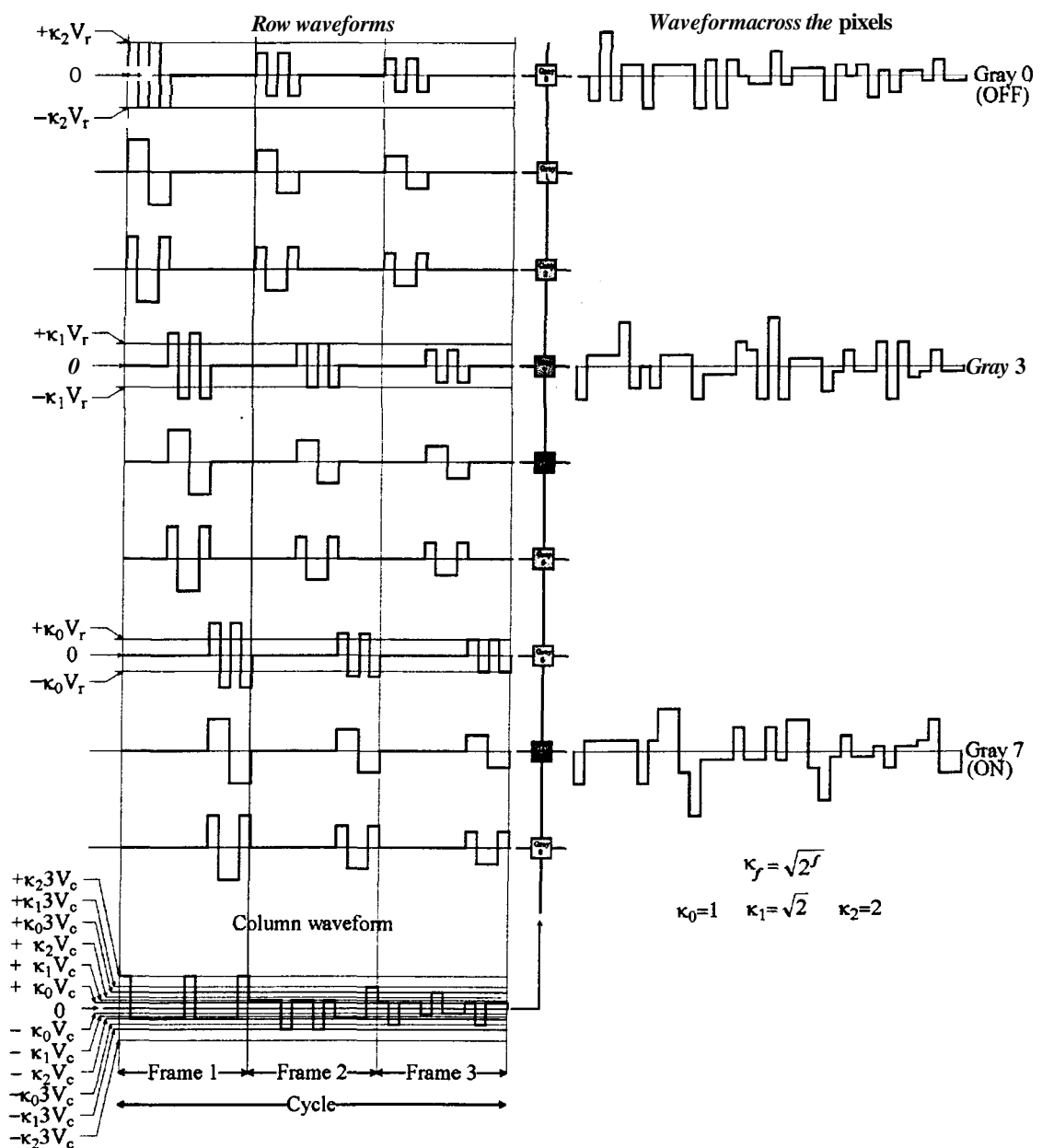


Figure 4-3 Typical addressing waveform of successive approximation based on MLA by selecting three rows at a time for displaying eight gray shades using three frames.

In fast-responding LCDs transmission of OFF pixels increases due to clustering of large amplitude row select pulses. This may lead to the *frame response phenomenon* (see section 2.4.6). In order to suppress the frame response, all the subgroups in the matrix LCD may be selected with one row select pattern once before changing to another row select pattern. Good brightness uniformity of the pixel can be obtained by changing the row select pattern whenever a new subgroup is selected as discussed in chapter 2. The typical addressing waveforms are shown in Figure 4-4.

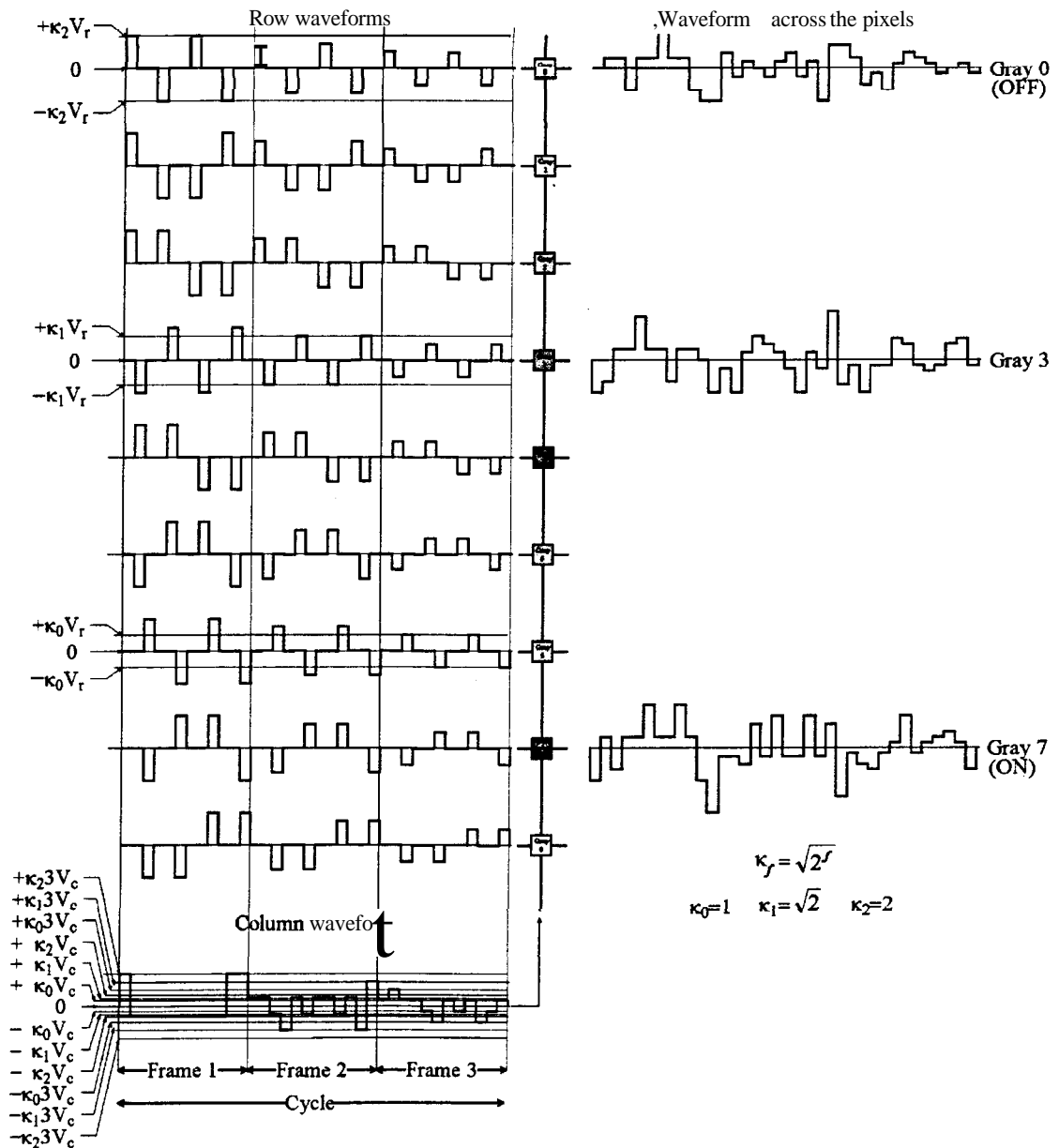


Figure 4-4 Typical addressing waveform of successive approximation based on MLA by selecting three rows at a time for displaying eight gray shades while row select pulses are distributed in each frame.

In multi-line addressing technique the number of voltage levels in the row and column waveforms are three and $(s+1)$ respectively. Where, s is the number of rows in each subgroup. Amplitudes of both row and column waveforms are modified by a factor $k_f = \sqrt{2^f}$, $0 \leq f \leq (g-1)$ in g frames. The number of voltage levels in any one frame is same as that of multi-line addressing technique. The voltages necessary for row and column waveforms for the g frames are generated in voltage level generators (VLGs). Analog multiplexers are used to select the voltages corresponding to each frame. These multiplexers are common to the both row and column drivers as shown in the Figure 4-5. Hence, the row and column drivers that are used in multi-line addressing to display bi-level images can be used for displaying gray shades using successive approximation technique.

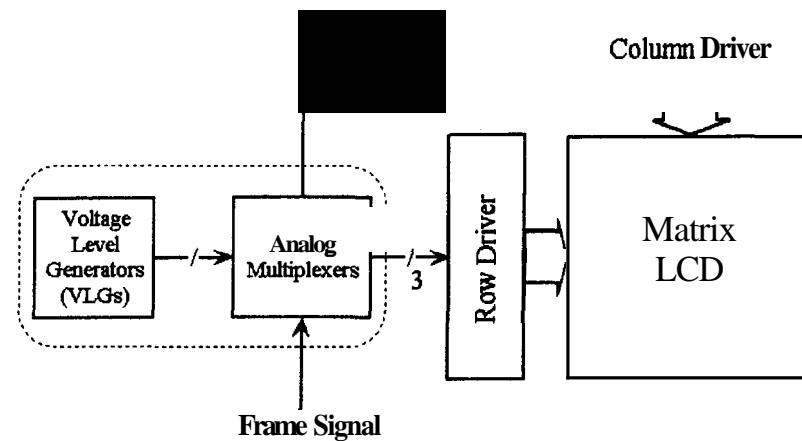


Figure 4-5 Block diagram row and column driver requirement for displaying gray shades using successive approximation.

The detailed analysis of the successive approximation using multi-line addressing technique for displaying gray shades is discussed in the next section.

4.4. Analysis

A subgroup is selected with voltages corresponding to one of the row select pattern. The voltages are $+V_r$ and $-V_r$, corresponding to $+1$ or -1 . The row voltage is zero during the $\left(\frac{N}{s} - 1\right)$ time intervals. The column voltage is the dot product of the row select pattern and the data vector, which is given by

$$C_{f,k}(j) = \sum_{i=1}^s \left[O(i,j) d_{f,ks+i} \right] V_c \quad (4.3)$$

To display any one of the 2^g gray shades g frames are used. Both the row and column voltages are multiplied by a factor $\kappa_f = \sqrt{2^f}$, wherein f ranges from 0 to $(g-1)$. The square of the voltage for the f^{th} frame across the i^{th} pixel in the k^{th} subgroup is given by

$$V_{f,ks+i}^2 = \frac{\sum_{j=1}^q \left[\kappa_f V_r O(i,j) - C_{f,k}(j) \kappa_f V_c \right]^2 + \sum_{\substack{n=0 \\ n \neq k}}^{N/s-1} \sum_{j=1}^q \left[C_{f,n}(j) \kappa_f V_c \right]^2}{\left(\frac{N}{s}\right) q} \quad (4.4)$$

$$V_{f,ks+i}^2 = \frac{\kappa_f^2 V_r^2 \sum_{j=1}^q [O(i,j)]^2 - 2\kappa_f V_r \kappa_f V_c \sum_{j=1}^q O(i,j) C_{f,k}(j) + \sum_{n=0}^{N/s-1} \sum_{j=1}^q [C_{f,n}(j) \kappa_f V_c]^2}{\left(\frac{N}{s}\right) q}$$

$$V_{f,ks+i}^2 = \frac{\kappa_f^2 V_r^2 \sum_{j=1}^q O(i,j)^2 - 2\kappa_f^2 V_r V_c d_{f,ks+i} \sum_{j=1}^q O(i,j)^2 + \kappa_f^2 V_c^2 \sum_{n=0}^{N/s-1} \sum_{i=1}^s \sum_{j=1}^q O(i,j)^2 (d_{f,ns+i})^2}{\left(\frac{N}{s}\right) q}$$

$$V_{f,ks+i}^2 = \frac{\kappa_f^2 V_r^2 q - 2\kappa_f^2 V_r V_c d_{f,ks+i} q + q \kappa_f^2 V_c^2 \sum_{n=0}^{N/s-1} \sum_{i=1}^s (d_{f,ns+i})^2}{\left(\frac{N}{s}\right) q}$$

$$V_{f,ks+i}^2 = \frac{\kappa_f^2 V_r^2 q - 2\kappa_f^2 V_r V_c d_{f,ks+i} q + \kappa_f^2 V_c^2 N q}{q \left(\frac{N}{s} \right)} \quad (4.5)$$

Hence, the rms voltage across the i^{th} pixel in the k^{th} subgroup over a cycle is given by

$$V_{ks+i} = \sqrt{\frac{\sum_{f=0}^{g-1} \kappa_f^2 (V_r^2 q - 2V_r V_c d_{f,ks+i} q + V_c^2 N q)}{q g \left(\frac{N}{s} \right)}} \quad (4.6)$$

If the selected pixel in the $(ks+i)^{th}$ location is OFF, then $d_{f,ks+i} = +1$, for all f ranging from 0 to $(g-1)$. The rms voltage across the OFF pixel is given by

$$V_{off} = \sqrt{\frac{\sum_{f=0}^{g-1} \kappa_f^2 (V_r^2 - 2V_r V_c + V_c^2 N)}{g \left(\frac{N}{s} \right)}} \quad (4.7)$$

Similarly, for an ON pixel $d_{f,ks+i} = -1$ for all f . Thus the rms voltage across the ON pixel is given by,

$$V_{on} = \sqrt{\frac{\sum_{f=0}^{g-1} \kappa_f^2 (V_r^2 + 2V_r V_c + V_c^2 N)}{g \left(\frac{N}{s} \right)}} \quad (4.8)$$

The Selection ratio (**SR**) defined as $\left[\frac{V_{on}}{V_{off}} \right]$ and is maximum when

$$V_r = \sqrt{N} V_c \quad (4.9)$$

$$SR = \sqrt{\frac{\sqrt{N} + 1}{\sqrt{N} - 1}} \quad (4.10)$$

Supply voltage requirement

OFF pixels in the display are biased near the threshold voltage (V_{th}) in order to obtain a good contrast ratio. Hence, $V_{off} = V_{th}$

$$V_{off} = \sqrt{\frac{\sum_{f=0}^{g-1} \kappa_f^2 (V_r^2 - 2V_r V_c + NV_c^2)}{g \left(\frac{N}{s}\right)}} = V_{th}$$

$$\sqrt{\frac{(2^g - 1) (V_r^2 - 2V_r V_c + NV_c^2)}{g \left(\frac{N}{s}\right)}} = V_{th}$$

Where, $\sum_{f=0}^{g-1} \kappa_f^2 = 2^g - 1$ and substituting $V_r = \sqrt{N} V_c$

$$V_c = \sqrt{\frac{g \left(\frac{N}{s}\right)}{(2^g - 1) (2N - 2\sqrt{N})}} V_{th}$$

$$V_c = \sqrt{\left(\frac{g}{2^g - 1}\right) \frac{\sqrt{N}}{2s(\sqrt{N} - 1)}} V_{th} \quad (4.11)$$

Supply voltage requirement depends on the maximum swing in the addressing waveforms. Amplitude of the row select voltage ($\kappa_{g-1} V_r$) is lower than the maximum amplitude of column voltage ($\kappa_{g-1} s V_c$) for $N < s^2$ and is greater when $N > s^2$. Hence, the supply voltage requirement (V_{sup}) is determined separately for these two conditions.

Case I: ($N \leq s^2$)

$$V_{sup} = 2s \kappa_{g-1} V_c$$

$$V_{sup} = 2s \sqrt{2^{g-1}} \sqrt{\left(\frac{g}{2^g - 1}\right) \frac{\sqrt{N}}{2s(\sqrt{N} - 1)}} V_{th}$$

$$V_{sup} = \sqrt{\frac{2s}{\left(1 - \frac{1}{\sqrt{N}}\right)} \left(\frac{g 2^{g-1}}{2^g - 1}\right)} V_{th} \quad (4.12)$$

Case II: ($N \geq s^2$)

$$V_{sup} = 2\kappa_{g-1}V_r$$

$$V_{sup} = 2\sqrt{2^{g-1}}\sqrt{N} V_c$$

$$V_{sup} = 2\sqrt{2^{g-1}}\sqrt{N} \sqrt{\left(\frac{g}{2^g - 1}\right) \frac{\sqrt{N}}{2s(\sqrt{N} - 1)}} V_{th}$$

$$V_{sup} = \sqrt{\frac{2N}{s\left(1 - \frac{1}{\sqrt{N}}\right)}} \left(\frac{g2^{g-1}}{2^g - 1}\right) V_{th} \quad (4.13)$$

Supply voltage requirement when successive approximation is used for displaying gray shades is higher than bi-level display by a factor $\sqrt{\frac{g2^{g-1}}{2^g - 1}}$ (see equation 2.33 and 2.34 for a comparison). Supply voltage for displaying 256 gray shades using 8 frames is twice that of bi-level display (see Figure 4-6).

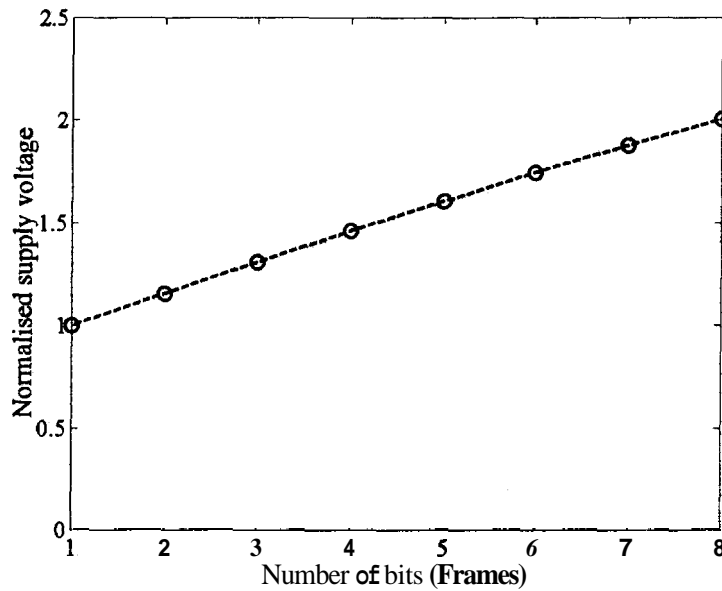


Figure 4-6 Supply voltage (Normalised to that of bi-level display) versus number of bits/pixel while using successive approximation to display gray shades.

This increase in supply voltage is due to varying amplitude of row and column voltages in different frames. The minimum supply voltage can be obtained when $N = s^2$ as in the

case of multi-line addressing technique [20][21]. The hardware realization of a new LCD controller for displaying gray shades using successive approximation based on multi-line addressing technique is discussed in the next section.

4.5. Design and implementation

A simple block diagram of a system for displaying gray shades using successive approximation based on multi-line addressing is as shown in the Figure 4-7. Information to be displayed is stored in the memory. Row select patterns for selecting s-rows in the selected subgroup are generated in row select patterns generator. The s-bit row select pattern and the s-bit data from the data memory are used to generate the column data in the column signal generator (CSG). The column data is then shifted into the column driver. Subgroup sequencer generates the row data, which determines the subgroup to be selected at a given instant of time. Row select pattern is transferred to row driver to select the rows in the subgroup. The row and column voltages are scaled by a factor $\sqrt{2^f}$ in g frames (i.e., $0 \leq f \leq g - 1$) to display 2^g gray shades using successive approximation. All the voltages necessary for the row and column drivers are generated using a voltage level generator. The row and column voltages corresponding to each frame are selected using analog multiplexers. The control unit generates all the control signals for the various sub-blocks and synchronises the flow of the data to scan the matrix display.

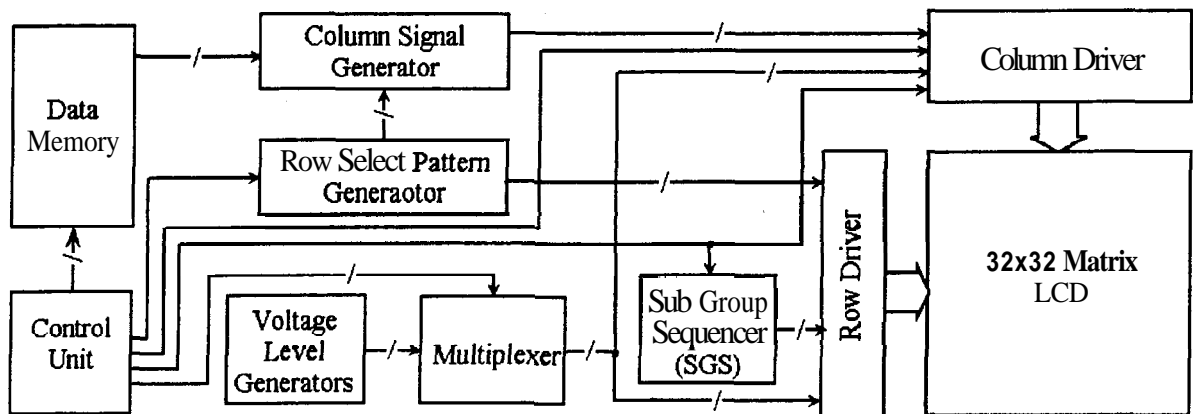


Figure 4-7 Block diagram of MLA driven display system using successive approximation for gray shades.

A controller for displaying gray shades has been implemented using a Complex Programmable Logic Device (CPLD). Figure 4-8 shows the detailed block diagram of the

display system used for displaying gray shades. The controller has been designed to display 16 gray shades using a 32x32 matrix LCD by selecting 3 rows at a time. Hardware design and implementation of the LCD controller is discussed in the next sections.

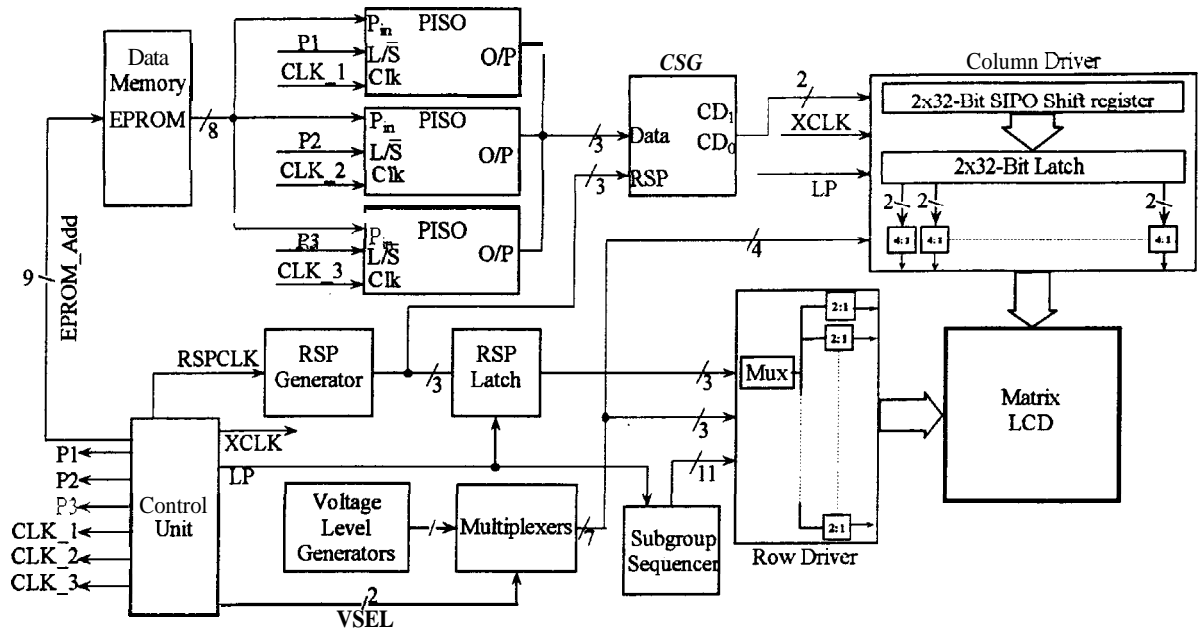


Figure 4-8 Detailed block diagram of the display system for displaying gray shades using successive approximation based on multi-line addressing technique.

4.5.1. Data memory

The information to be displayed is stored in the memory. To display 16 gray shades 4 bits are necessary to represent the data of each pixel. These 4-bit data can be stored in consecutive memory locations. In each frame one bit from the memory is extracted to compute the column data. Alternatively, each bit (MSB to LSB) of the four bit data may be separated and stored in four consecutive memory blocks. In each memory block the data is stored as bit-mapped memory as in the case of data for bi-level image. To demonstrate the technique using a 32x32 matrix LCD, image data are stored in EPROM as bit-mapped image in four consecutive memory blocks. EPROM 2764 is used to store bit plane images. In each memory location of the EPROM 8-bits can be stored. Hence, 8-bits in each bit plane image are grouped to form a byte as shown in the Figure 4-9(a). Each bit is represented as P_{ij} corresponds to i^{th} row and j^{th} column in each bit-plane image. The bit mapping of image into the EPROM is shown in Figure 4-9(b).

The reading data from the memory is sequential while selecting three rows at a time. To read all 4x128 memory locations, nine address lines are necessary (EPROM_Add[8..0]). The 8-bit data from the memory is loaded into the three 8-bit parallel in serial out (PISO) shift registers as shown in the Figure 4-10.

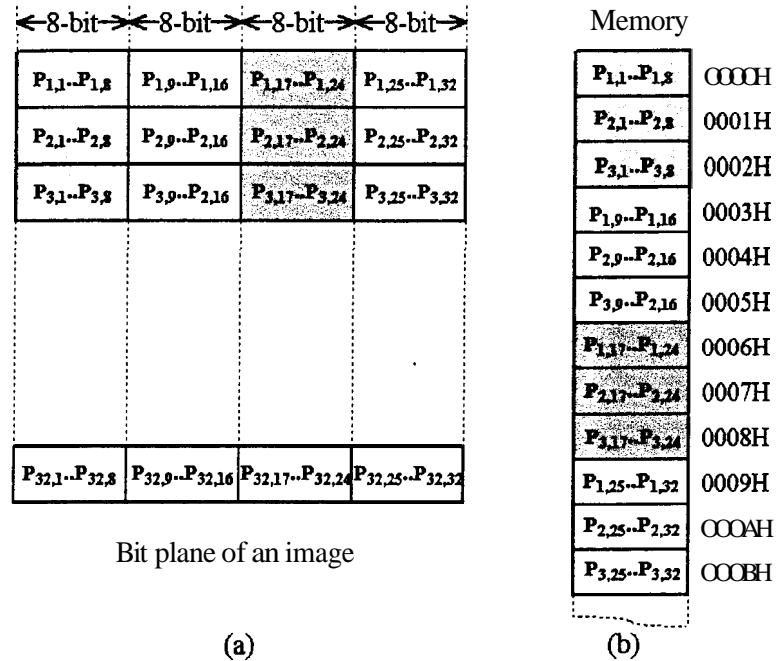


Figure 4-9 Schematic of the data storage in the memory (a) Bit plane of an image to be displayed in 32x32 matrix LCD, (b) bit mapped linear array of memory.

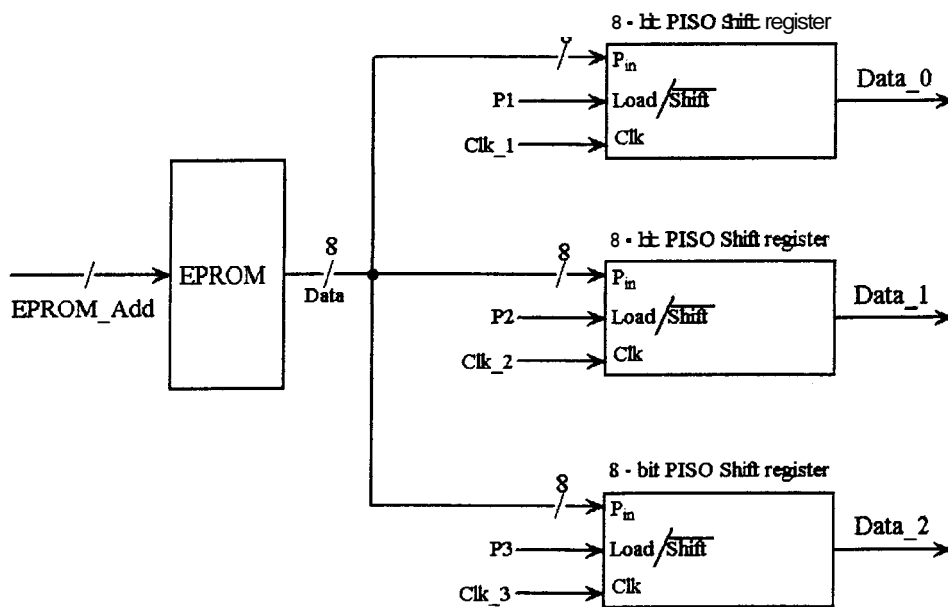


Figure 4-10 Schematic diagram of the data extraction from the memory for column data computation.

The sequence of reading the 8-bit data from the memory and loading into the **PISO** shift register is shown in the Figure 4-11.. At every rising edge of the Add-clk the address lines of the EPROM (i.e., EPROM-Add) is incremented to fetch the 8-bit data from the memory corresponding to eight columns of the selected subgroup. The data corresponding to the 3 rows in the selected subgroup is loaded when **P1**, **P2** and **P3** are high into the three **PISO** shift registers at the rising edge of the clock pulses **clk_1**, **clk_2** and **clk_3** respectively. When **P1**, **P2** and **P3** are low the same clock pulses **clk_1**, **clk_2** and **clk_3** are used to shift the data serially as **Data-0**, **Data_1** and **Data-2** respectively to the column signal generator.

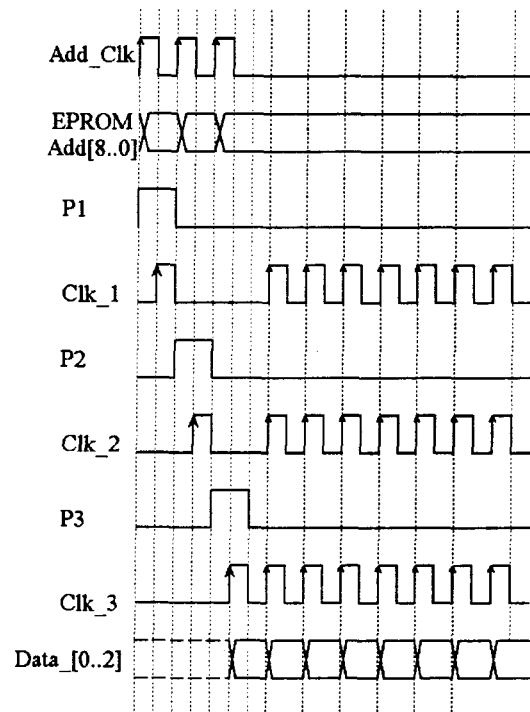


Figure 4-11 Control signals to load the **8-bit** data parallel in to the 3 shift registers and shifting it serially to the column signal generator.

4.5.2. Row select pattern generator

The s-bit row select pattern is generated for selecting the subgroups in the matrix LCD. The row select patterns used to select the subgroups are columns of the Hadamard matrix. The generation of the orthogonal matrices and their matrix representation is given in Appendix B. The three orthogonal functions [**RSP_2,RSP_1,RSP_0**] and its matrix representation is as shown in the Figure 4-12.

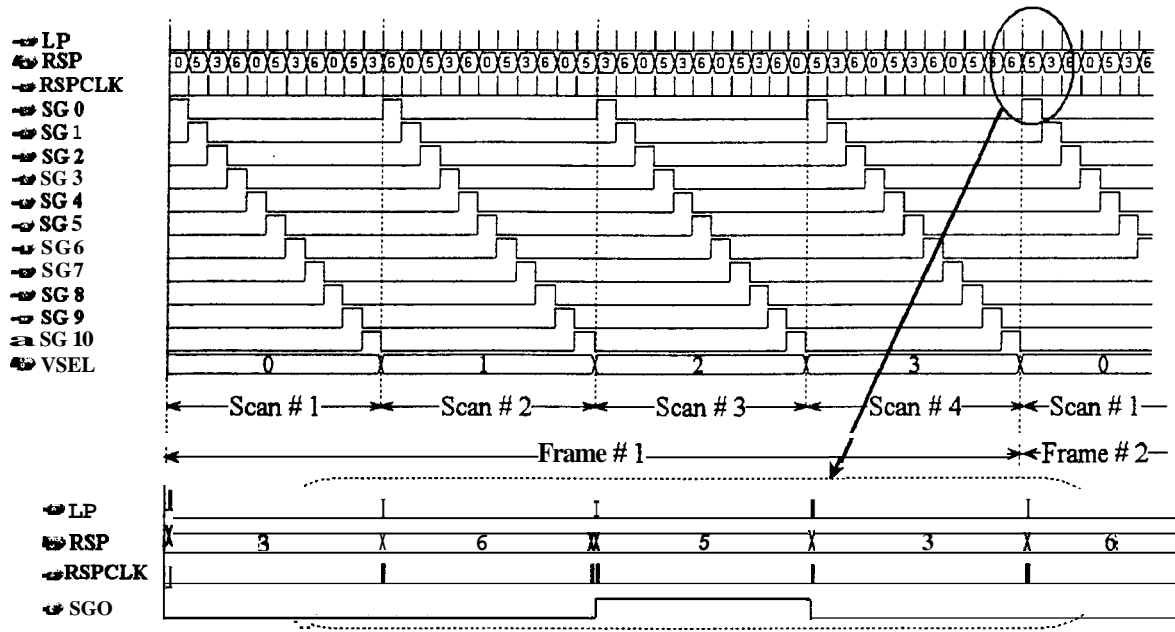


Figure 4-14 Timing sequence of row select patterns in one frame.

Table 4-1

	Frame #1				Frame #2				Frame #3				Frame #4			
	VSEL 00 Scan #1	VSEL 01 Scan #2	VSEL 10 Scan #3	VSEL 11 Scan #4	VSEL 00 Scan #1	VSEL 01 Scan #2	VSEL 10 Scan #3	VSEL 11 Scan #4	VSEL 00 Scan #1	VSEL 01 Scan #2	VSEL 10 Scan #3	VSEL 11 Scan #4	VSEL 00 Scan #1	VSEL 01 Scan #2	VSEL 10 Scan #3	VSEL 11 Scan #4
SG0	0	6	3	5	5	0	6	3	3	5	0	6	6	3	5	0
SG1	5	0	6	3	3	5	0	6	6	3	5	0	0	6	3	5
SG2	3	5	0	6	6	3	5	0	0	6	3	5	5	0	6	3
SG3	6	3	5	0	0	6	3	5	5	0	6	3	3	5	0	6
SG4	0	6	3	5	5	0	6	3	3	5	0	6	6	3	5	0
SG5	5	0	6	3	3	5	0	6	6	3	5	0	0	6	3	5
SG6	3	5	0	6	6	3	5	0	0	6	3	5	5	0	6	3
SG7	6	3	5	0	0	6	3	5	5	0	6	3	3	5	0	6
SG8	0	6	3	5	5	0	6	3	3	5	0	6	6	3	5	0
SG9	5	0	6	3	3	5	0	6	6	3	5	0	0	6	3	5
SG10	3	5	0	6	6	3	5	0	0	6	3	5	5	0	6	3
				0				5					3			6

The entire sequence of row select patterns in a cycle is tabulated in the Table 4-1. The row select pattern which is skipped at end of every frame has been shaded in the Table 4-1 for easy identification. This is essential for dc free operation. This shifts the sequence of row select pattern while selecting the subgroups by one row select pattern at the beginning of

every frame. After four such frames (i.e., one cycle) the entire sequence repeated to refresh the display continuously.

4.5.3. Column Signal Generator (CSG)

Column signal generator computes the dot product of the row select pattern and the data in the selected subgroup. It requires s one-bit multiplier and a serial adder to add s output bits of the multipliers to compute dot product. An Ex-OR gate has been used as a 1-bit multiplier and Table 4-2 shows the truth table of Ex-OR gate as well as 1-bit multiplier. The outputs of the s Ex-OR gates are summed (with equal weightage) to compute column data. The output from the summer is shifted to the column driver card. The generation of column data in all the g frames is same as that for displaying bi-level image.

Table 4-2

Truth Table Ex-OR gate		
Input A (Data)	Input B (RSP)	Output Y
0	0	0
0	1	1
1	0	1
1	1	0

Truth Table 1-bit multiplier		
Input A (Data)	Input B (RSP)	Output Y
+1	+1	+1
+1	-1	-1
-1	+1	-1
-1	-1	+1

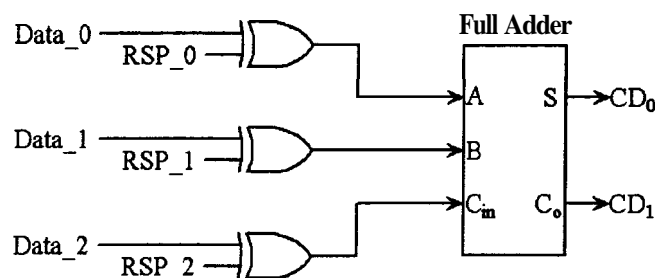


Figure 4-15 Schematic of the column signal generator to generate the column data when selecting three rows at a time.

Column signal generator has been implemented using three Ex-OR gates and a full adder as shown in the Figure 4-15 since three rows are selected simultaneously at a given instant

of time. The two bit column data from the full adder are represented as CD_1 and CD_0 are shifted to the column driver. The 3-bit data (i.e., $Data_0$, $Data_1$ and $Data_2$) changes at every rising edge of the Clk_3 as shown in the Figure 4-11. The falling edge of the same clock (i.e., Clk_3) has been used to shift (i.e., $XCLK$) the data in the column driver.

4.5.4. Voltage Level Generator

The simplest way to generate drive voltages required for the row and column driver is to use voltage divider network as shown in the Figure 4-16. Capacitor (C) is connected as shown to reduce the distortion of the drive waveforms at the time of voltage switching.

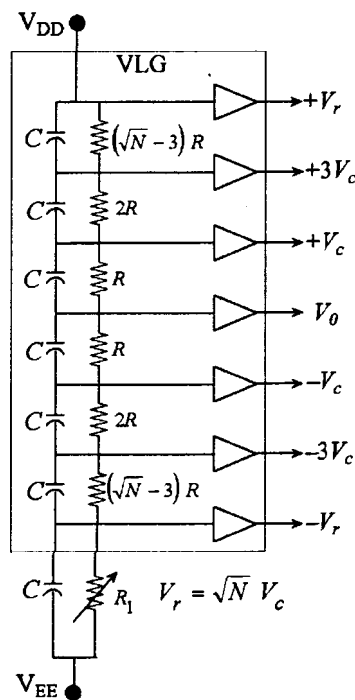


Figure 4-16 Voltage level generator using voltage divider network for MLA technique while selecting three rows at a time.

Number of voltages in the column waveform is $s+1$ when s rows are selected simultaneously and three voltage levels $+V_r$, 0 and $-V_r$ are necessary for the row driver. The voltage level generator (VLG) shown in Figure 4-16 is for the MLA technique for bi-level image while selecting three rows at a time. The potentiometer (R_1) is used to adjust the display contrast by changing the absolute value of the row and column voltages without affecting their ratios. In order to display gray shades using successive approximation row and column voltages are multiplied by a factor κ_f in g frames. The row and column

voltages for four frames for displaying gray shades using successive approximation method can be generated in two different ways as shown in Figure 4-17 and Figure 4-18.

In the Figure 4-17 only one voltage level generator is used and the potentiometers R_1 , R_2 , R_3 and R_4 are connected to it through 4:1 analog multiplexer. One of the potentiometers is connected to the resistor network using the 2-bit frame signal as control input to a 4:1 analog multiplexer. The scaling factor is varied in each frame by fixing the potentiometer R_1 , R_2 , R_3 and R_4 in the ratios $2\sqrt{2} : 2 : \sqrt{2} : 1$ respectively.

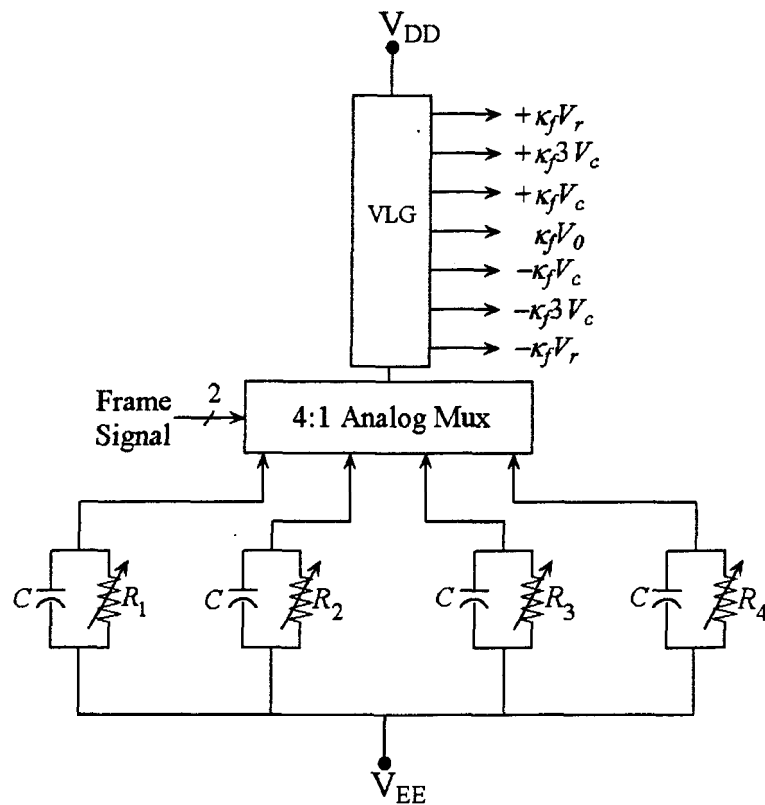


Figure 4-17 Schematic of the voltage level selector using single VLG for generating row and column voltages corresponding to the four frames.

Alternatively the schematic shown in Figure 4-18 uses four voltage level generators with the scaling factors κ_f (where f ranges from 0 to 3) while scanning the display in 4 successive frames. This method has been implemented to generate voltages for the row and column drivers.

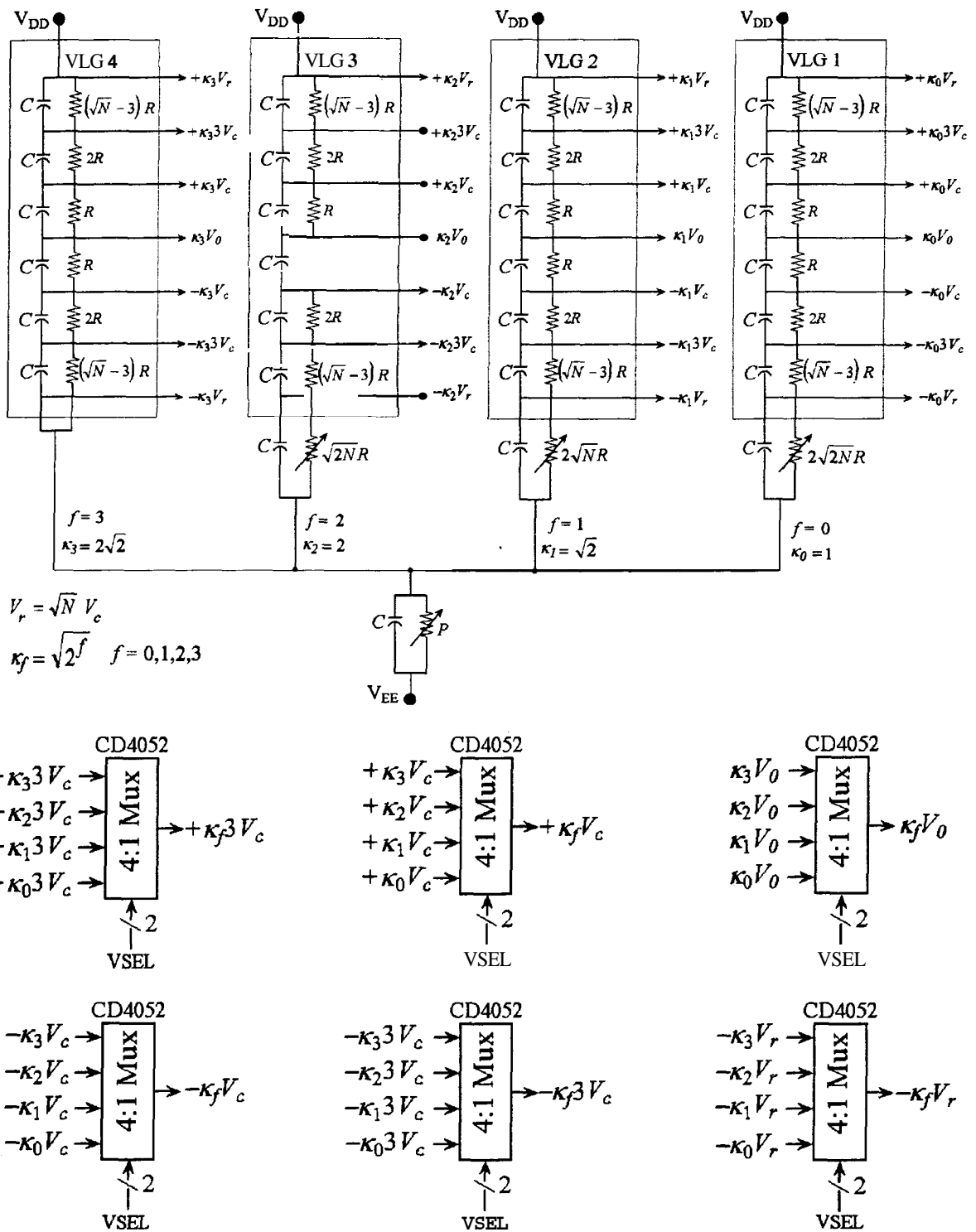


Figure 4-18 Schematic block diagram of the voltage level selector corresponding to the four frames using four VLGs.

The potentiometer (P) is used to adjust the display contrast by changing the absolute value of the row and column voltages without affecting their ratios. The scaled voltage levels from VLG1 to VLG4 correspond to the four bits from LSB to MSB respectively while

scanning the display. Output from one of the VLG is selected corresponding to each frame using 4:1 analog multiplexers. The control signals VSEL generated in the control unit are used as select inputs to the 4:1 analog multiplexers.

4.5.5. Subgroup Sequencer

Subgroup sequencer generates the row data, which determines the subgroup to be selected at a given instant of time. Subgroup sequencer is either a ring counter of length (N/s) or a 1:(N/s) decoder. Here, a 4-bit counter is configured as a mod-11 counter. The eleven decoded outputs SG0, SG1,SG10 are used to select the subgroups one at a time (see Figure 4-14).

4.5.6. Row Driver

In multi-line addressing techniques the row waveforms have three voltage levels. Two voltage levels $+V_r$ and $-V_r$ to select the rows in a subgroup while V_o is applied to the non-selected rows. These voltages are scaled by a factor κ_f in the four frames to display 16 gray shades. Wherein $\kappa_f = \sqrt{2^f}$ and f ranges from 0 to 3. The voltages from the voltage level generators are selected using multiplexers as explained in the previous sections. Figure 4-19 shows the schematic diagram of the row driver for driving 32 rows of the matrix LCD by selecting 3 rows at a time. Here, CMOS analog triple 2-channel Multiplexers / Demultiplexers CD4053 were used to design row driver. Row voltage levels $+\kappa_f V_r$ and $-\kappa_f V_r$ are selected from the RSP generator (i.e., RSP_0, RSP_1 and RSP_2) using a CD4053. Here, row select patterns are used as select inputs to the 2:1 multiplexers. The output from these multiplexers is either $+\kappa_f V_r$ or $-\kappa_f V_r$ depending on the row select pattern 0 or 1, respectively named as RW-0, RW-1 and RW-2. These are connected to each subgroup block to one of the inputs of each 2:1 analog multiplexer as shown in the Figure 4-19. The other input of all the 32, 2:1 multiplexers are connected to the voltage level $\kappa_f V_o$ generated in the VLGs. The subgroup blocks are controlled from the subgroup sequencer outputs SG[10..0]. One subgroup is selected at any instant of time. Hence, only three rows corresponding to the selected subgroup will be selected. For example when

SG0 is high, only first three rows are selected with the row selected patterns with voltages $+\kappa_f V_r$ or $-\kappa_f V_r$.

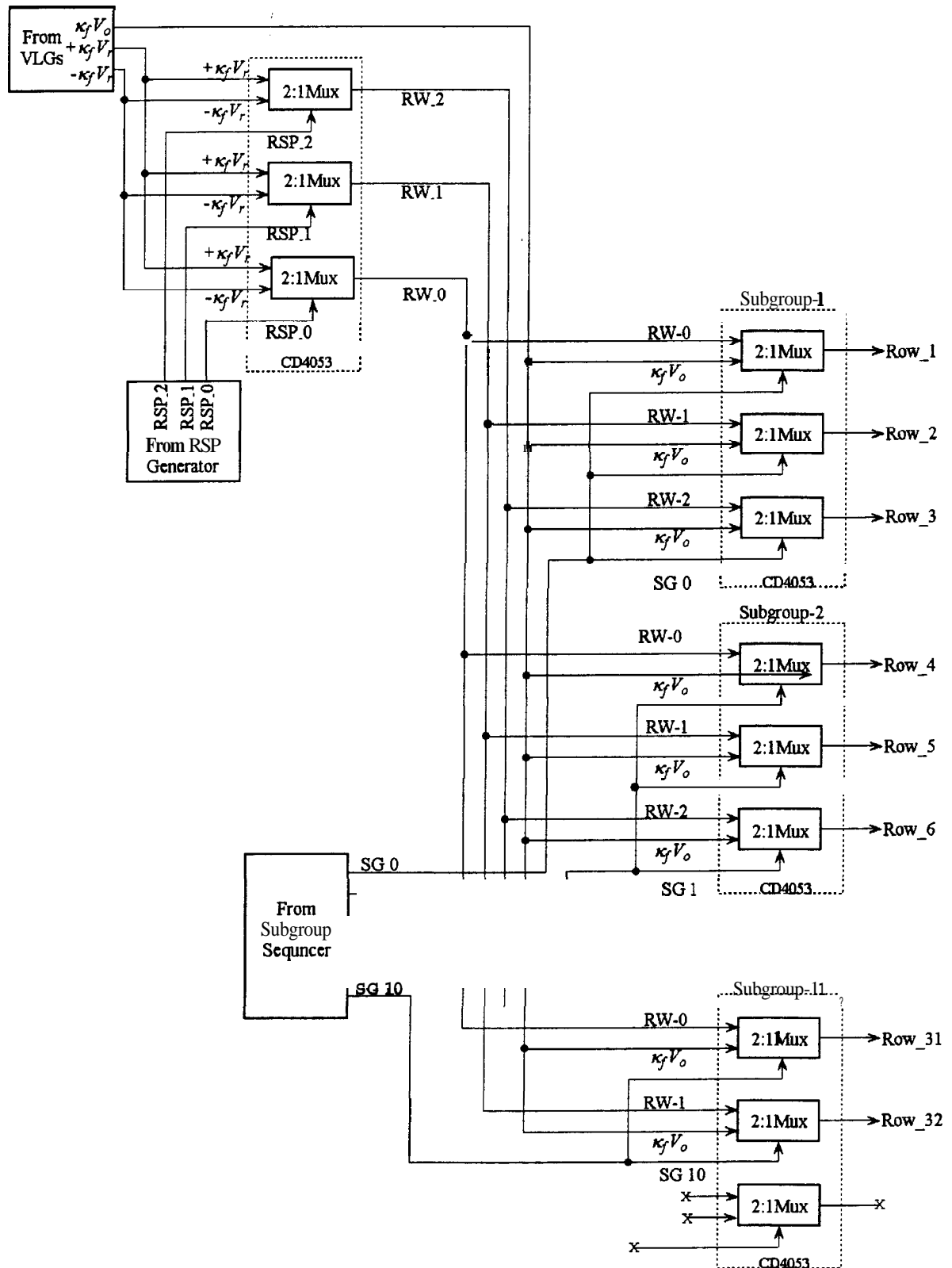


Figure 4-19 Schematic block diagram of the row driver.

The select signals for the rest of the subgroups (i.e., SG 1, SG 2,SG10) are low, thus the voltage level for the rest of the rows are at $\kappa_f V_o$. At every falling edge of the latch pulse (LP) the subgroups are selected and the voltages are applied till the next falling edge of the latch pulse. The column data in the column driver which corresponds to the selected subgroup is also latched simultaneously at the falling edge of the latch pulse. This ensures that both the row and column voltages are applied to the matrix display at the same time.

4.5.7. Column Driver

Column driver for displaying gray shades while using successive approximation technique is same as that used for displaying bi-level images. Four column voltage levels are necessary while selecting 3 rows at a time. The conventional LCD driver supports two voltage levels at a time using a one-bit data. Hence, a column driver has to be designed to support four voltage levels at a time using a 2-bit data. In this case 2-bit column data CD_1 and CD_0 from the CSG are shifted into the shift register serially. This data is simultaneously loaded into the latch when data corresponding to all the columns in the display are shifted in. For a 32 column matrix LCD, 2x32 bit shift register with a parallel latch and 32, 4:1 analog multiplexer are necessary to obtain four column voltage levels depending on the two bit column data. The column driver requirement for each column is as shown in the Figure 4-20.

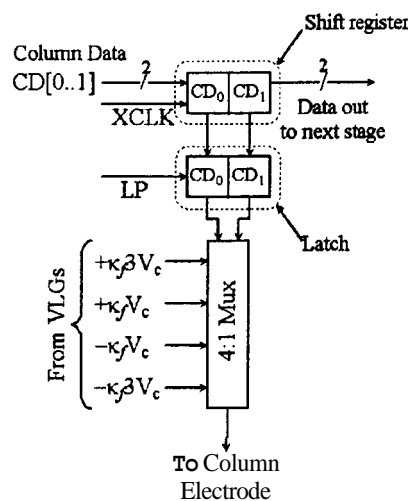


Figure 4-20 Schematic of the column driver required for driving each column.

Column driver has been implemented using standard LCD column drivers SED 1180 and CMOS series CD4051 a 8:1 analog multiplexer (since 4:1 analog multiplexer is not

available, CD4051 8:1 analog multiplexer has been used). Hence, the column driver has been designed to support up to eight voltage levels. Here, two SED 1180 is used as serial in parallel out (SIPO) shift register with latch by connecting ac drive signal FR to V_{DD} and other LCD drive power inputs V_2 , V_3 and V_{SSH} to ground. The SED1180 has a 16 nibble (4-bit) shift register fed by parallel data inputs D_0 , D_1 , D_2 and D_3 . The 2-bit column data CD_0 and CD_1 are connected to data input pins D_0 and D_1 . The other two input pins D_2 and D_3 are connected to ground. In case one want to use eight voltage levels D_2 can be used as additional column data input. Hence, the same column driver can be used to drive eight voltage levels with three bit data while selecting up to seven rows at a time. CD_0 and CD_1 are connected to both the SED1180 and it is shifted into the SED 1180 on the falling edge of the shift clock (XCLK) under the control of the active high enable inputs EI1 and EI2. That is, when EI1 is high the column data is for the first 16 columns. After shifting 16 column data for the first SED1180, EI1 goes low and EI2 is high then next 16 column data is shifted into the second SED1180. After shifting all the 32 column data into the SED1180, the display data is latched on the falling edge of the latch pulse (LP). The latched output from the SED 1180 is connected to the 32, analog multiplexers (CD 4051) as shown in the Figure 4-21.

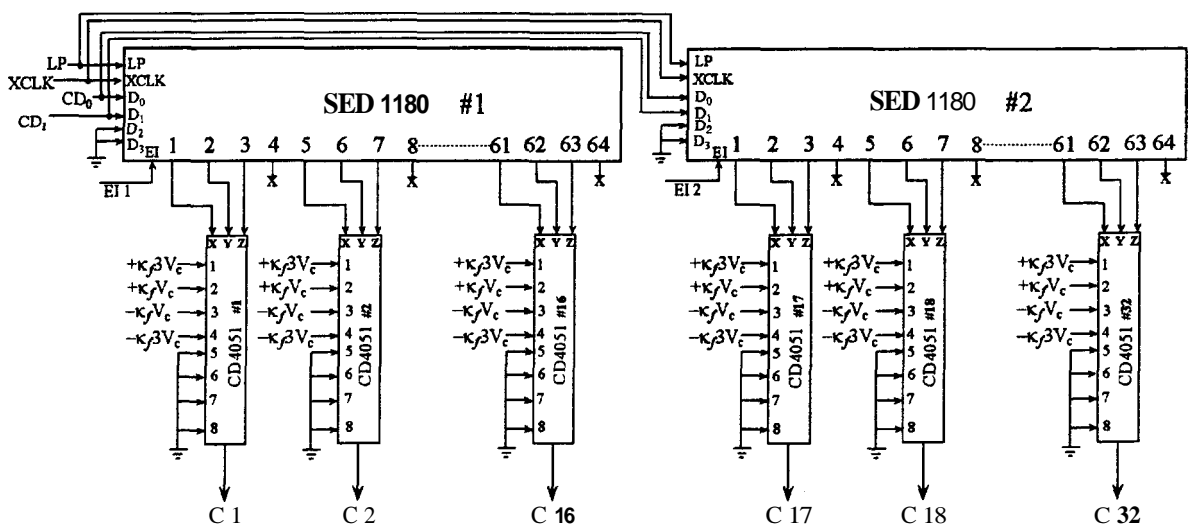


Figure 4-21 Schematic of the column driver for driving 32 column matrix LCD.

The three bits from each nibble are connected to the three bit control inputs of 8:1 analog multiplexers. The fourth bit of each nibble is not used as shown in the Figure 4-21. Four column voltages from output of 4:1 analog multiplexers connected to the VLGs

(i.e., $+ \kappa_f 3V_c$, $+ \kappa_f V_c$, $- \kappa_f V_c$ and $- \kappa_f 3V_c$ see Figure 4-18) are the inputs of all the CD4051, the other four inputs (not used) are connected to ground. The outputs from the 32, CD4051 are connected to the 32 columns of the matrix LCD.

4.5.8. Control unit

Control unit generates all the necessary signals to control the operation of various blocks as explained in the previous sections.

a) Shift Clock (XCLK)

The column data from the column signal generator is shifted into the column driver at every falling edge of a shift clock (XCLK).

b) EI1 and EI2

Display data is shifted into the two SED 1180 #1 and SED 1180 #2 at the falling edge of the shift clock (XCLK) only when corresponding enable signals EI1 or EI2 are high.

c) VSEL

Two-bit control signal VSEL generated to select voltage levels for row and column drivers, from the voltage level generators using 4:1 analog multiplexers.

d) Latch pulse

After shifting all the column data to the column driver, both the column voltage and row voltage are latched at the falling edge of the latch pulse (LP).

The Altera's Complex Programmable Logic Device (CPLD) EPM7128ELC-20 is used as a controller. All the blocks except row driver, column driver, voltage level generators have been implemented in this chip. Inputs to the controller are Master clock (MCLK), power on reset (Por) and 8-bit data from the EPROM. Power on reset (Por) is used to reset all the counter and flip-flops when the power switch is turned ON to ensure proper operation of all the counters and flip-flops. The various signals, which are generated in the LCD controller is shown in the Figure 4-22. All the control signals were first simulated using

Altera MAX-plus II software. The timing sequence for computing column data for all the 32 columns when a subgroup is selected with a given row select pattern is shown in Figure 4-23.

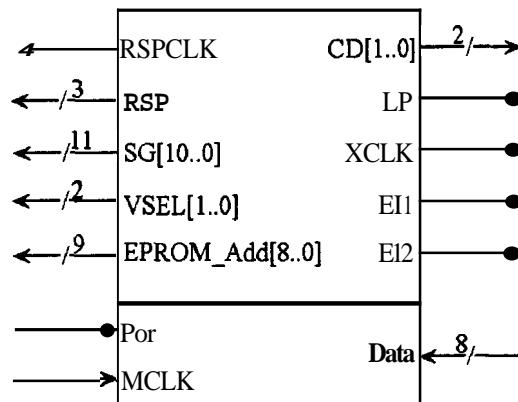


Figure 4-22 Various I/P pins of the LCD controller designed for displaying gray shades.

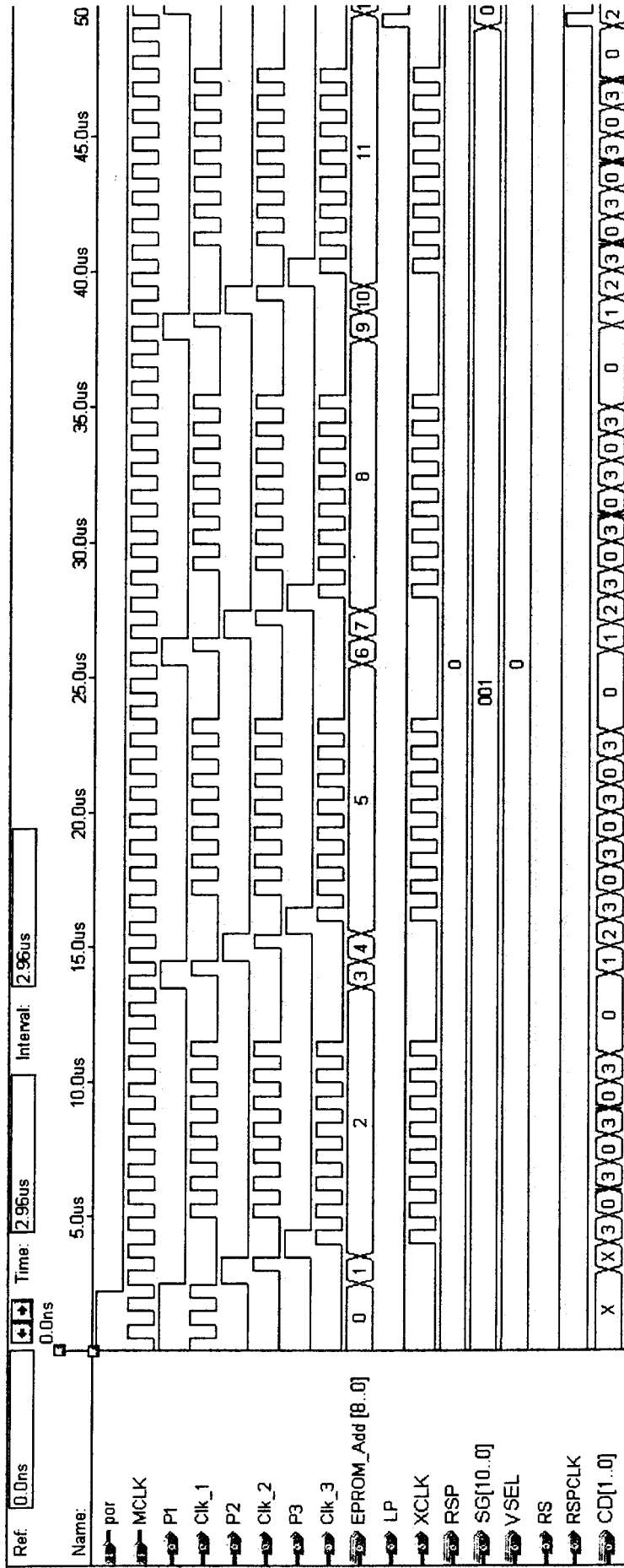
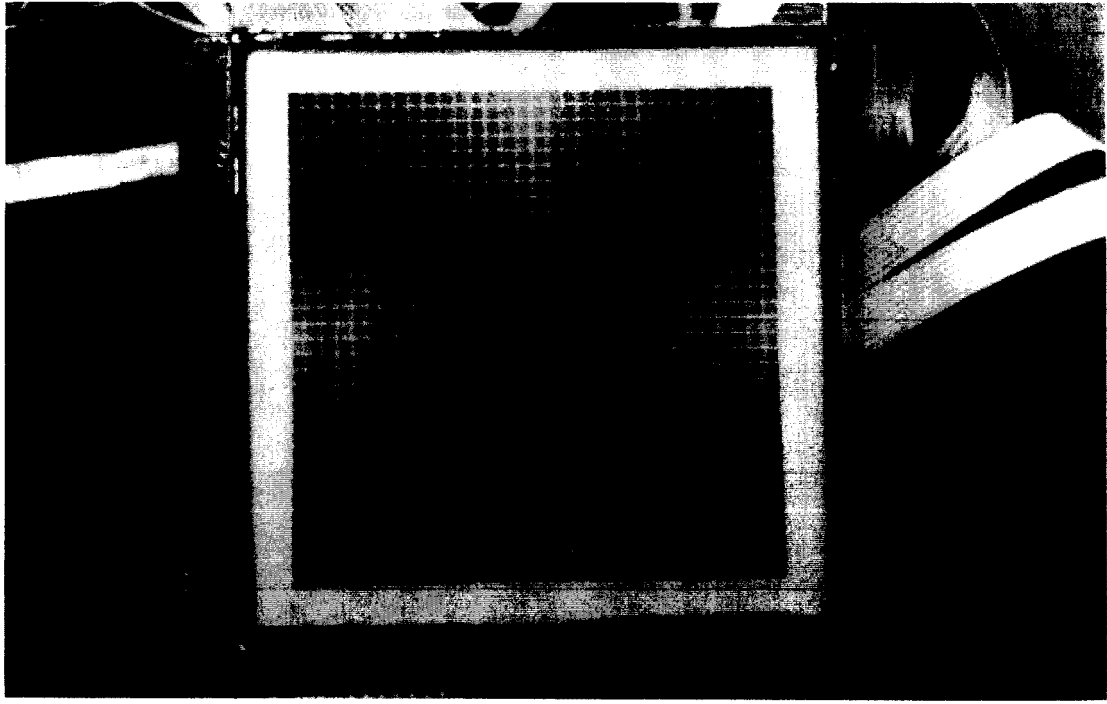


Figure 4-23 Simulated timing sequence of the controller between two latch pulse

4.6. Results and discussions

The addressing technique discussed in this chapter has been demonstrated using a 32x32 matrix TN LCD. Photograph 4-1 shows the matrix LCD displaying 16 gray shades.



Photograph 4-1 32x32 matrix LCD displaying 16 gray shades using successive approximation by selecting three rows at a time.

The typical row and column waveforms were generated using *Waveform Generator WFG 500* (see Appendix C, Figure C-2) to measure the light transmission across the pixel and switching time between gray shades. The transmissions across a pixel for the 16 gray shades were measured using single pixel electro-optic setup (see Appendix C, Figure C-1) by varying the supply voltage. Figure 4-24 shows electro-optic response measured when successive approximation method is used for displaying 16 gray shades. Supply voltage necessary for driving the display when successive approximation method based on multi-line addressing technique is given by (equation 4.13),

$$V_{sup} = \sqrt{s \left(1 - \frac{1}{\sqrt{N}} \right) \left(\frac{g 2^{(g-1)}}{2^g - 1} \right)} V_{th}$$

While driving 32x32 matrix LCD by selecting 3 rows at a time to display 16 gray shades, $N = 32$, $s = 3$ and $g = 4$, hence $V_{sup} = 7.776V_{th}$. The threshold voltage for the liquid crystal mixture used for the display is 1.599V, supply voltage requirement is around $V_{sup}=12.5V$.

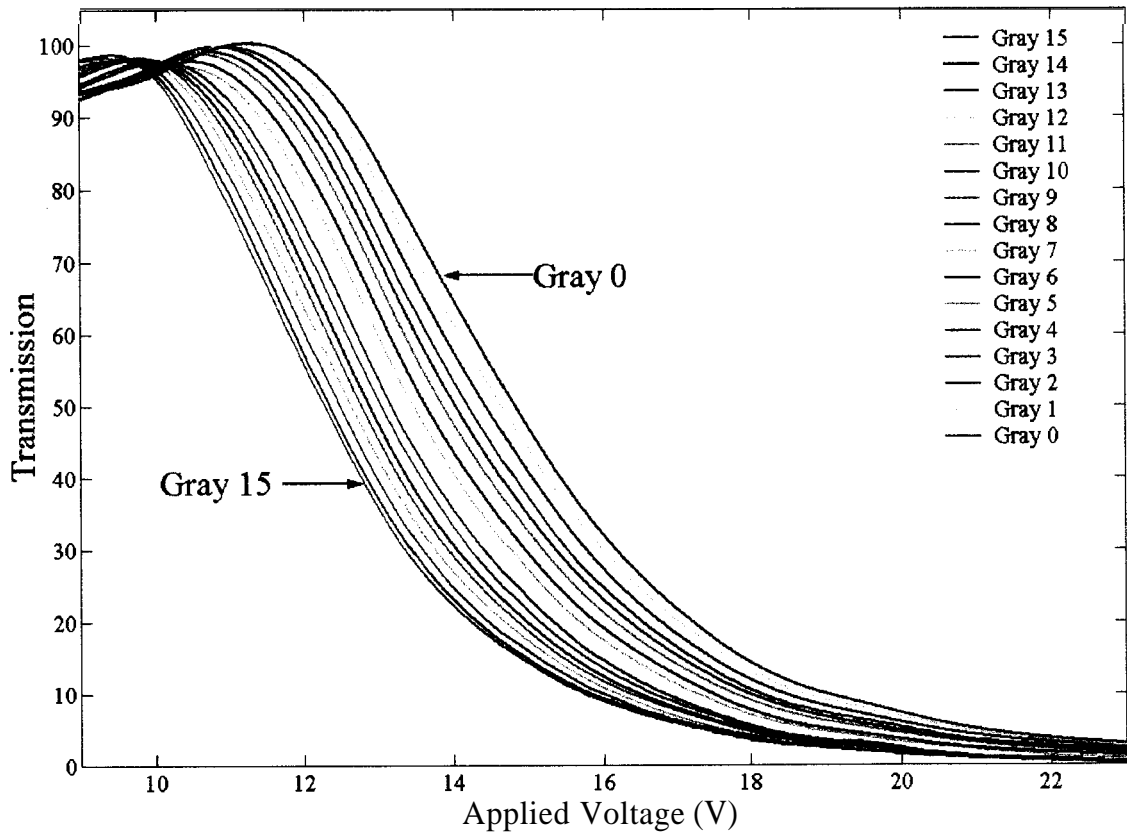


Figure 4-24 Transmission across the cell for 16 gray shades versus supply voltage.

Figure 4-25 shows the typical response of the liquid crystal test cell when actual waveforms were applied when the pixel is driven to display the gray shades between OFF (Gray 0) and ON (Gray 15) states. The switching time between OFF to ON and from ON to OFF state is around 98ms and 99ms respectively. The switching time between the all the 16 gray shades were measured and the results are tabulated in the Table 4-3. The switching time ranges from 48ms to 122ms.

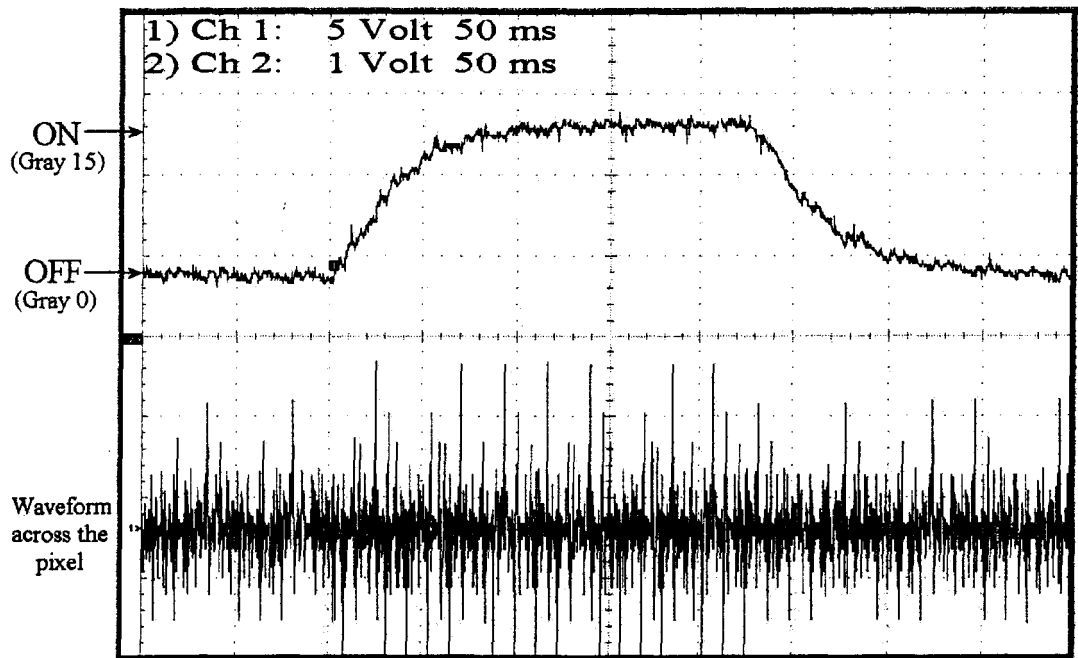


Figure 4-25 Electro-optic response of a pixel when switched between ON and OFF states.

Table 4-3 Response time measured (ms)

		Rise time (OFF to ON) →															
		0	1/16	2/16	3/16	4/16	5/16	6/16	7/16	8/16	9/16	10/16	11/16	12/16	13/16	14/16	1
Fall time (ON to OFF) ↑	0	-	113	109	120	122	120	118	123	113	109	114	112	110	98	96	98
	1/16	104	-	111	104	120	121	117	111	108	119	116	110	106	107	110	99
	2/16	99	101	-	114	113	107	112	101	96	112	104	112	105	101	101	88
	3/16	101	96	98	-	99	83	105	107	96	104	106	98	99	91	88	100
	4/16	117	103	89	100	-	94	98	107	96	104	100	89	105	101	96	93
	5/16	116	113	86	87	87	-	92	108	90	90	102	106	89	91	94	92
	6/16	107	106	98	93	110	84	-	89	96	92	97	96	89	89	87	87
	7/16	106	116	97	95	99	96	85	-	89	87	87	88	97	80	86	88
	8/16	96	96	86	74	96	93	79	76	-	82	88	76	87	84	85	82
	9/16	97	108	96	93	99	98	102	78	84	-	77	83	74	72	69	69
	10/16	100	96	98	94	94	97	92	84	76	70	-	73	76	86	86	78
	11/16	102	100	106	96	94	102	93	92	77	79	86	-	67	71	66	62
	12/16	92	101	86	101	93	93	87	96	74	78	82	76	-	68	68	67
	13/16	91	96	91	96	99	92	86	93	74	66	69	86	90	-	54	49
	14/16	92	107	93	100	96	93	91	98	96	81	83	62	69	67	-	48
	1	99	102	92	97	111	97	92	96	92	80	76	62	66	66	66	-

The controller part for driving 32x32 matrix TN LCD to display 16 gray shades was implemented using the Altera's CPLD EPM7128ELC-20. Photograph 4-2 shows the LCD displaying 16 gray shades using successive approximation approach by selecting 3 rows at a time. The row and column waveforms across the ON (Gray 15) and OFF (Gray 0) and

the resultant waveform across the pixel were captured using the oscilloscope. Figure 4-26 shows waveforms in four successive frames. Figure 4-27 shows the row and column waveforms in one of the four frames and the resultant waveform across the pixel. The rms voltages across the pixels were measured using a logging multimeter (HP 3467A). Figure 4-28 shows the rms voltages measured across the pixels versus supply voltage for the 16 gray shades. The selection ratio (i.e., the ratio of rms voltage across the Gray 15 to that of Gray 0) versus supply voltage is plotted in the Figure 4-29. The selection ratio obtained from these measurements agrees within 0.5% of the theoretical value of 1.1956. The rms voltage across the pixels were measured and compared with the theoretical values. Table 4-4 shows the error in rms voltage across the pixels for the 16 gray shades under various supply voltages and the error ranges between 0.1260% to 2.2207%.

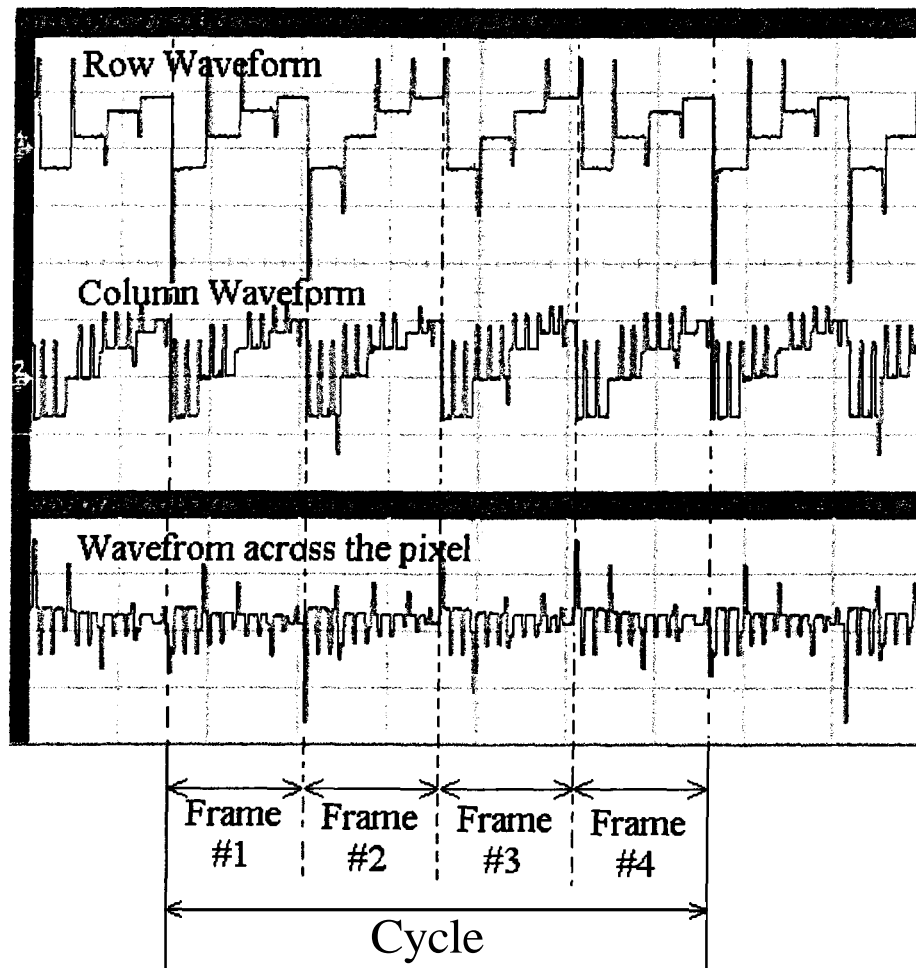


Figure 4-26 Row waveform, column waveform and waveform across the pixel captured using the oscilloscope showing four frames.

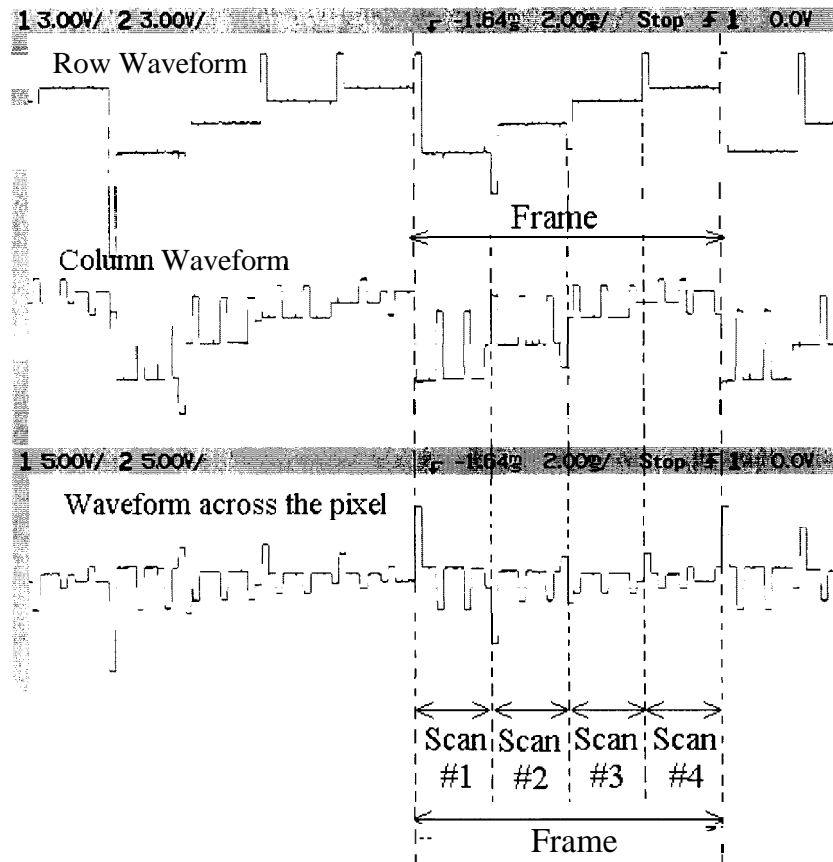
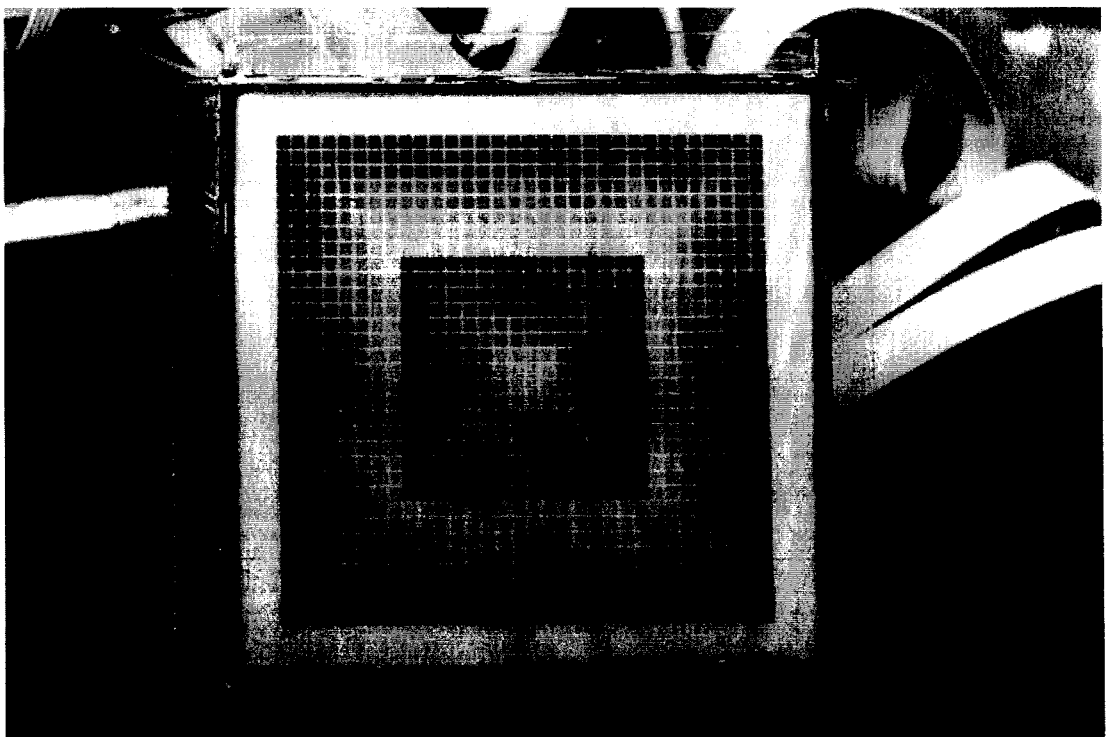


Figure 4-27 Typical addressing waveforms captured using the oscilloscope in a frame and the resultant waveform across the pixel.



Photograph 4-2 32x32 matrix LCD displaying 16 gray shades using successive approximation by selecting three rows at a time.

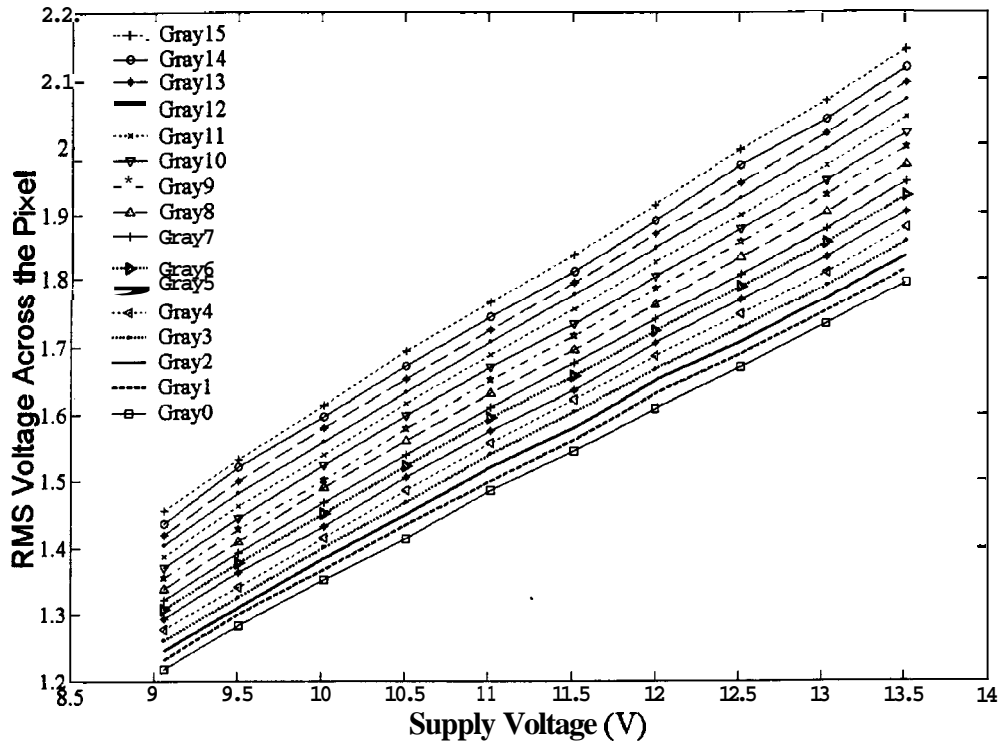


Figure 4-28 The rms voltage measured across the pixels with 16 gray shade. versus the supply voltage.

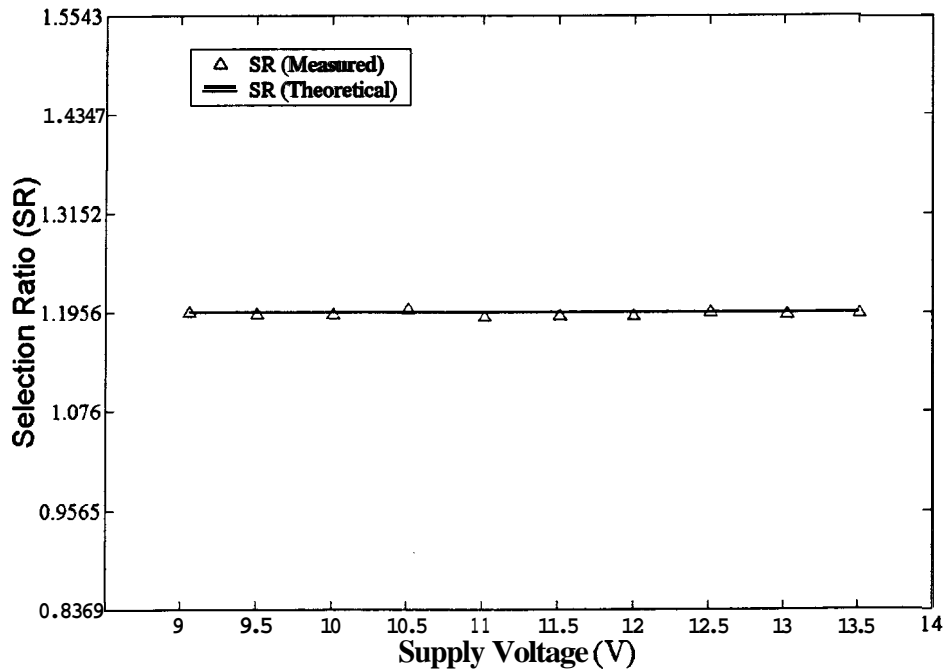


Figure 4-29 Selection ratio versus supply voltage.

Table 4-4

Supply Voltage (Volts)	% Of Error for different gray shades = $\left(\frac{V_{rms}(Calculated) - V_{rms}(Measured)}{V_{rms}(Calculated)} \right) 100$															
	Gray15	Gray14	Gray13	Gray12	Gray11	Gray10	Gray9	Gray8	Gray7	Gray6	Gray5	Gray4	Gray3	Gray2	Gray1	Gray0
9.0630	0.1261	0.4692	0.5568	0.6565	0.7183	0.8781	0.8242	0.9634	1.0771	0.9217	0.7936	0.6697	0.6442	0.5844	0.3590	0.1158
9.5040	0.3632	0.1368	0.4493	0.6024	0.2219	0.4075	0.3755	0.5555	0.5976	0.4529	0.2384	0.6176	0.5021	0.2976	0.4776	0.3304
10.0130	0.3974	0.4638	0.4513	0.1521	0.2755	0.2586	0.5598	0.1651	0.4861	0.4439	0.5105	0.4998	0.1942	0.0723	0.4116	0.3178
10.5100	0.3087	0.0601	0.2187	0.3451	0.2593	0.3093	0.4553	0.4575	0.6398	0.5247	0.3188	0.4136	0.3381	0.1948	0.6498	0.7020
11.0150	0.1762	0.3931	0.4830	0.4823	0.6055	0.6065	0.6312	0.6799	0.8023	0.4895	0.5390	0.4460	0.2108	0.1555	0.1531	0.3741
11.5160	0.6903	0.9898	0.8936	0.8848	1.0503	1.2303	1.1544	1.2152	1.1932	1.1445	1.2004	0.8201	0.6054	0.8069	0.5818	0.2791
12.0010	0.8172	1.0651	1.0432	1.1168	1.1807	1.3433	1.2267	1.4017	1.5333	1.3221	1.1544	1.0724	0.9361	0.5737	0.3845	0.3997
12.5140	0.8081	1.0044	1.2957	1.4285	1.6047	1.6682	1.5618	1.6545	1.8985	1.7008	1.5888	1.5484	1.4734	1.3386	1.0938	0.8346
13.0270	1.2294	1.5754	1.5771	1.7156	1.8957	1.9674	1.8757	2.0779	2.2194	2.0865	2.0423	2.0356	1.8150	1.5880	1.3702	1.0754
13.5130	1.3301	1.5821	1.5940	1.7377	1.9213	2.0001	1.9212	2.0758	2.2207	2.1007	2.1174	2.0669	1.8930	1.6973	1.4778	1.1943