A DIGITAL CORRELATION RECEIVER FOR THE AURIBIDANUR DECAMETRE WAVE RADIO TELESCOPE

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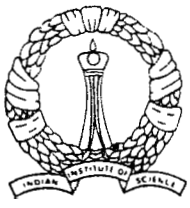
By
D. K. RAVINDRA, B.E.,



Department of Electrical Communication Engineering
Indian Institute of Science
Bangalore-560012
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PREFACE

THE WORK PRESENTED IN THIS THESIS HAS BEEN CARRIED OUT AT THE RAMAN RESEARCH INSTITUTE, BANGALORE WHERE THE AUTHOR IS WORKING, IT WAS DONE UNDER THE GUIDANCE OF DR. S. KRISHNAN AND PROFESSOR V. RADHAKRISHNAN OF THE RAMAN RESEARCH INSTITUTE, AND PROFESSOR A, KUMAR, DEPARTMENT OF ELECTRICAL COMMUNICATION ENGINEERING, INDIAN INSTITUTE OF SCIENCE, BANGALORE, THE AUTHOR IS REGISTERED AS A PH.D. RESEARCH STUDENT WITH THE INDIAN INSTITUTE OF SCIENCE, BANGALORE UNDER THEIR EXTERNAL REGISTRATION PROGRAMME,

THE DIGITAL CORRELATION RECEIVER WHOSE DESIGN, DEVELOPMENT, CONSTRUCTION AND TESTING ARE PRESENTED IN THIS THESIS IS TO BE PART OF THE DECAMETRE WAVE RADIO TELESCOPE AT GAURIBIDANUR WHICH WAS SET UP JOINTLY BY THE RAMAN RESEARCH INSTITUTE AND THE INDIAN INSTITUTE OF ASTROPHYSICS, BANGALORE. ITS REALISATION IS THE CONTRIBUTION MADE BY THE AUTHOR TO THIS JOINT PROGRAMME ALTHOUGH THE WORK WAS CARRIED OUT ENTIRELY AT THE RAMAN RESEARCH INSTITUTE, BANGALORE.

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CONTXNTS

GLOSSARY OF SYMBOLS

a_n	-	Cosine Correlation Coefficient
b_n	-	Sine Correlation Coefficient
$\mathcal{B}(\Delta\tau)$	-	Bandwidth decorrelation
	-	Velocity of propagation of em wave through cable
	-	Velocity of propagation of em wave through free space
$\Delta\nu$	-	Bandwidth of the signal
$\Delta\psi$	-	Phase Correction angle
$\Delta\tau$	-	Error in time delay compensation
K	-	Kelvin (Chap. 1)
L	-	Length of cable in metres
λ	-	Wavelength .
	-	Metre (Chap, 1)
	-	Direction Cosine in declination (Chap. 4) .
ms	-	millisecond
μs	-	microsecond
ns	-	nanosecond
ϕ, ϕ_2	-	Two phase clocks in the Correlator Circuit
ρ_T	-	True Correlation Coefficient
ρ_m	-	measured Correlation Coefficient
S_1, S_2	-	Down converted signals from Ant. 1 and Ant. 2 respectively.
S_1', S_2'	-	Down Converted signals (90°-phase shifted) from Ant.1 and Ant. 2 respectively
T_{map}	-	Brightness temperature
τ_g	-	Time delay due to path length difference in space

τ_2	-	Time delay due to path length differences through cable
	-	Total time delay
	-	Increment angles for the beams in the FT processing
V_n	-	nth harmonic of spatial frequency
W	-	Watt
ω	-	radian frequency
x	-	interferometer spacing
Z	-	Zenith angle

GLOSSARY OF ABBREVIATIONS

A/L -n	Adder/Latch Circuit-n
ADD-CL	Address clock for reading console thumbwheel switches
AN	Alpha numeric
An	Attenuators-n
BPF	Bandpass filter
BUF-n	Buffer number n
CL-12	Control signal for MUX-12
CLCO	Clock for counter-O
CLEN	Clock enable
CLK-n	Bandpass sampling clock-n
CLN	Clock for normal operation
CLP	Clock for phase correction
CL PROG	Clock for programming
CLXY-n	Input and output clock signals for multiplier-n
CM-12	Control signal for MUX-12
CMOS	Complementary Metal-oxide semiconductor logic
Cn	Control signal for MUX-n
COMP-O	Comparator number zero
COS	Cosine
CPAL	Counter for alarm condition
$\overline{\text{CSBC}}$	Chip select signal for bus coupler
CSn	Chip select signal for n-RAM
DEC	Beclination
DFT	Discrete Fourier Transform

$\overline{\text{DIEN}}$	Data input enable
DMA	Direct memory Access
$\overline{\text{DMA OUT}}$	Direct memory access signal in microprocessor
DSB	Double sideband
ECIL	Electronic Corporation of India Ltd.
EFn	External flag-n
ENAN	Enable an-RAM
ENBN	Enalbe bn-RAM
EXNOR	Exclusive- Nor gate
EXOR	Exclusive- or gate
mFF-n	Flip flop number n for the function m
FT	Fourier transform
GIP	Sap in process signal
Gn	Logic gate circuit-n
GT-n	Grading table - n
HP	Hewlett Packard
IF	Intermediate Frequency
K	Total number of samples
Ka	Number of anticoincidences
Kc	Number of coincidences
KHz	Silo Hertz
LC	Latch counter
LSB	Least significant bit
LSI	Large scale integrated circuit
MHz	Mega Hertz
	Multiplier - n

MONO-n	Monostable number n
MPEN	Microprocessor enable
$\overline{\text{MRD}}$	Memory Read cycle in microprocessor
MSB	Most significant bit
MTRLI	Multi Telescope Radio Linked Interferometer
MTU	Magnetic Tape Unit
MTX	Matrox
MUX-n	Multiplexer - n
$\overline{\text{MWR}}$	Memory Write cycle in nicroprocessor
Nn	Noise source - n
OPC1 > BF	output of counter-1 at the completion of Beam-finish
QmCn	m^{th} bit output from counter n
R/W	Read/Write signals for n-RAM
RA	Right Ascension
n-RAM	Menory for storing particular data given by n
RAMs	Random-access memories
READ-N	Read pulses in the normal node
RLO	Reset LATCH-0
R	Read only memories
S/N	Signal to noise ratio
SCMn	Sign bit for multiplier-n in correction mode
SEW	Signal from east-west array
Sin	Sine
SMn	Sign bit for multiplier number - n
Sn	Keyboard switch - n

SNMn	Sign bit for multiplier-n in normal mode
SNRn	Signal to noise ratio in channel n
SNSn	Signal from North-South element - n
SR	Service Request signal
SSB	Single sideband
STLO	Strobe LATCH-0
STLIX, STLI	Strobe Latch-1 signals
T/C-0	True/complement circuit number - 0
tn	propagation time
TPB-DEL	Write signal in delay buffer unit
TPB-TV	Write signal in TV buffer unit
TTL	Transistor-transistor logic
TTY	Teletype unit
TV	Television
VLA	Very Large Array
VLBI	Very Long Base line Interferometer
Xn	n^{th} bit input at Multiplier-1
Xn'	n^{th} bit input at Multiplier-2
Xn	Control bits for delay shift register in N-S channels (FIG 5.9)
y_n	n^{th} bit input at Multiplier-1
y_n'	n^{th} bit input at Multiplier-2
y_n	Control bits for delay shift register in N-S channel (FIG 5.9)
ZCD	Zero-cross detector
Z_n	Control bits for delay shift register in E-W channel

LIST OF FIGURES

LIST OF TABLES