

**A DIGITAL CORRELATION RECEIVER  
FOR THE  
AURIBIDANUR DECAMETRE WAVE RADIO TELESCOPE**

A thesis submitted for the degree  
of  
**DOCTOR OF PHILOSOPHY**  
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PREFACE

THE WORK PRESENTED IN THIS THESIS HAS BEEN CARRIED OUT AT THE RAMAN RESEARCH INSTITUTE, BANGALORE WHERE THE AUTHOR IS WORKING, IT WAS DONE UNDER THE GUIDANCE OF DR. S. KRISHNAN AND PROFESSOR V. RADHAKRISHNAN OF THE RAMAN RESEARCH INSTITUTE, AND PROFESSOR A. KUMAR, DEPARTMENT OF ELECTRICAL COMMUNICATION ENGINEERING, INDIAN INSTITUTE OF SCIENCE, BANGALORE, THE AUTHOR IS REGISTERED AS A PH.D. RESEARCH STUDENT WITH THE INDIAN INSTITUTE OF SCIENCE, BANGALORE UNDER THEIR EXTERNAL REGISTRATION PROGRAMME,

THE DIGITAL CORRELATION RECEIVER WHOSE DESIGN, DEVELOPMENT, CONSTRUCTION AND TESTING ARE PRESENTED IN THIS THESIS IS TO BE PART OF THE DECAMETRE WAVE RADIO TELESCOPE AT GAURIBIDANUR WHICH WAS SET UP JOINTLY BY THE RAMAN RESEARCH INSTITUTE AND THE INDIAN INSTITUTE OF ASTROPHYSICS, BANGALORE. ITS REALISATION IS THE CONTRIBUTION MADE BY THE AUTHOR TO THIS JOINT PROGRAMME ALTHOUGH THE WORK WAS CARRIED OUT ENTIRELY AT THE RAMAN RESEARCH INSTITUTE, BANGALORE.

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GLOSSARY OF SYMBOLS

$a_n$	- Cosine Correlation Coefficient
$b_n$	- Sine Correlation Coefficient
$B(\Delta\tau)$	- Bandwidth decorrelation
	- Velocity of propagation of em wave through cable
	- Velocity of propagation of em wave through free space
$\Delta\nu$	- Bandwidth of the signal
$\Delta\psi$	- Phase Correction angle
$\Delta\tau$	- Error in time delay compensation
K	- Kelvin (Chap. 1)
L	- Length of cable in metres
$\lambda$	- Wavelength
	- Metre (Chap, 1)
	- Direction Cosine in declination (Chap. 4)
ms	- millisecond
$\mu$ s	- microsecond
ns	- nanosecond
$\phi, \phi_2$	- Two phase clocks in the Correlator Circuit
$\rho_T$	- True Correlation Coefficient
$\rho_m$	- measured Correlation Coefficient
$S_1, S_2$	- Down converted signals from Ant. 1 and Ant. 2 respectively.
$S_1', S_2'$	- Down Converted signals ( $90^\circ$ -phase shifted) from Ant.1 and Ant. 2 respectively
$T_{map}$	- Brightness temperature
$\tau_i$	- Time delay due to path length difference in space



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- $\tau_2$  - Time delay due to path length differences through cable
- Total time delay
- Increment angles for the beams in the FT processing
- $V_n$  - nth harmonic of spatial frequency
- $w$  - Watt
- $\omega$  - radian frequency
- $x$  - interferometer spacing
- $z$  - Zenith angle

## GLOSSARY OF ABBREVIATIONS

A/L -n	Adder/Latch Circuit-n
ADD-CL	Address clock for reading console thumbwheel switches
AN	Alpha numeric
An	Attenuators-n
BPF	Bandpass filter
BUF-n	Buffer number n
CL-12	Control signal for MUX-12
CLCO	Clock for counter-0
CLEN	Clock enable
CLK-n	Bandpass sampling clock-n
CLN	Clock for normal operation
CLP	Clock for phase correction
CL PROG	Clock for programming
CLXY-n	Input and output clock signals for multiplier-n
CM-12	Control signal for MUX-12
CMOS	Complementary Metal-oxide semiconductor logic
Cn	Control signal for MUX-n
COMP-0	Comparator number zero
COS	Cosine
CPAL	Counter for alarm condition
$\overline{\text{CSBC}}$	Chip select signal for bus coupler
CSn	Chip select signal for n-RAM
DEC	Declination
DFT	Discrete Fourier Transform

<u>DIEN</u>	Data input enable
DMA	Direct memory Access
<u>DMA OUT</u>	Direct memory access signal in microprocessor
DSB	Double sideband
ECIL	Electronic Corporation of India Ltd.
EF <sub>n</sub>	External flag-n
ENAN	Enable an-RAM
ENBN	Enable bn-RAM
EXNOR	Exclusive- Nor gate
EXOR	Exclusive- or gate
mFF-n	Flip flop number n for the function m
FT	Fourier transform
GIP	Sap in process signal
G <sub>n</sub>	Logic gate circuit-n
GT-n	Grading table - n
HP	Hewlett Packard
IF	Intermediate Frequency
K	Total number of samples
K <sub>a</sub>	Number of anticoincidences
K <sub>c</sub>	Number of coincidences
KHz	Kilo Hertz
LC	Latch counter
LSB	Least significant bit
LSI	Large scale integrated circuit
MHz	Mega Hertz
	Multiplier - n

MONO-n	Monostable number n
MPEN	Microprocessor enable
$\overline{\text{MRD}}$	Memory Read cycle in microprocessor
MSB	Most significant bit
MTRLI	Multi Telescope Radio Linked Interferometer
MTU	Magnetic Tape Unit
MTX	Matrox
MUX-n	<b>Multiplexer - n</b>
$\overline{\text{MWR}}$	Memory Write cycle in microprocessor
Nn	Noise source - n
OPC1 > BF	output of counter-1 at the completion of Beam-finish
QmCn	m <sup>th</sup> bit output from counter n
R/W	Read/Write signals for n-RAM
RA	Right Ascension
n-RAM	Memory for storing particular data given by n
RAMs	Random-access memories
READ-N	Read pulses in the normal mode
RLO	Reset LATCH-0
RAM	Read only memories
S/N	Signal to noise ratio
SCMn	Sign bit for multiplier-n in correction mode
SEW	Signal from east-west array
Si n	Sine
SMn	Sign bit for multiplier number ÷ n
Sn	Keyboard switch - n

SNM <sub>n</sub>	Sign bit for multiplier-n in normal mode
SNR <sub>n</sub>	Signal to noise ratio in channel n
SNS <sub>n</sub>	Signal from North-South element - n
SR	Service Request signal
SSB	Single sideband
STLO	Strobe LATCH-0
STLIX, STLI	Strobe Latch-1 signals
T/C-0	True/complement circuit number - 0
t <sub>n</sub>	propagation time
TPB-DEL	Write signal in delay buffer unit
TPB-TV	Write signal in TV buffer unit
TTL	Transistor-transistor logic
TTY	Teletype unit
TV	Television
VLA	Very Large Array
VLBI	Very Long Base line Interferometer
X <sub>n</sub>	n <sup>th</sup> bit input at Multiplier-1
X <sub>n</sub> '	n <sup>th</sup> bit input at Multiplier-2
X <sub>n</sub>	Control bits for delay shift register in N-S channels (FIG 5.9)
y <sub>n</sub>	n <sup>th</sup> bit input at Multiplier-1
y <sub>n</sub> '	n <sup>th</sup> bit input at Multiplier-2
y <sub>n</sub>	Control bits for delay shift register in N-S channel (FIG 5.9)
ZCD	Zero-cross detector
Z <sub>n</sub>	Control bits for delay shift register in E-W channel

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