CHAPTER -5

MICROCOMPUTER SYSTEM

5.1 Introduction

The data from the Fourier Transform (FT) processor is displayed on a TV monitor and also stored on an incremental magnetic tape recorder at the end of each post-integration period. The computed brightness values corresponding to different beams are displayed on the TV monitor as a column of points. A two-dimensional brightness distribution map is obtained by real-time processing and displaying successive columns of points progressing leftwards as the earth rotates from west to east. As already mentioned in Sec. 2.2.2.4 a microcomputer based on the RCA 1802 microprocessor has been designed and constructed to act as a peripheral controller for the real-time operation mentioned above.

In addition to the above operation, the microcomputer is designed to read the control settings for the number of beams, the pre-integration time, the post-integration time, the grading function and the delay required to be implemented. This information obtained from the console is stored in a pre-assigned memory area of the computer for controlling the various subsystems of the digital correlation receiver. The microcomputer is also designed to obtain the information, alternatively, from an input/output device, namely, the teletype unit.

That is, the option to control the correlation receiver either from the consple or from the teletype unit, has been built into the system.

The computer controls the following output devices in the real-time operation:

1) An incremental magnetic tape unit (MTU), Kennedy Model 1610, used for recording the final computed data. The data is stored on the tape for further processing, if any. An incremental magnetic tape unit was chosen for asynchronous data transfer from the FT system, to cater to a wide option of the number of data points and periodicity of the data sets.

2) A TV monitor ECIL Model 803, used as a graphic display terminal to give the brightness distribution map.

3) A digital printer, HP model 5055A, incorporated into the system. It is a slow device but gives a hard copy of the data flow at various subsystem levels. Hence the printer may be used as a debugging device.

In the off-line mode, the system has been designed:

1) To monitor the control console of the FT processor. The controls are set by means of thumbwheel switches. The computer has been designed to economically multiplex all the thumbwheel data settings through a single input

and output port.

2) To write the data in the phase correction memory, $\Delta\psi$-RAM. This data is obtained from the field calibration of some known strong sources.

3) To write an arbitrary grading function in any one of the two memories, the GI-RAM or G2-RAM. The grading function may be fed through the teletype unit or may be generated within the computer. In addition to these two memories for storing arbitrary grading functions, it may be recalled (ref. Chap.4) that there are four memories wherein fixed grading functions have been stored.

3) To set the control bits of the delay shift registers in the correlators as given in Chap. 3. The control bits for the E-W array and the various groups of the N-S array are obtained from a delay table, which is available from a dedicated memory area in the computer. The correlator receiver has been designed to operate with the least possible delay decorrelation for different zenith angle zones as discussed in Chap. 3. The total zenith angle range of $\pm 60^{\circ}$ is divided into 8 zones and the control bits for the delay shift registers have to be set differently for the various zenith angle zones.

In on-line operation of the computer, a fast data acquisition scheme in real-time is envisaged. The data from the Tmap-RAM of the FT processor is sequentially transferred to the internal memory area of the computer

at the end of each post-integration period. Faster operation is achieved by the design of a direct memory access (DMA) mode of data transfer. The data block contains a header of a fixed number of bytes (16) giving the console settings. This will enable data identification at the time of its retrieval from the magnetic tape for further processing.

An important feature of the design involves addressing the data buffer register of the alphanumeric (AN) display and the graphic memory systems of the TV interface circuit as extended memory locations of the computer. This avoids output port expansion and the hardware design feature gives faster communication with the TV interface unit. In such a design it is necessary to employ high speed logic circuitry with a good drive capability.

Some amount of data processing has been incorporated in the software to convert the computed 16 bit brightness distribution values to give 16 grey levels (4 bit) on a black and white TV monitor. A simple algorithm for the 4 bit conversion is implemented.

Further processing of the data can be done by expanding the memory size of the system. This will,

however, limit the on-line data acquisiton speed in real-time operation.

Fig 5.1 gives the block schematic of the computer system with the necessary interface units to drive various peripheral units. Fig 5.2 gives the program flow chart for all the segments of the software. Appendix-5 gives the details of the microprocessor.

5.2 System design of the microcomputer

5.2.1 System hardware

5.2.1.1 Interface unit for the Control Console

For the processing of the received data, information such as the range of beams, the pre-integration and the post-integration times, values of the delays and the grading function to be employed, is required. This information may be supplied to the system by means of thumbwheel switches available for this purpose in the control console. The interface unit of the micro-computer has, therefore, been designed to retrieve the information at the beginning of the data processing, and to supply it to the appropriate subsystems of the receiver. Processing of the data results in the brightness distribution values corresponding to various

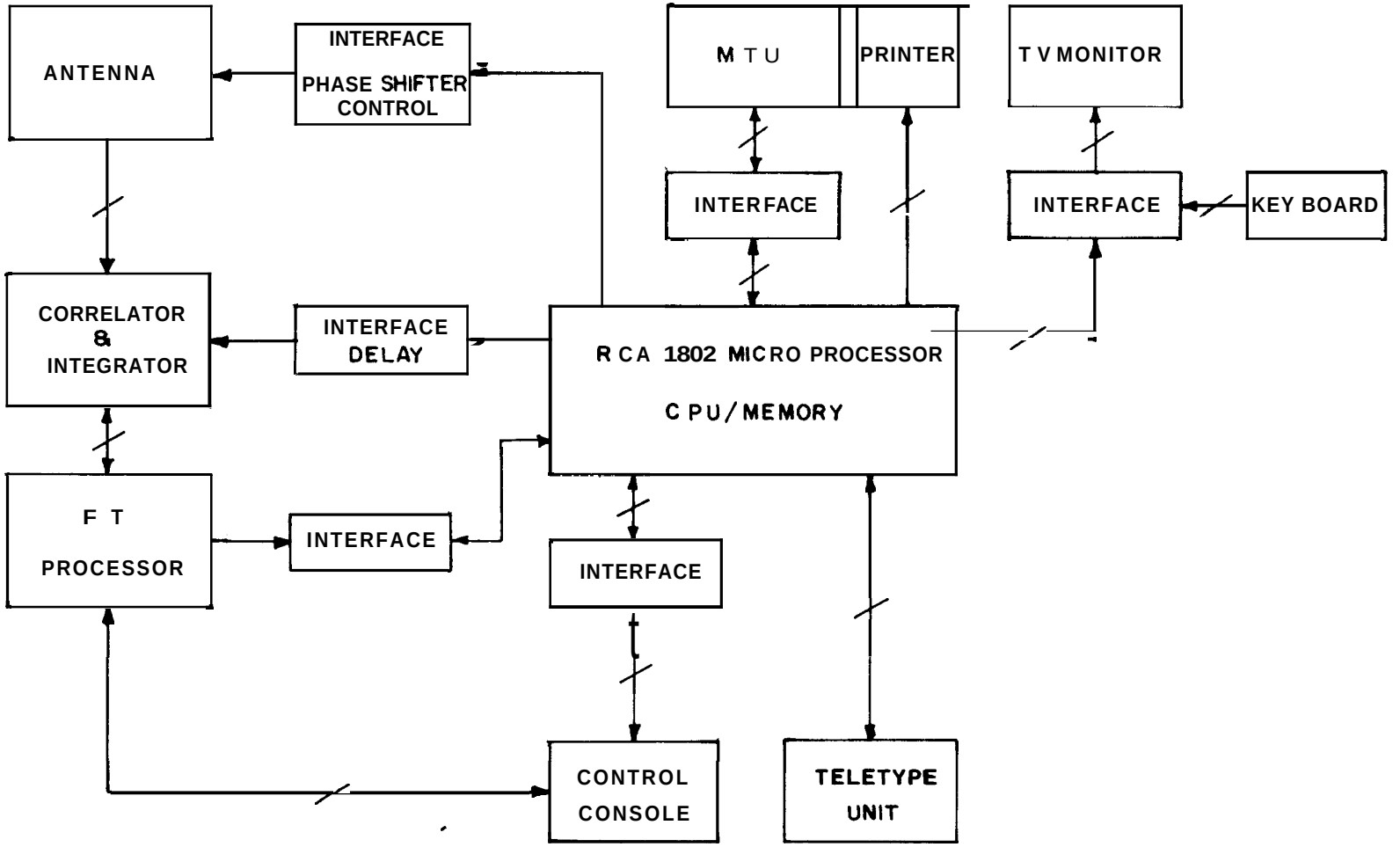


FIG. **5.1** MICROCOMPUTER SYSTEM.

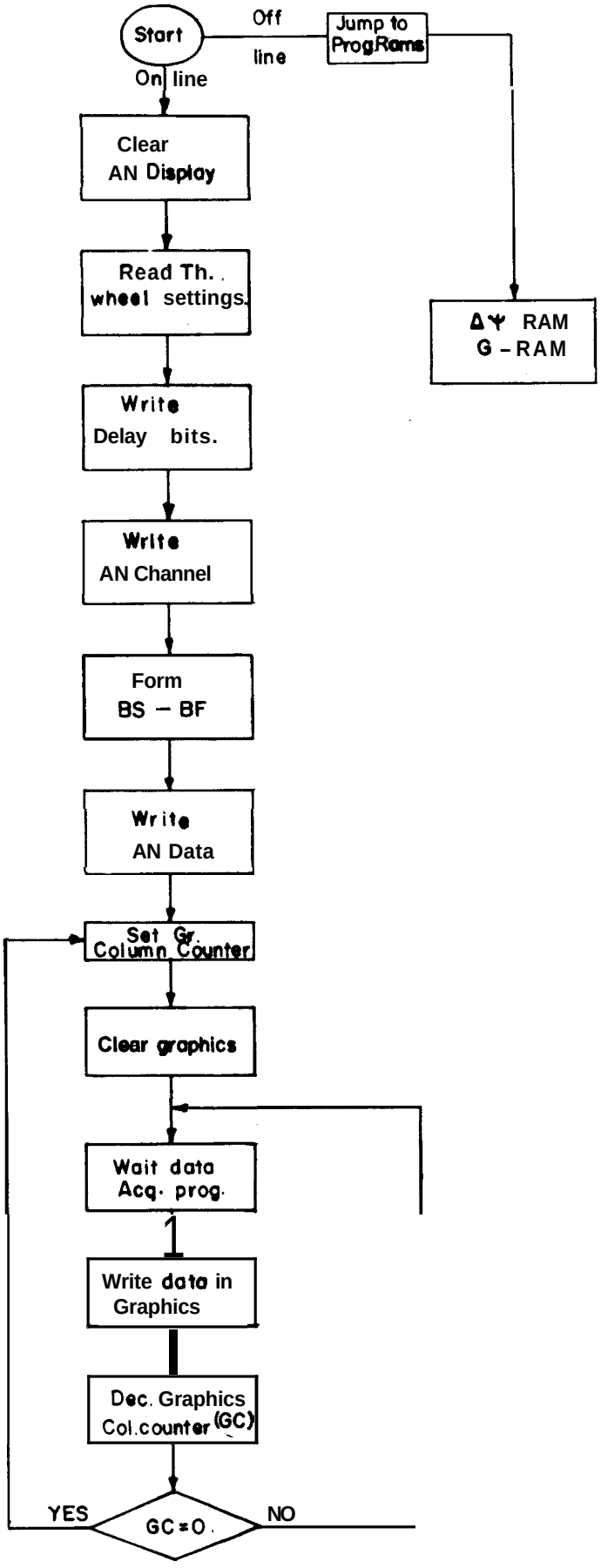


FIG. 5.2 FLOW CHART OF THE SOFTWARE SCHEMATIC.

beams and is displayed as a column of points on the graphic display. The 'BEAM-START' and the 'BEAN-FINIS2' settings on the console give the number of beams to be computed, and controls the display area on the graphic display of the TV monitor.

There are in all 16 octal digits for the console settings. These are grouped into bytes taking two octal digits in one byte and are multiplexed through an 8-channel multiplexer to the input of the micro-computer. The control for the channel selection of the multiplexer is generated by the software of the micro-computer and is given at the output port. After suitable delay for data setting up time of the multiplexer, the thumbwheel data is taken through the input port to the specified location in the memory under software control.

5.2.1.2 RAM Data Entry Module

The field calibration of the receiver is done by observing some strong sources, whose positions in the sky are accurately known. The phase errors of the N-S elements are thus determined. The phase correction data so obtained is stored in the off-line mode, in the phase correction memory, the $\Delta\Psi$-RAM, and the correction

is applied on the measured correlation co-efficients before Fourier transforming as discussed in Chap. 4.

5.2.1.3 Interface Unit for the Delay System

As already discussed, in order to keep the delay decorrelation within acceptable limits, the signals from the E-W and the N-S array are delay compensated before correlation. 6 bytes of data are required for each of the eight zones in the zenith angle range (-60^{o} to $+60^{o}$) to set the control bits of the delay shift registers in all the 23 groups of the N-S elements and one E-W channel. This data is obtained from a look-up table located in a reserved area of the memory in the microcomputer. In the initialising process of the receiver, the microcomputer system demultiplexes the 6 byte data and groups in the control bits to set the required delay in the 23 groups of N-S elements and one E-W channel.

5.2.1.4 Interface Unit for the MTU

The FT processor issues a "TAPE TRIGGER" pulse after the integration of as many data sets as given by the "Post-integration Multiplier" setting

for each beam. On the receipt of TAPE–TRIGGER pulse, data string of all the beams from BEAM–START to BEAM–FINISH, having a word length of 16 bits for each beam, is transferred from the Tmap - RAM of the FT processor to the MTU and to the TV interface unit. The "DATA READY PULSE" is issued from the FT processor for each beam when the data from the Tmap - RAM is available at the data bus. The TAPE TRIGGER pulse and the DATA READY PULSE form the control signals for initiating data transfer under DMA mode. As the microprocessor is an 8 bit version, the computed data of 16 bit length pertaining to each beam is multiplexed into 2 bytes for further handling.

Since the receiver has a wide choice for control settings, specially in the integration time and the number of beams, the computed data output is not at a regular rate. An asynchronous data transfer is the only choice in such a situation. An incremental MTU was therefore chosen.

The DATA READY pulse is issued once in 256 μs which is the time for computing the brightness for each beam from the correlation coefficients a_ns and b_ns. Hence, two bytes of data pertaining to

each beam have to be transferred in about 1/4 ms. The MTU is a slow device accepting the data at a maximum rate of 500 bytes per second, For on-line operation, the MTU is thus 16 times slower than the maximum possible data generation rate. However, by choosing a smaller number of beams for a given pre-integration time or by choosing a larger post-integration multiplier, the data can be transferred without overflow,

5.2.1.5 Interface Unit for the TV Monitor

The on-line processed data is presented on a TV monitor to display the two-dimensional sky brightness distribution map. The computed brightness of a beam (for a particular declination) modulates the intensity of the corresponding point on the 256 point display column. It may be pointed out that a maximum of only 256 points can be displayed in a column on the graphic display of the TV screen. Therefore, if the thumbwheel setting requires the entire declination range to be covered (512 beam positions), the software is designed to choose alternate beams for the display. Further, the software is designed also to convert the 16 bit brightness to 16 grey levels (4 bits) of the intensity of the display,

The console settings of the receiver are also displayed in alphanumeric form on a part of the TV screen. Matrox Video-RAM (MTX-1632SL) and the Graphics Module (MTX-256) are used for generating the alphanumeric (AN) characters and the graphic display, respectively. APPENDICES 7 and 8 give the salient features of these modules. To facilitate the cursor control in the off-line data entry on the AN display and to clear the AN memory, a local! edit mode for the AN display is used. The keyboard data entry interface has been designed to write any ASCII characters on the display.

5.2.2 System Software

Fig. 5.2 gives the schematic of the software of the microcomputer system. In the off-line mode, the data is written into the memories $\Delta\psi$-RAM and G-RAMs as already discussed earlier. In the on-line mode, after initialisation, the AN display is cleared by writing blank in each location of the AN memory comprising 16 X 32 characters. Then the control console is read and the data corresponding to the thumbwheel settings are stored in the allocated memory to display on the right top corner of the TV monitor. Depending on the delay zone selected, the delay buffer

connected to the front end system is loaded with 6 bytes of the control data taken from the delay look-up table. Then the titles "BEAM START", "BEAM FINISH", etc., of the control information of the system are written on the TV monitor.

The start and the stop points on the graphic column counter have to be determined from the BEAM START and the BEAM FINISH thumbwheel switches on the console. The LSB of the converted 9 bit data of each of the above thumbwheel switches is dropped leaving 2 bytes of data corresponding to BEAM START and BEAM FINISH to be stored in the specified locations.

Then the data of AN display corresponding to the thumbwheel settings of various control information is written. Now the horizontal position of the graphic row counter is set, thereby the cursor is at the right column of the graphic display. . The software control then clears the graphic memory and waits for the data acquisition. The FT processor signals the computer after the computation and the data is transferred from the Tmap-RAM of the FT processor to the computer memory in the DMA mode. The data thus obtained is written on the MTU, byte by byte in the incremental mode. Then, the data after conversion

is written into the graphic memory which is displayed as a column of grey level dots and the graphic column counter is decremented. The computer waits in the data acquisition mode for the next cycle of operation. Once the column counter is decremented to zero, the graphic display is cleared. A hard copy of the display before clearing the screen can be taken by operating the video hard copy unit.

5.3 Detailed Circuit Design

5.3.1 Interface Unit for the Control Console

Fig. 5.3 gives the schematic diagram of microprocessor interface circuit. Thumbwheel switches in the control console are read and stored in specified locations by software control. 48 bits (6 bytes) of information pertaining to BEAM START etc, is multiplexed through eight channel multiplexers. The control for channel select is generated in the microcomputer and given as data output through the output port. After suitable delay for the data settling time of the multiplexer, data from the thumbwheel switches are taken on the data bus to the specified locations through the input port under software control. Fig. 5.4 gives the input and output port connections to the microprocessor along with the timing diagrams. The $\overline{MRD}$ signal of the

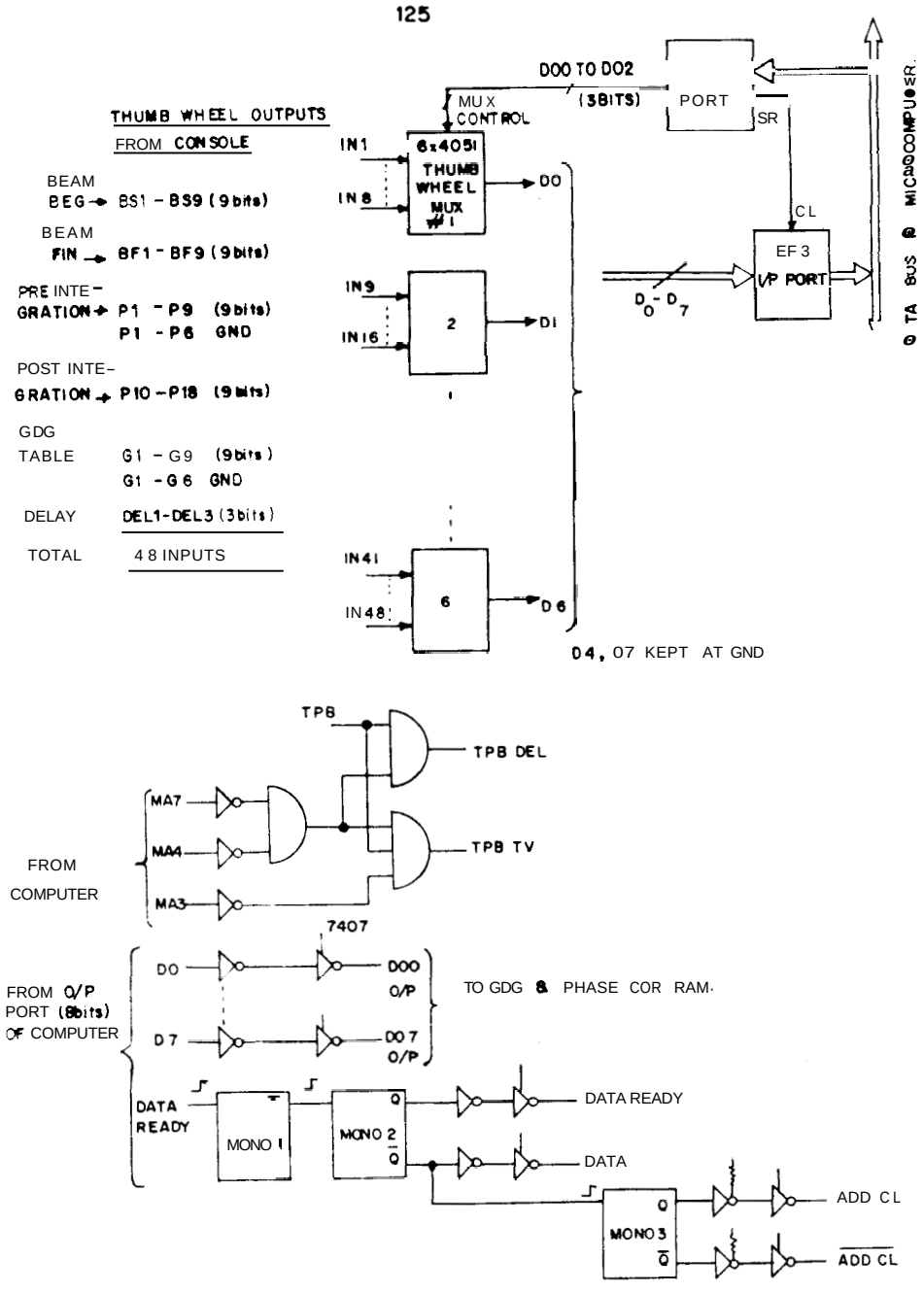


FIG. 5.3. BLOCK SCHEMATIC OF MICROPROCESSOR INTERFACE (MPI-II)

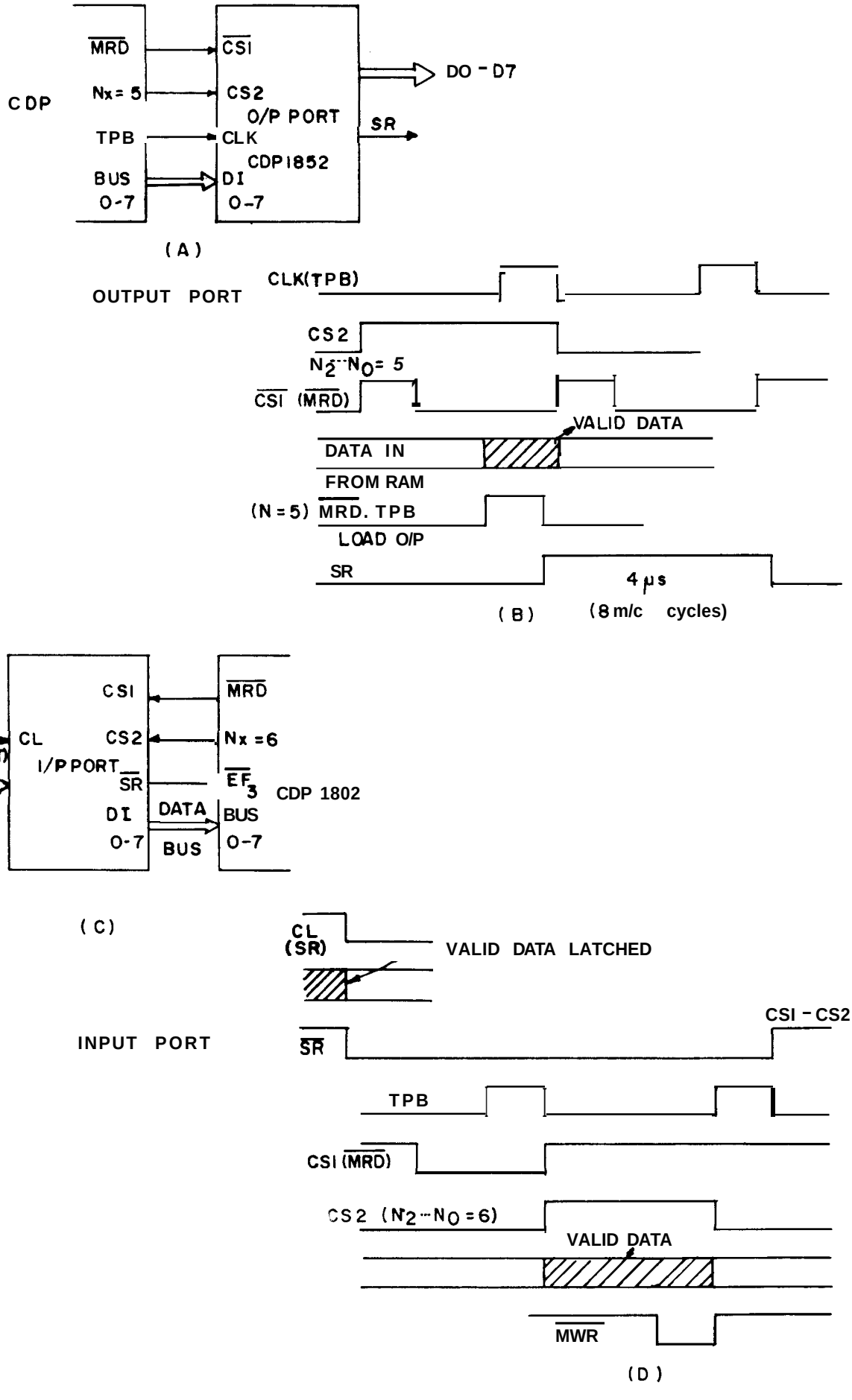


FIG.5.4. INPUT/OUTPUT PORT CONNECTIONS.

microprocessor is connected to the controlpin $\overline{CS1}$ of the output port. The output port is hardwired for decoding Nx set to 5 and connected to the control pin of CS2 of the output port. The data is latched into the output when $\overline{CS1}$, CS2 and CLK (TPB) pulses are all true as shown in the timing diagram of the figure. The service request signal, SR, in the output port is generated at the termination of the function $\overline{CS1}$.CS2 and will be held true until the following high-to-low-level transition of the CLK pulse. This pulse is 4 µs long with the present operation of computer at a clock frequency of 2 MHz. The output drivers of the output port are always enabled.

The SR signal is connected to the clock input of the input port. The high-to-low level transition of the SR signal, sets the service request flip-flop in the input port and latches the data in the input register. The $\overline{SR}$ output of the input port is used to signal the microprocessor, by connecting it to the input $\overline{EF3}$ flag of the processor. The software in the system tests for this flag and once it senses the setting of this flag, the program proceeds with an input instruction. The input port is decoded for Nx set to 6 and connected to the CS2 pin of the input port. When CS1 ($\overline{MRD}$) and CS2 are true, the

three state output drivers of the input port are enabled. The $\overline{MWR}$ pulse writes the valid data from the data bus into the location specified under the program control. The service request flip-flop in the input port is reset at the negative edge of CS1.CS2 pulse thereby keeping the flip-flop ready for the next input cycle.

Fig. 5.5 gives the schematic of the software for reading all the thwnbwheels in the console. Register 9 is a memory pointer for storing thwnbwheels values in a sequential order. Register C is an address counter, the data of which is used as the address control of the thumbwheel multiplexer (Pig. 5.3) and Register B is used as an index register. The thumbwheel switches operate in octal mode and hence the data from two switches are read as one byte with 4th and 8th bit set as zero. This is decoded into two bytes by first reading the 3 LSB bits of the multiplexed data as one byte, by ANDing the data with 07 and storing the result in one location. Next the multiplexed data is right shifted by 4 bits and again ANDed with 07 and stored in the following location. Thus each thumbwheel data is stored as a separate byte in the memory.

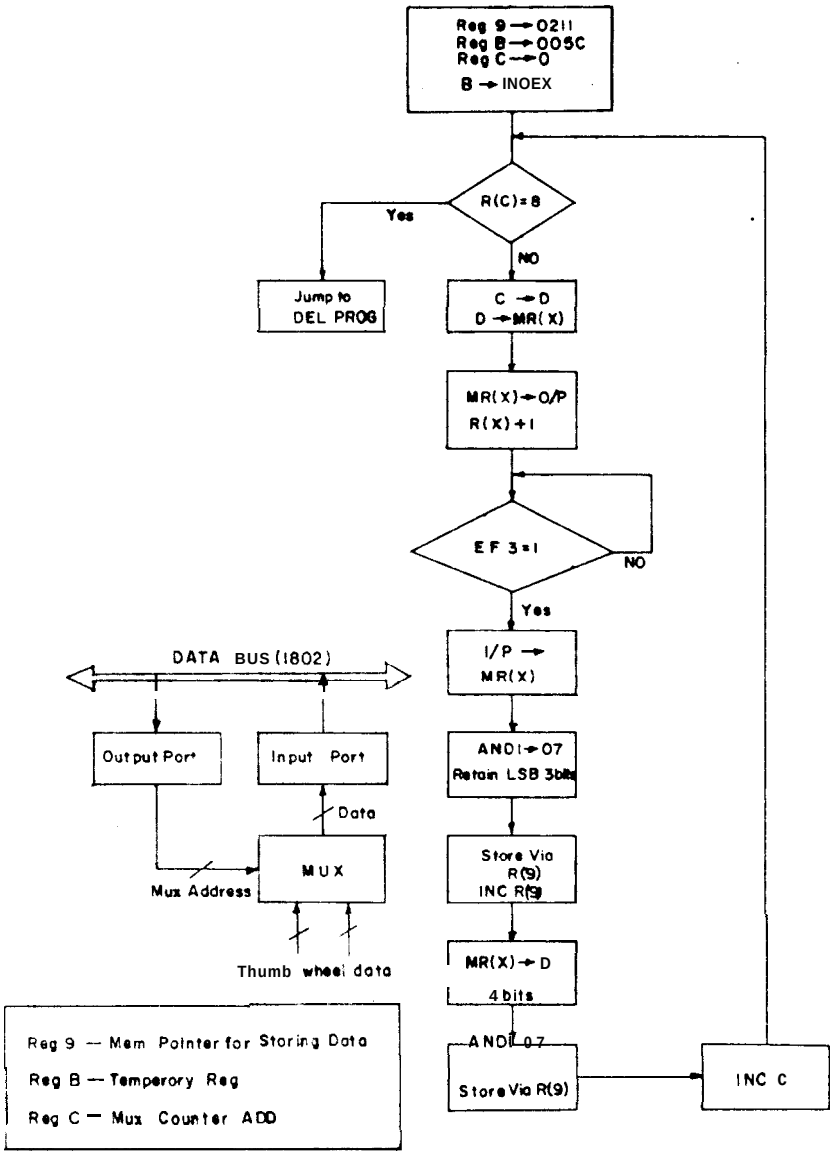


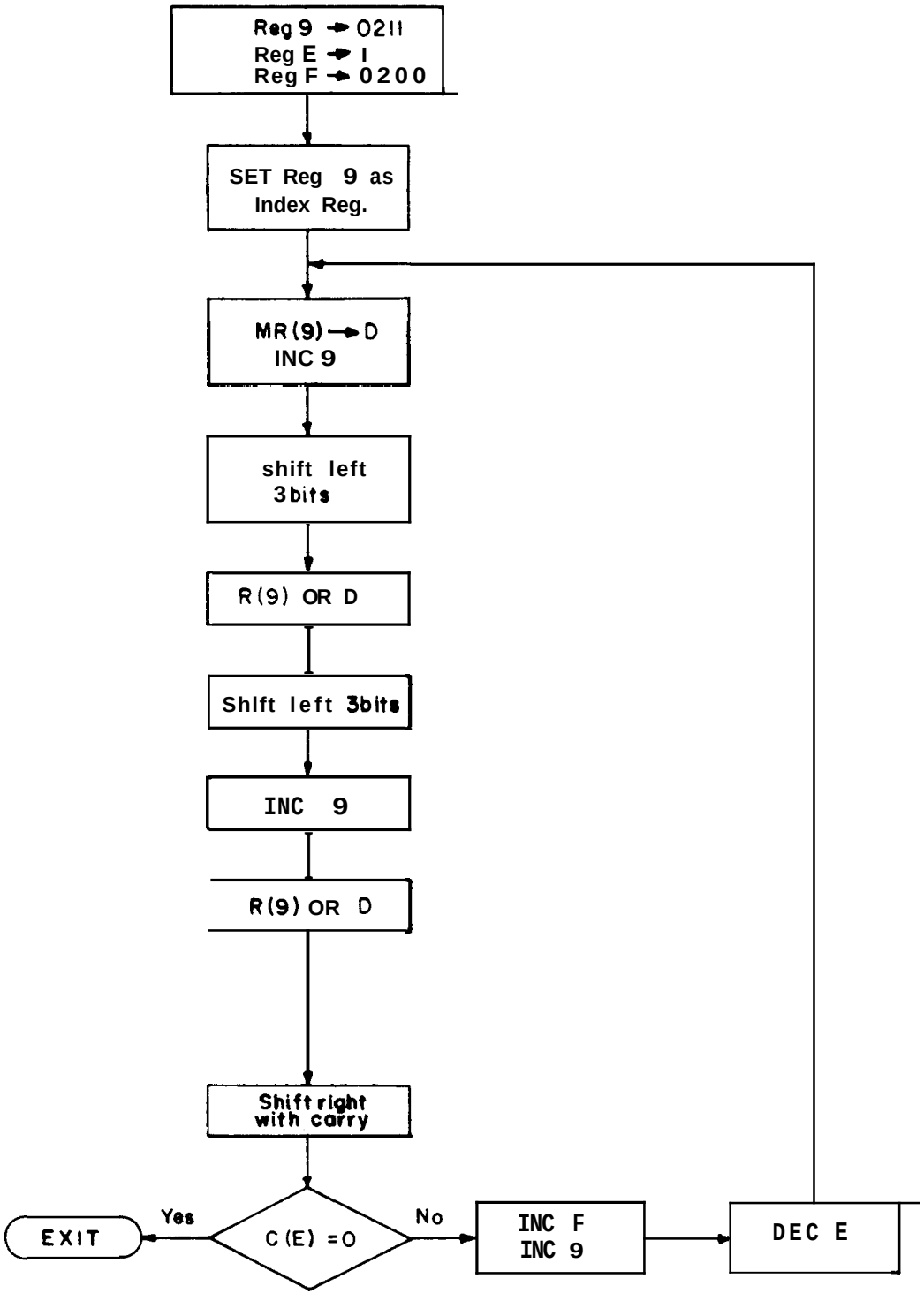
FIG. 5.5 FLOW CHART FOR WRITING THUMB WHEEL SETTINGS

Because of limitation of memory in the graphics display, only 256 points are displayed even though the brightness is computed for 512 points. Every alternate point is displayed. Only 8 MSB bits are retained in both the BEAM START and BEAM FINISH data. Fig. 5.6 gives program for converting thumbwheel data (9 bits) corresponding to BEAM START and BEAM FINISH data, to 8 bits.

5.3.2 RAM Data Entry Module

Data entry into the $\Delta\psi$ -RAM, and G-RAM, is done OFF line. Fig. 5.7 gives the block schematic of the circuit employed. The data from the output port of the computer is gated to the data bus of the RAMs. A service request signal, SR, from the output port is used to generate the write pulse for the RAMs and to advance their addresses.

MONO-4 gives a 1 μs delay for data settling time in the output port, and MONO-5 generates a 1 μs write pulse for the RAM. The pulse is level shifted to 12V, and applied to the RAM driving circuitry in the FT processor unit. The $\overline{Q}$ output of MONO-5 is used to trigger the MONO-6 circuit, which in turn generates a 1 μs ADD-CL pulse to advance the



Reg.9 — Mem pointr for thumbwheol data
Reg F — Mom pointer for BS & BF
Reg E — Temp. Reg.

FIG.5.6. FLOW CHART FOR GETTING BS & BF FROM THUMBWHEEL DATA.

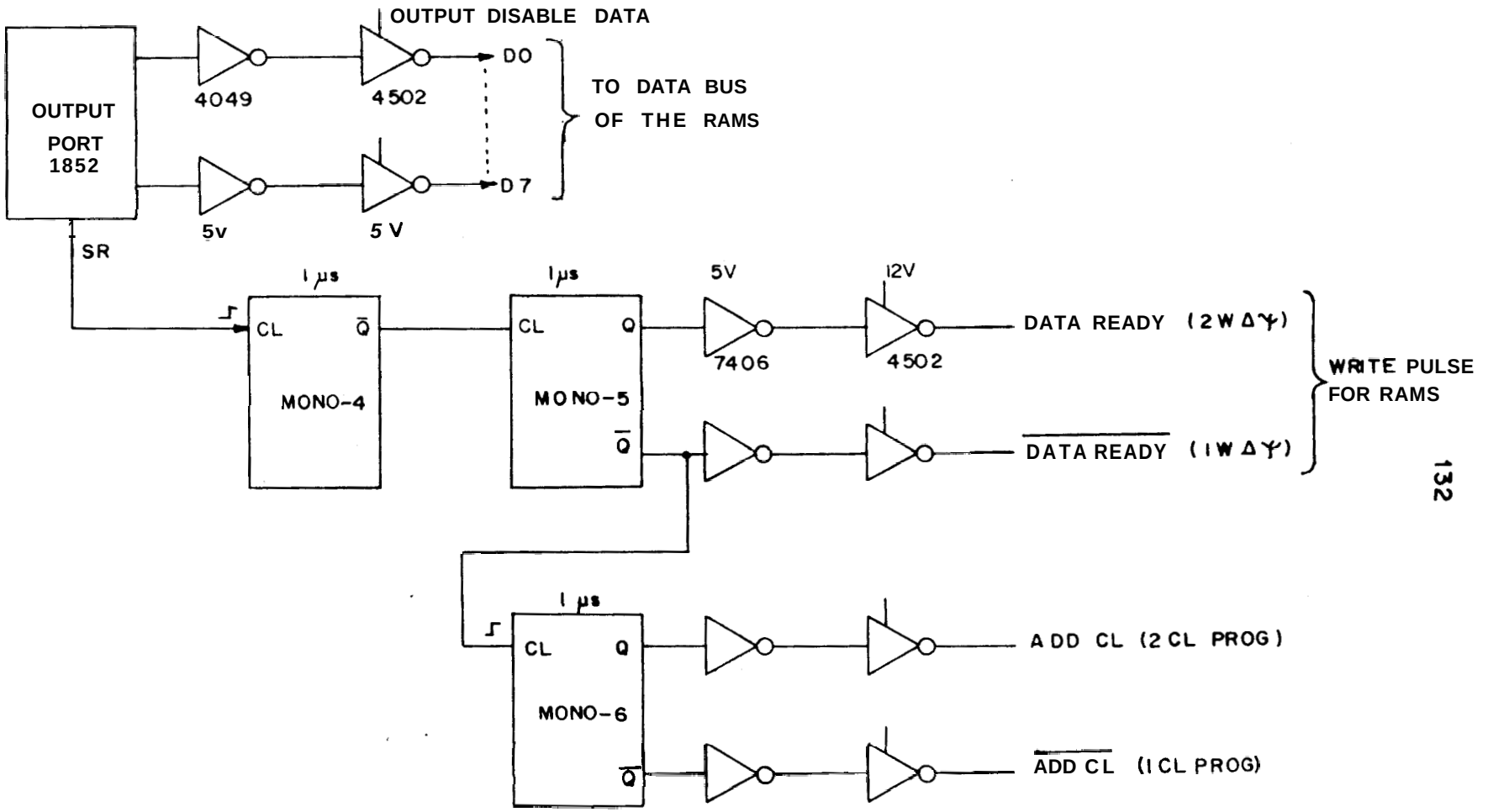


FIG.5.7 .BLOCK SCHEMATIC OF RAM DATA ENTRY MODULE.

address counter in the FT processor system in manual setting of the address generator. A switch is provided to set the address manually in the console. Data is written into either the $\Delta\psi$-RAM or the G-RAM selected from the console. Write and chip select signals are appropriately chosen. Data is fed either through paper tape or the keyboard of TTY.

Fig. 5.8 gives the software schematic for writing data into RAMs. Register D is set as the Index register and is the data pointer from where 128 bytes of data are stored initially to be transferred into the RAM. Register C is the address counter which transfers 128 bytes of data. Write and CS pulses for the RAM are generated whenever output instruction is executed as described earlier.

In case the same data has to be written in all the memory locations of the RAM, the above program is slightly modified as shown in the figure. Consider data zero is to be written in all the locations of RAM. Here zero is written in the start location, that is in the location 0780 and the Index register is decremented after the output instruction. With this operation, the memory pointer for the data is not incremented and zero will be written in all the

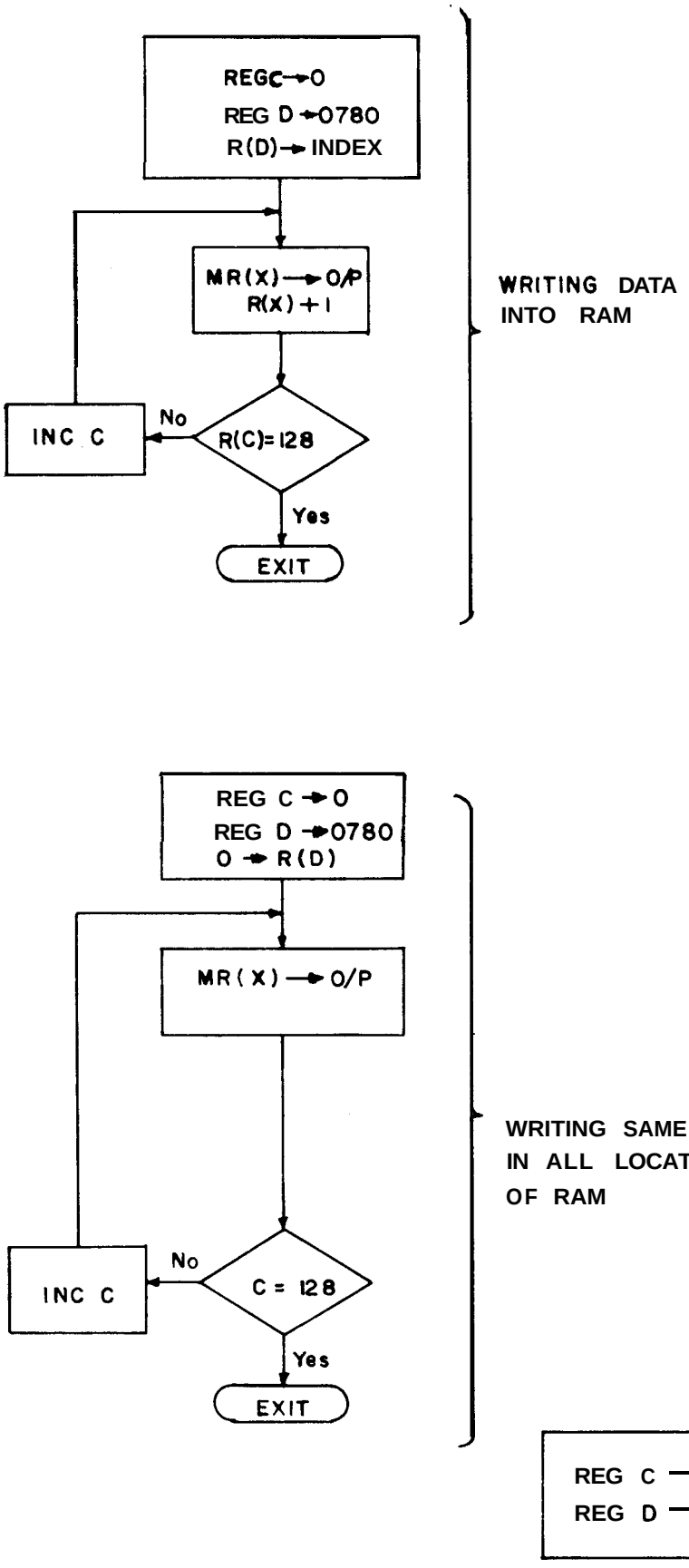


FIG. 5.8 FLOW CHART FOR WRITING DATA INTO ΔY-RAM & G-RAM.

locations of the RAM. The need for putting in zero arises only in testing and debugging the system.

5.3.3 Interface Unit for the Delay System

It may be recalled (ref. Chap. 3) that delay is introduced in all the N–S channels and the E–W channel to compensate for the path differences for sources at different declinations. The 90 N-S elements are divided into 23 groups each of 4 N–S elements. 2 control bits are required to control the delay in each group, thereby requiring 48 bits (6 bytes) for all the N–S and E–W channels. Provision has been made in the delay buffer for 32 groups in the N–S and 1 group in the E–W for future expansion of the system. Fig. 5.9 gives the block schematic diagram of the interface unit for the delay system. Since there are 32 groups and each requires 2 bits Xn, Yn, alternate data bits of first eight bytes are grouped as X1 to X32 and Y1 to Y32 respectively and brought out to the delay buffer unit. The ninth byte corresponding to the control delay bits of the E–W element is designated as Z1 to 28.

There are in all eight settings corresponding to the eight delay zones in the declination range of

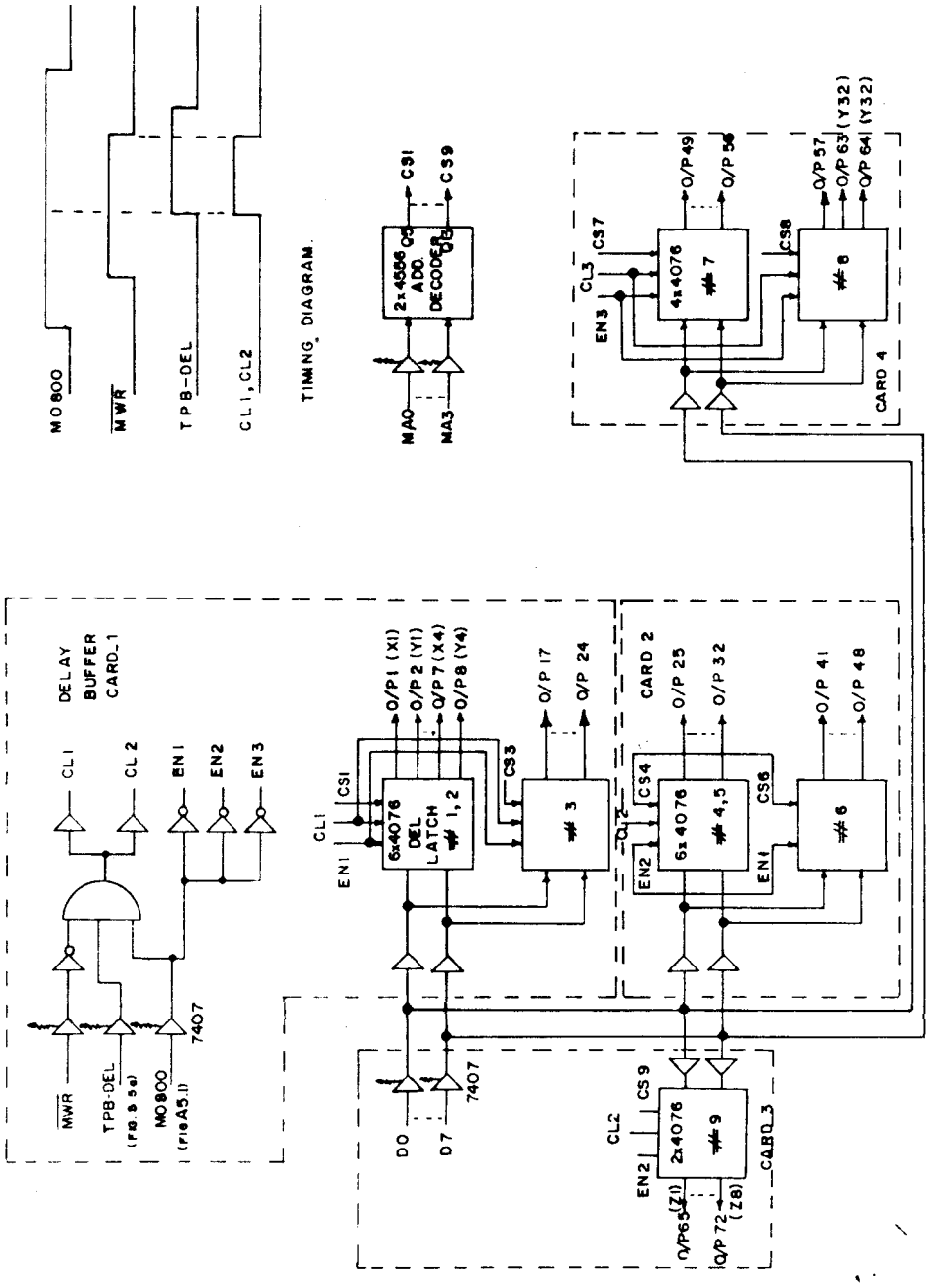


FIG.5.9. BLOCK SCHEMATIC OF DELAY BUFFER.

$\pm 60^{\circ}$ (Ref. Chap. 3). The nine bytes of data pertaining to any particular zone is stored in the latch circuits formed by 4 bit CMOS chips, 4076, as shown in the figure. These latch circuits are addressed as locations in the memory, thereby avoiding output ports. Memory reference instructions are sufficient to load these latch circuits. $\overline{\text{MWR}}$ and TPB-DEL pulses are used along with the decoding of memory address lines to latch the data by controlling the clock and enable signals as shown in the diagram.

The address decoder uses two chips (4556), to decode the address lines MA0-MA3 to give the signals CS1 to CS9. These signals are used to control 9 latches of one byte each. The TPB-DEL pulse is issued after gating the decoded output of MA4-MA7 address lines and TPB pulse of the processor (Ref. Fig. 5.3). M0800 signal is the decoded address Pine which goes as the EN signal for selecting the delay buffer from location 0800 onwards (Ref. Fig. A5.1(a)).

The timing diagram in the figure shows the generation of clock pulses which go to different delay buffer chips. Because of the lengths of cable

(about 3 metres) from the computer to the interface unit for the delay system, the control and data signals are buffered sufficiently. Shift registers for providing the delay operate on 12V supply, while the microcomputer operates on 5V. The delay buffer is designed to operate at 12V and hence the control and data bits are level shifted at the input, thereby avoiding level shifting at the multibit output of the delay buffer unit. An open collector TTL buffer, 7407, is used for level conversion with very small propagation delays.

Fig. 5.10 gives the flow chart for loading the delay buffer corresponding to the delay zone selected. 72 bytes of control data corresponding to 8 delay zones are stored from location 0735 as shown in the Fig. 5.10. The delay zone specified by the thumbwheel on the console is stored in location 0220. Register B is initially set to point to this memory location. Register C is set with a constant 9 and Register 8 is set to 0805 to point the delay buffer latch (Fig 5.9). Memory address 0805 to 080D refers to the 9 byte latch in the delay buffer unit. Register D is the memory pointer for obtaining the data corresponding to the delay zone selected. The memory location to be

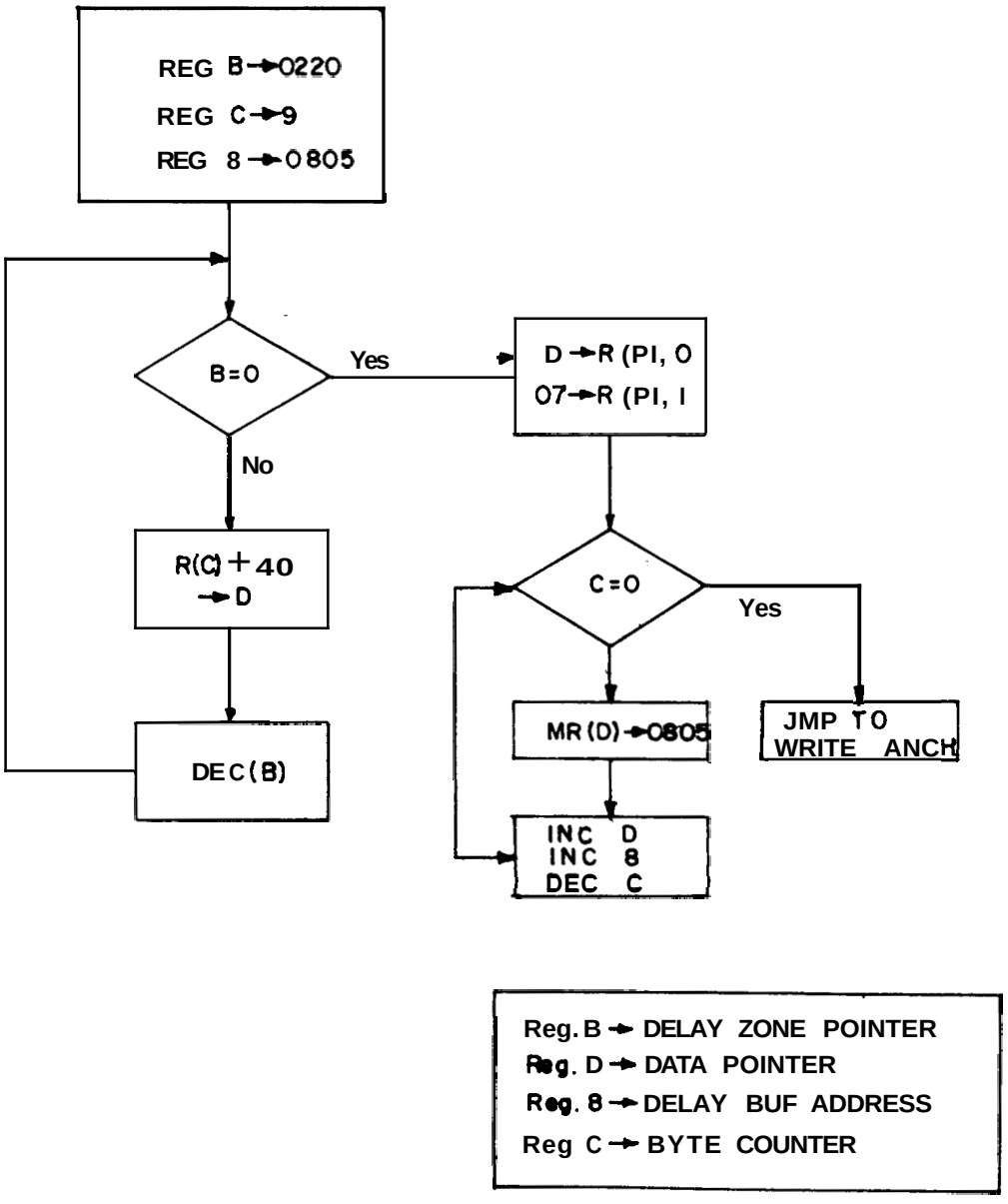


FIG. 5.10 FLOW CHART FOR WRITING DELAY BITS IN THE BUFFER.

pointed is computed from the delay zone setting on the console. The delay zone selected (a number from 0 to 7) is multiplied by 9 and added with 35 to give the lower order byte in the Register D, and 07 is stored in the higher order byte. Thus Register D points to the memory location corresponding to the control data pertaining to the particular delay zone. 9 bytes of data following the memory location pointed by Register D are stored in locations 0805 onwards in the delay buffer unit.

5.3.4 Interface Unit for the MTU

Fig. 5.11 gives the schematic diagram of the MTU interface unit and Fig. 5.12 gives the timing diagram.

The flip-flop, FF1, is reset by setting the Q output of CPU which is hardwired to reset FF1. The data from the processor unit (Dl–16) is strobed by the rising edge of the $\overline{\text{CSBC}}$ pulse of the processor unit into the input latch circuit at the end of the integration period. The $\overline{\text{CSBC}}$ pulse also sets FF1, registering EF1 request. The microprocessor software, after initialising, will be in the wait state looking for the setting up of flag EF1.

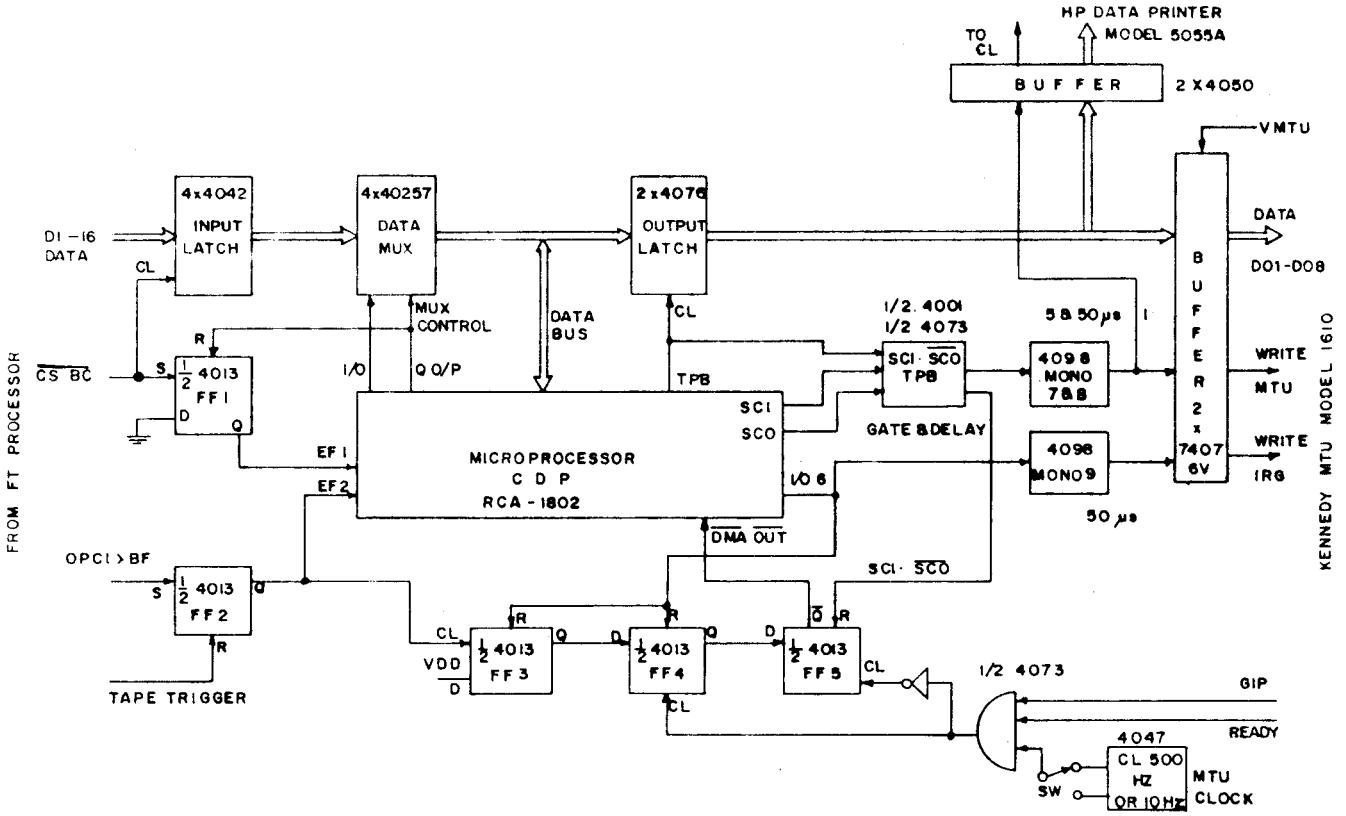


FIG. 5.11. BLOCK SCHEMATIC FOR MTU INTERFACE UNIT. (MPI-1)

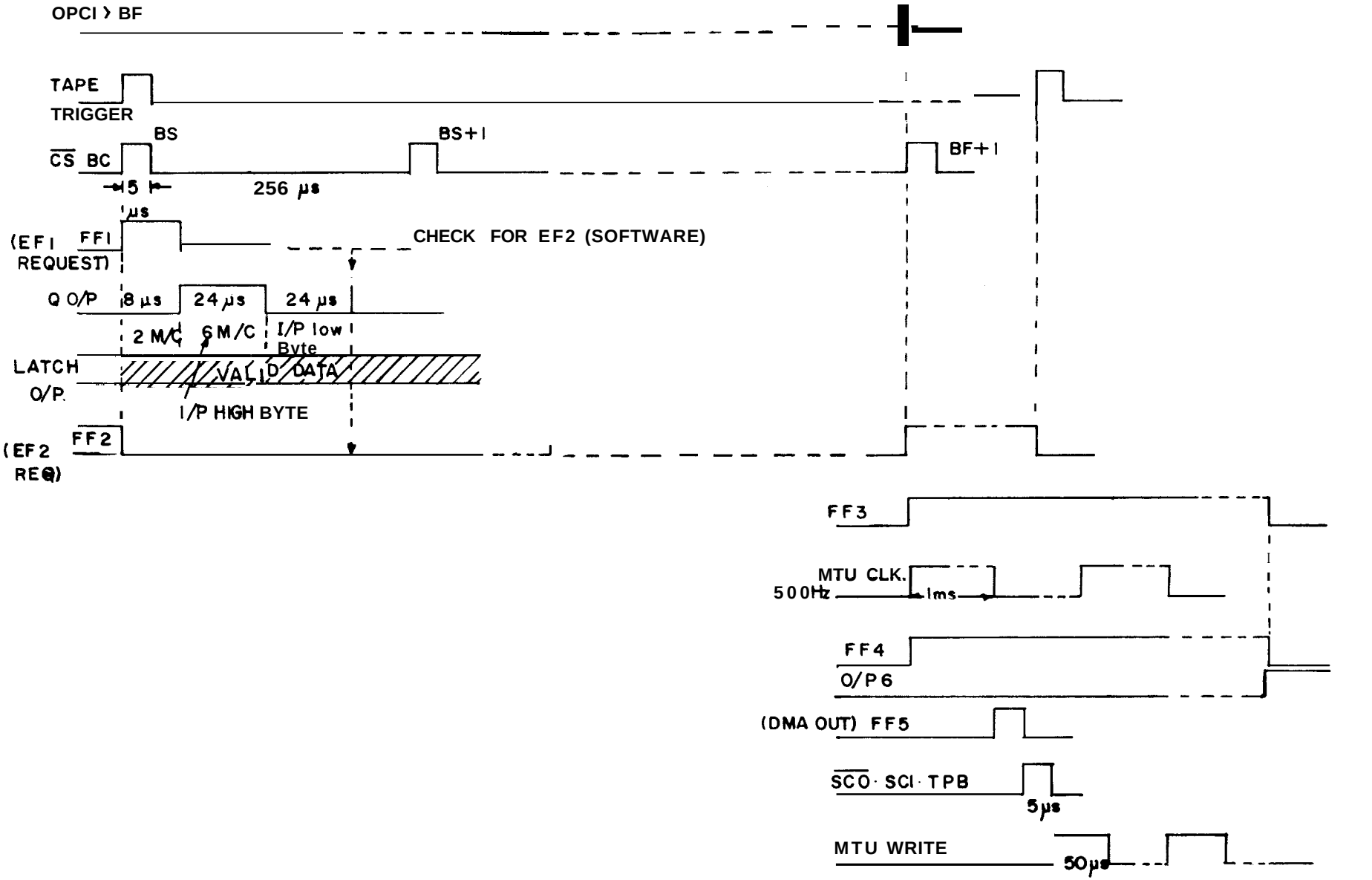


FIG.5.12.TIMING DIAGRAM FOR MTU INTERFACE UNIT (MPI-I)

The computer then inputs the data of 16 bits pertaining to each beam into 2 bytes from the specified location in the memory and keeps count of number of bytes transferred. 8 μs (executing 2 m/c cycle instructions) after EF1 request, the high byte of data is transferred. Q output from the processor resets FF1. After 24 us (executing 6 m/c cycle instructions), the low byte of data is transferred (Ref. timing diagrams in APPENDIX 5). Program looks for EF2 request, which is set after the dumping operation is over. This flag is set up by the flip-flop, FF2, on the rising edge of the signal, OPC1 > BF. This signal is issued at the end of the post-integration time when processing for all the beams is completed. Once the EF2 flag is sensed, the processor puts out the data at the rate of the writing speed of the MTU in the DMA mode of transfer.

The Q output of EF2 also sets up the flip-flop, FF3, which enables the setting up of another flip-flop, FF4, at the rising edge of the MTU clock operating at 500 Hz. After sensing EF2 flag, $\overline{\text{DMA OUT}}$ request signal to the processor is generated from the flip-flop, FF5, only after one ms after setting FF4, in the following falling edge of the MTU clock to

allow the processor to come to the DMA mode of transfer. The MTU clock is issued for DMA operation only after ascertaining that the gap in process signal, GIP, and 'READY' signal from MTU are proper.

The DMA request initiates S2 state in the processor (Fig. A5.2) which is sensed in the interface unit and generates control signals to transfer data to MTU. The data from the processor bus is strobed into the output latch by the timing pulse generated by the signal, $\overline{SCO}$.SCI.TPB. The *WRITE' 'pulse of 50 µs duration is generated after giving 5 µs data settling time in the output latch, After transferring all the bytes to MTU, output instruction in the processor is executed to generate the record gap in the MTU. A separate counter in the processor keeps track of the number of bytes kept in memory to be transferred onto the MTU. Each record in the MTU contains console setting details and actual data computed for all the beam settings. The locations 0202 to 0210 are kept free in the memory for later expansion of the console settings.

The data and the control signals for the MTU are all level shifted to 6V by using open collector buffers, 7407, and energised by the 6V supply provided

by the MTU unit, in order to meet the MTU specifications. The unshifted data and the control signals operating at 5V are given through a buffer to a low speed recorder, for debugging purposes. In this case, the MTU clock is changed from 500 Hz to 10 Hz by an external switch control. The recorder is used only as the hardcopy facility for the data written in MTU, since write only MTU cannot be read in the field. This recording facility will aid in fault localising etc,

Fig. 5.13 gives the flow chart of the program for data acquisition from the FT processor and transferring the data onto the MTU. Register 2, is used as Index register and as memory pointer to input the 16 bit word from the FT processor as 2 byte data, The data is stored from location 0221 onwards in the memory. Register 3 is a byte counter which keeps account of the number of bytes to be transferred to the MTU. This register is preset with the number (16) corresponding to the number of bytes in the header pertaining to the details of the console settings, eg: BEAM START, BEAM FINISH, etc. Once data acquisition is complete, this register is decremented while transferring data to the MTU through DMA operation, Register 0 is used as the DMA pointer.

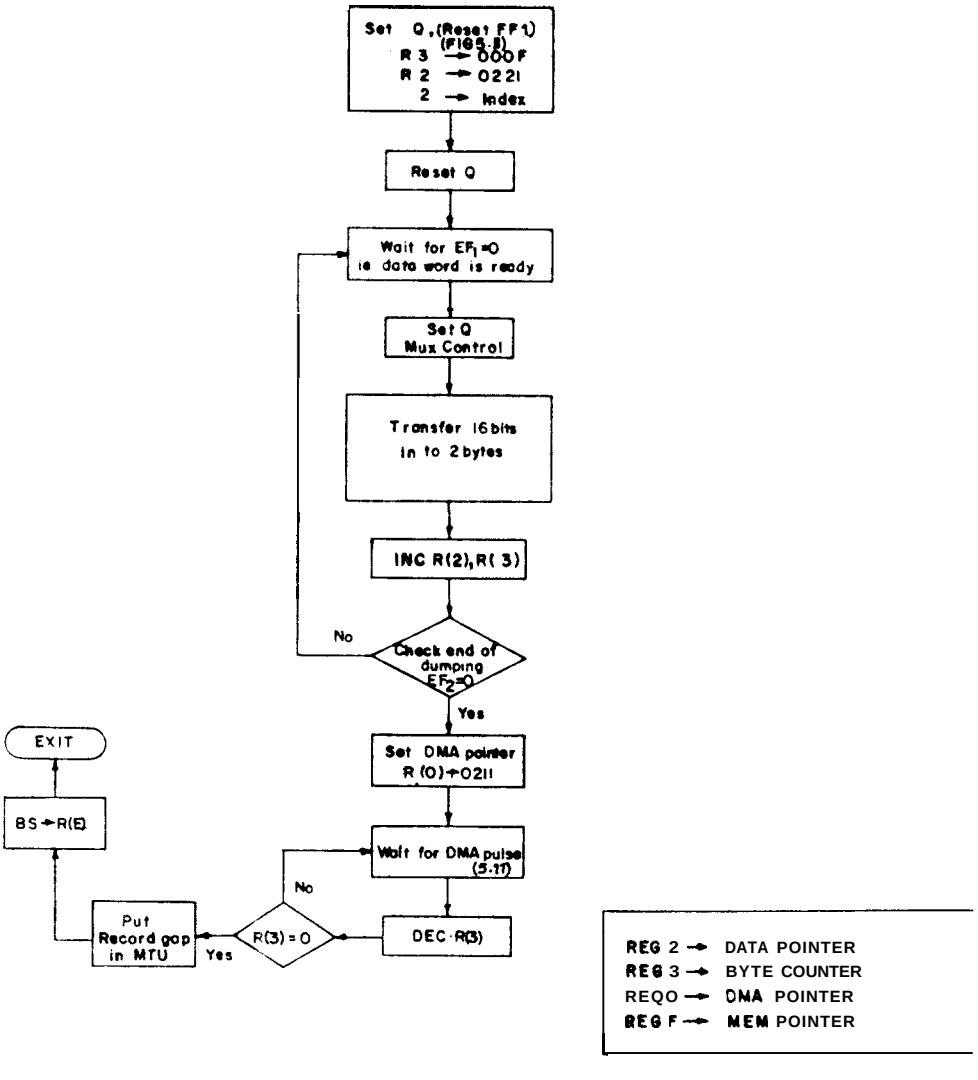


FIG. 5.13 FLOW CHART FOR
DATA ACQUISITION & MTU TRANSFER

5.3.5 Interface Unit for the TV Monitor

Fig. 5.14 gives a block schematic of the TV interface unit for keyboard control. The write signal, R/W AN, of 500 ns width and the chip select signals, CS AN, of 1.2 μs for the alphanumeric module are generated as shown in the figure to meet the timing requirements of the AN module given in APPENDIX 7. MONO-1 allows the settling time for the data from the TV keyboard to be strobed into the data latch. The data signals go through a gated latch circuit to the data bus of the AN module. MONOs 2 to 4, and the flip-flop, FF1, generate R/W AN and CS AN pulses as per the timing diagram shown. MONO-2 provides a delay of 400 ns for CS AN to provide write-set-up-time, t_{CSW} (240 ns minimum). MONO-4 provides a delay of 300 ns pulse for chip-select-hold-time, t_{CSH} (75 ns minimum), after R/W AN. The write pulse width, t_{WP}, of 500 ns (250 ns minimum) is provided by the Q output of MONO-3. CS AN pulse is provided by FF1 which is set by the rising edge of MONO-2, and reset by the falling edge of MONO-4. The R/W AN and CSAN pulses can be initiated by one of the following pulses:

1. Clear pulse from the keyboard,
2. Strobe signal from the keyboard, and
3. R/W AN-MP pulse from the microprocessor

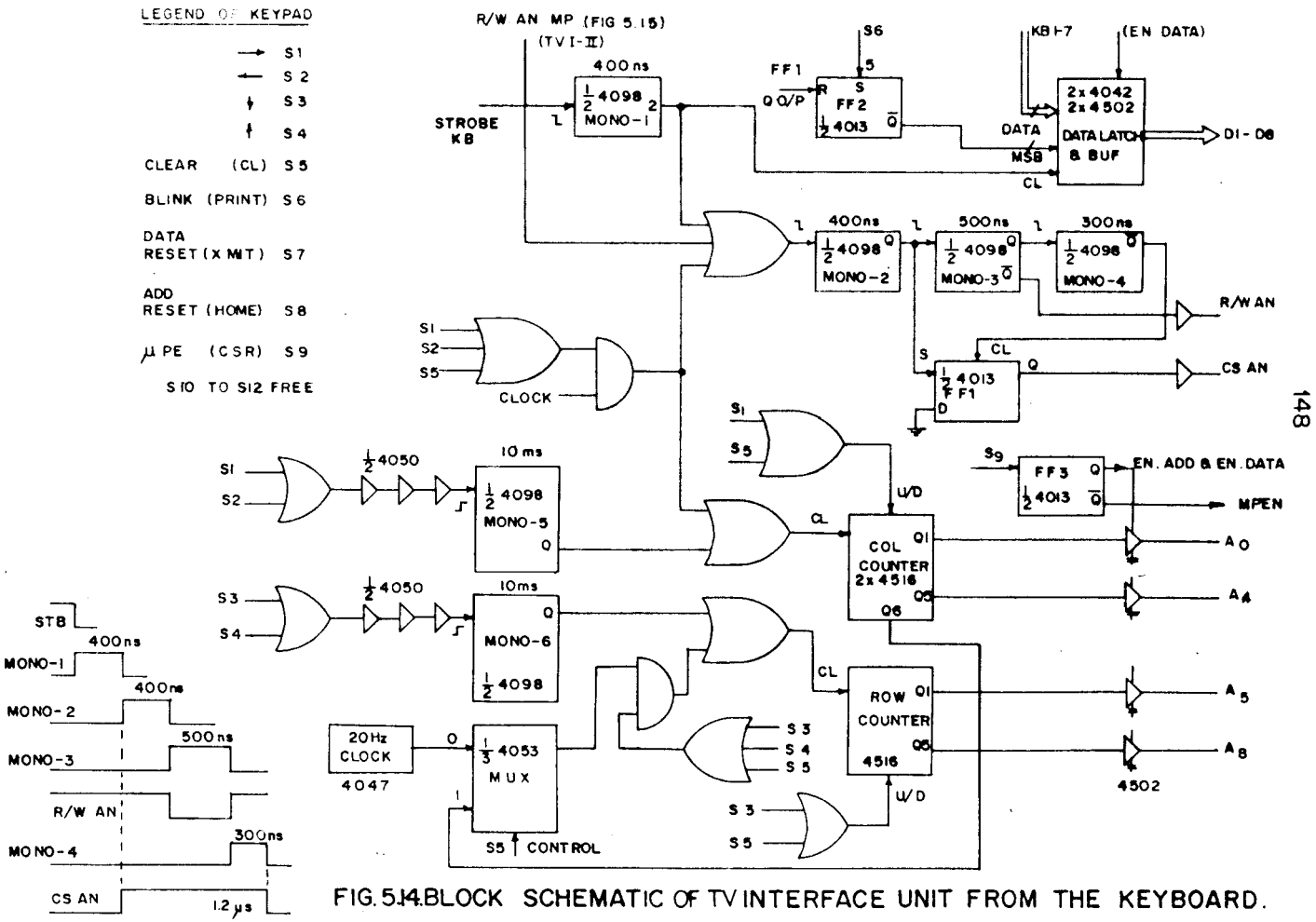


FIG. 5.14. BLOCK SCHEMATIC OF TV INTERFACE UNIT FROM THE KEYBOARD.

User defined keyboard switches, S1 to S9, are utilised in the AN display for generating the cursor control, for resetting the data and the address, for generating blinking characters and for clearing the display. The keyboard switch functions are shown in the Fig. 5.14.

The AN module comprises 512 memory locations corresponding to 16 rows by 32 columns. Lower case, upper case and Greek characters are all available, totalling 128 characters. The MSB of the data byte decides whether the character displayed is to be blinking or not. The flip-flop, FF2, is set by 36. The output of FF2 goes as the MSB of the data latch, while the other 7 bits of data are taken from the keyboard. After issuing write pulse, R/W AN, FF1 resets this blinking FF2.

Address lines, A0 to A4, control the column in which the character is to be displayed, while A5 to A8 control the raw. Two up/down counters are separately used for column control and row control and can be increnented or decremented under keyboard control. The column counter is a 5 bit one, a single clock pulse for which is produced by MONO-5 triggered by either right shift key, S1, or left shift key, S2. The counter is in the UP mode for right shift control.

Similarly row counter is a 4 bit one, the single clock pulse for which is produced by MONO-6 triggered by down shift key, S3, or up shift key, 54. The counter is in the UP mode for up shift control.

In the second mode of operation, any particular character from the keyboard can be written into all the 512 locations. This mode is used for blanking the screen. Clear switch, S5, is used for this operation. Both the counters are connected in series. The Q6 output of the column counter is connected to the clock input of the row counter through a multiplexer and some gate circuits as shown in the figure. An internal clock operating at 20 Hz is used to clock the column counter. By pressing the blank key, or any character and depressing S5, AN characters are copied row by row. Por shifting the cursor by more than few characters, the internal clock can be used by independently enabling the clock signal to the column counter by pressing switches S1, S2 or S5 and for the row counter by switches S3, S4 or S5.

Sufficient delay is introduced for the keys S1 to S4 to avoid switch bouncing. Switch, S9, is used

for enabling the microprocessor, by setting the flip-flop, FF3. FF3 is in the toggling mode and changes state for alternate pulse inputs. The microprocessor is enabled in the switch-on condition by the power-on reset of FF3. The data and address lines are disabled when microprocessor enable, MPEN, signal is active as shown in the figure.

Fig. 5.15 gives the block schematic of the microprocessor driven TV interface unit for driving Graphics module type, MTX-256. Separate latches are used for column address, row address and data for alphanumeric display. These latches are used as locations in memory apace in the microcomputer. This feature avoids output port expansion of the microcomputer and the hardware design becomes quite economical. Some memory locations (0800 to 08FF) are reserved as output ports. In this mode of operation, the output buffers are accessed in the memory write instructions. Timing signals, $\overline{\text{MWR}}$ and TPB-TV, pulses are gated to generate the clock signals for these latches. The data from the microprocessor data bus is transferred to these latches when MPEN signal is true. Each latch circuit is like a memory location and can be selected by decoding the address bits of the microprocessor as shown in Fig. A5.1(a). After loading column address,

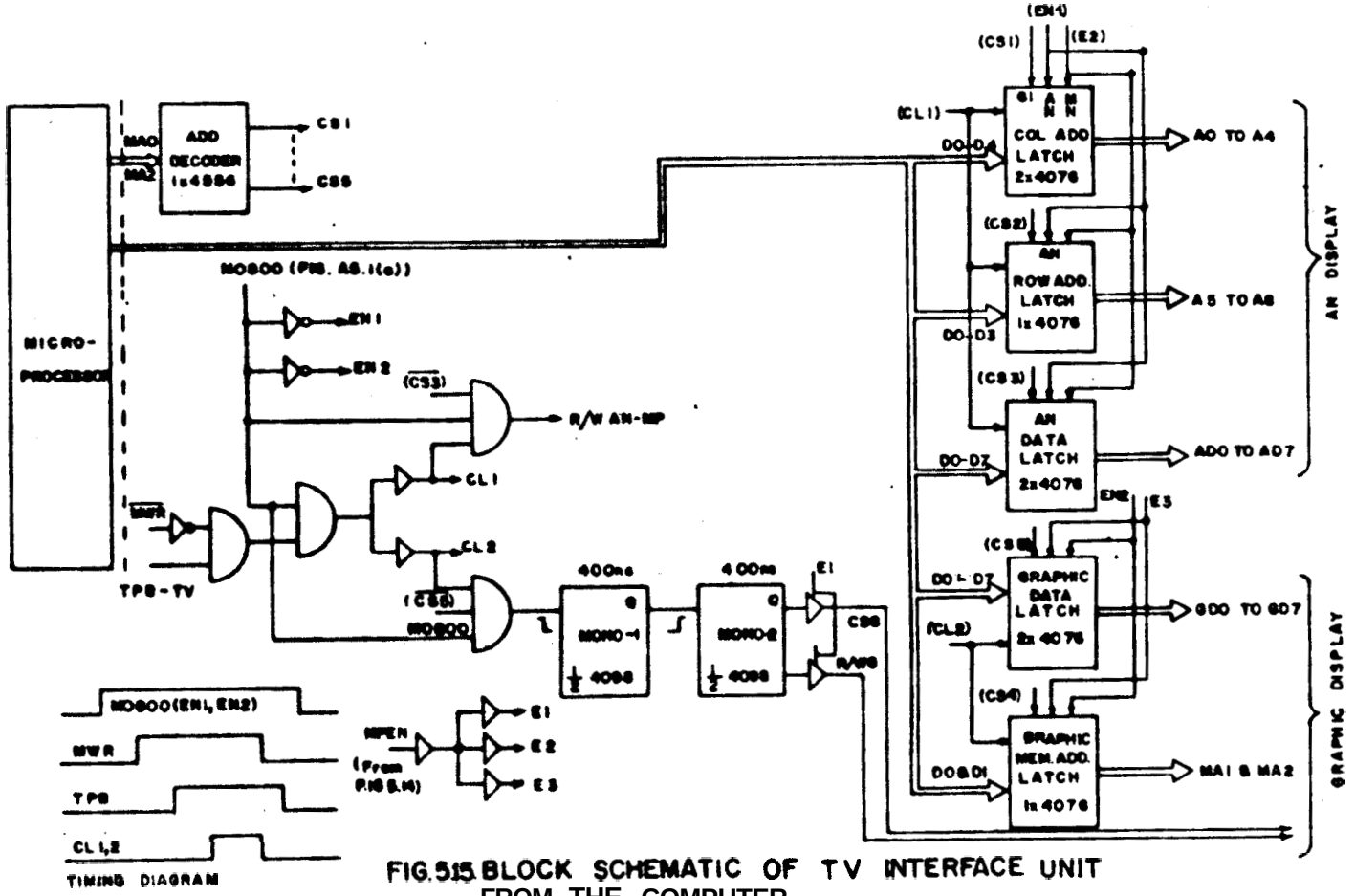


FIG.515 BLOCK SCHEMATIC OF TV INTERFACE UNIT FROM THE COMPUTER.

row address and the data into the appropriate latches, the R/W AN-MP signal is generated by gating the signals $\overline{CS3}$, CLI and MO800 as shown in the figure. The R/W AN-MP signal is used to generate R/W AN and CSAN for the alphanumeric display (Fig. 5.14). Thus different characters can be written in the selected places by the proper data flow under software control. Clearing the screen involves writing a blank character in each location of the AN display. The initialising program clears the screen.

Fig. 5.16 gives the schematic of the software for clearing the AN RAM. Registers B and C contain constants corresponding to the total number of columns (32) and rows (16) respectively to address all the locations. The data corresponding to 'BLANK' is written in all the locations by going through two loops as shown in the figure.

Fig. 5.17 gives the schematic of the software for displaying the house-keeping data on one corner of the TV screen. Console data like BEAM BEGIN, BEAM FINISH, etc, are stored in locations 0700 to 0731 of computer memory and Register D is used as memory pointer for the data. Register B is used as the

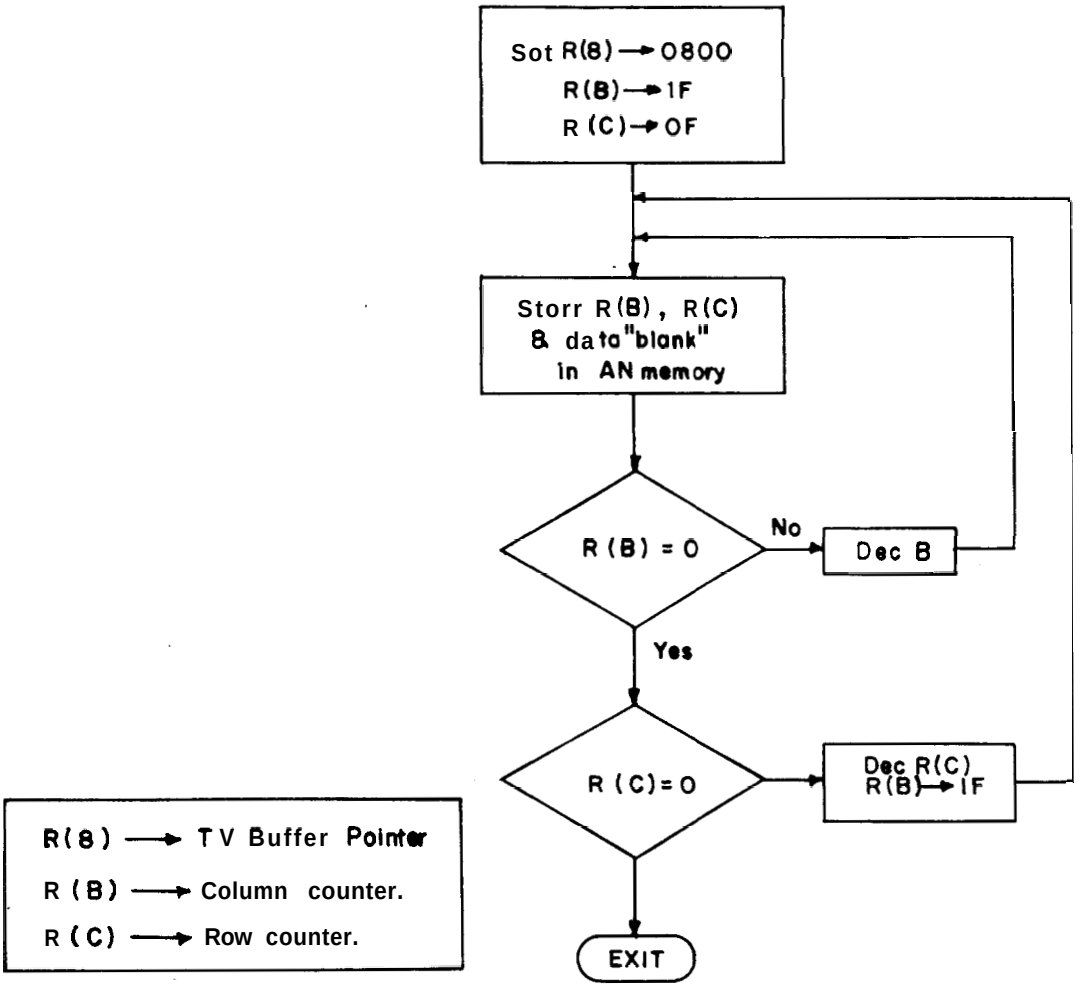


FIG.5.16 FLOW CHART FOR CLEARING AN DISPLAY

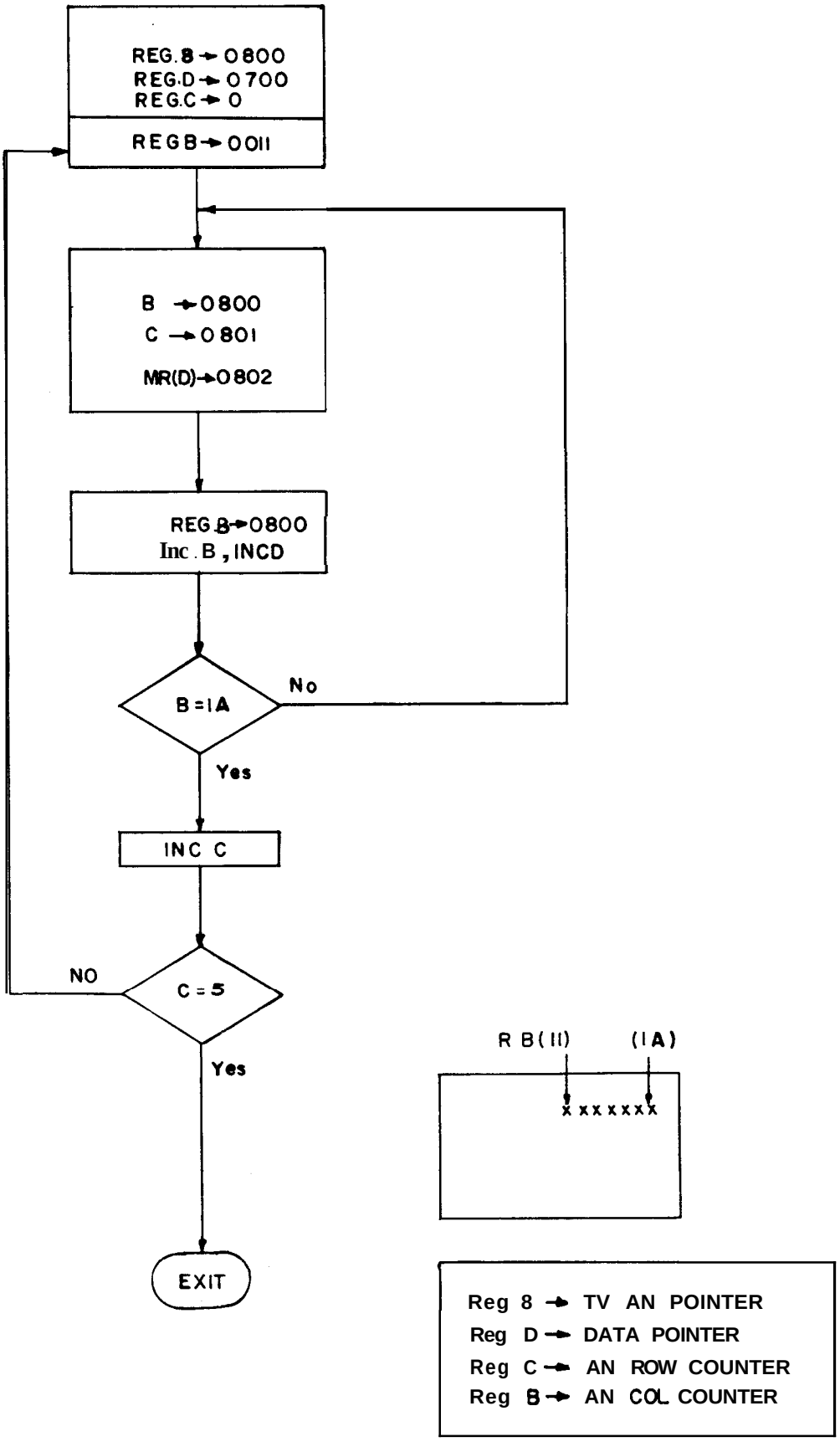


FIG.5.17 FLOW CHART FOR WRITING AN CHARACTERS.

column counter, while Register C is used as the row counter. Register 8 is used as the memory pointer to write data in the AN module.

Fig. 5.18 gives the flow chart of the program for writing data corresponding to the thumbwheel settings of the console. Register 9 is a memory pointer and is initially set to the memory location 0211 from where the console setting data is stored in the following 16 bytes. Register 8 is a TV buffer pointer. Registers B and C are used as the column address and row address counters respectively by the AN display.

The graphic data latch and memory address latch are two locations in the memory space of the graphics module and are loaded with suitable data by generating graphic control signals CSG and R/W G pulses as shown in the Fig. 5.15. MONO-1 provides a delay of 400 ns in generating CSG and R/W G pulses. This allows settling time in the output latch circuits for the data. CSG and R/W G are of 400 ns duration and taken as the Q and $\overline{Q}$ output of MONO-2. The same pulse duration for both the signals is possible because chip-select-to-write-set-up-time, t_{CSW}, and chip-select-to-hold-time, t_{CSH}, required is zero ns.

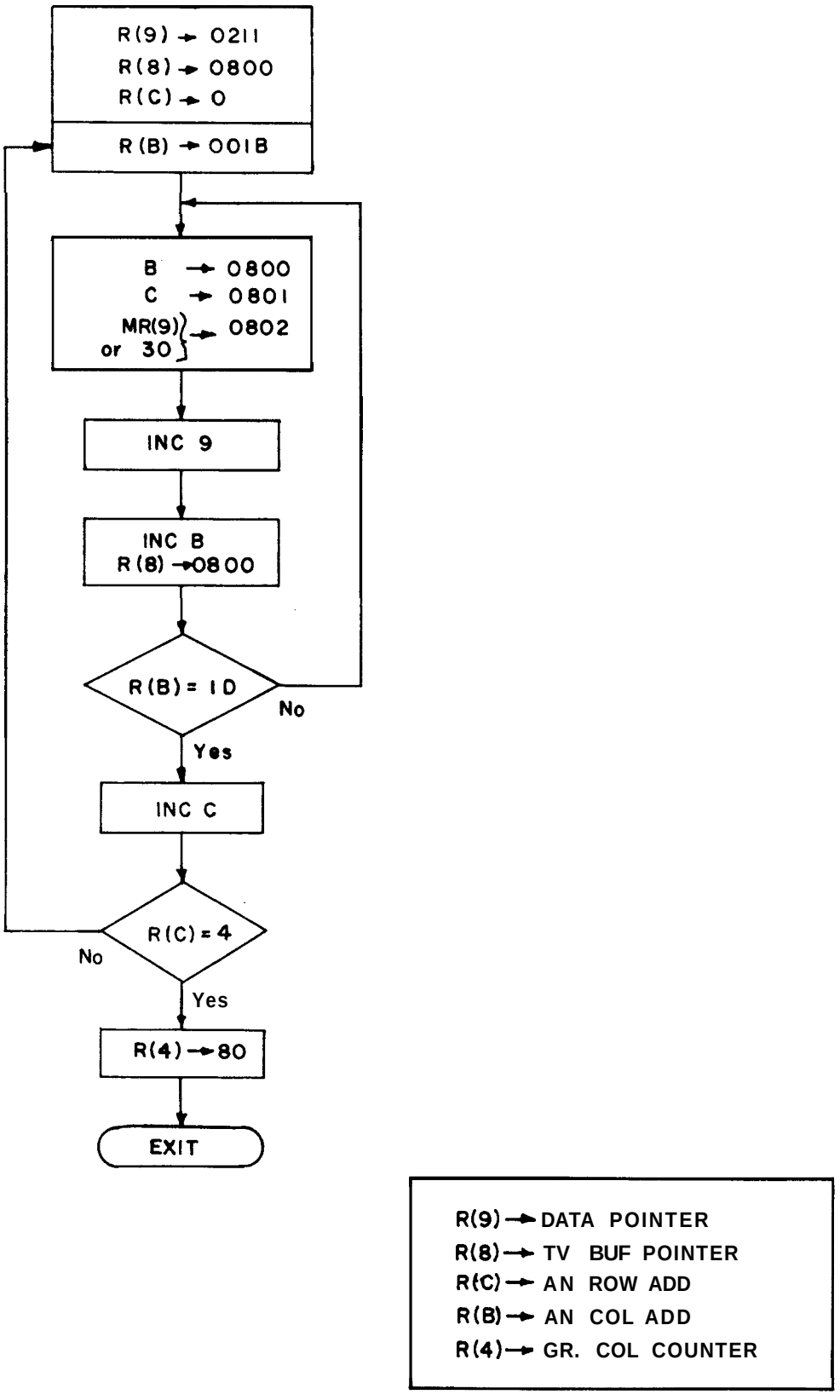


FIG. **5.18** FLOW CHART FOR WRITING ALPHANUMERIC DATA.

Timing requirements of the graphics module is given in the Fig. A8.6 (APPENDIX 8). MONO-1 is triggered by gating $\overline{CS5}$, CL2 and MO800 pulses as shown in the Fig. 5.15 when the data in the corresponding output latches have settled, MPEN, MO800, CL signals are all buffered to drive the various circuits. The timing diagram is also given in the Fig. 5.15.

Fig. 5.19 gives the flow chart of the program for clearing the graphics memory. For clearing the screen, the address has to be set to 3 and the data as zero and then the write pulse has to be issued. A delay of 3.3 ms has to be allowed before transferring any data onto the graphics memory which allows time for writing zeroes in all locations. Register 8 is used as the memory pointer for dumping the data and Register 5 is used for giving the delay time. A number of NOP cycles are executed in a loop and it comes out of the loop, after the required delay time.

Fig. 5.20 gives the flow chart for the program for writing computed data onto the graphics memory. At the end of each integration time, the brightness for all the beams are computed and stored in the computer memory. Since the graphics module has a

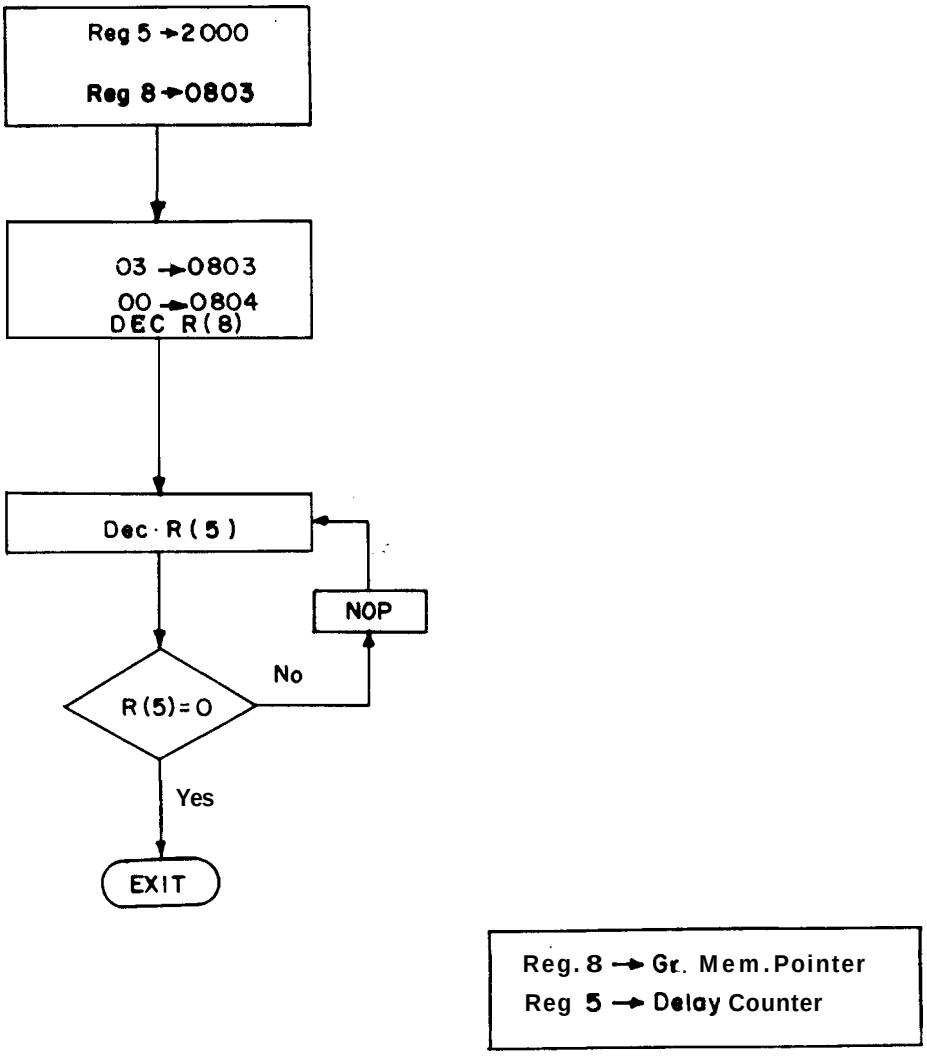


FIG. 5.19 FLOW CHART FOR CLEARING GRAPHIC MEMORY

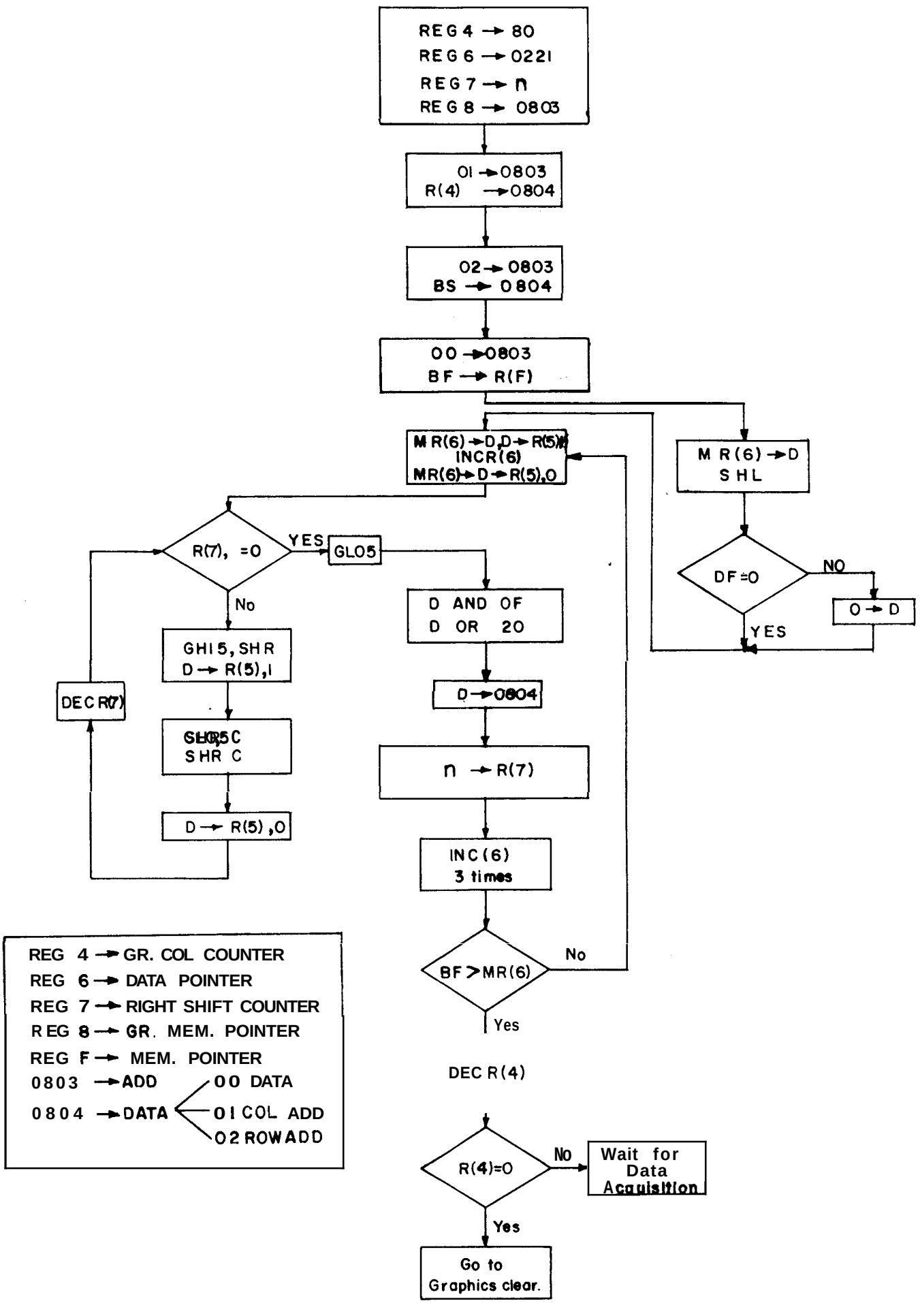


FIG. 5.20. FLOW CHART FOR WRITING GRAPHIC DATA

memory size of 256 X 256 locations, 256 points in each column are used to represent 512 beams in declination; i.e., only alternate beams are displayed. 4 MSB bits out of the 16 bit word corresponding to each beam can be chosen under software control. This number is converted to provide an analog voltage for intensity control of the TV monitor. Register 7 is used for storing a constant corresponding to the number of bits to be shifted. Address of the BEAM START and BEAM FINISH is available in the computer memory at 0200 and 0201 as 2 bytes as already given (Fig. 5.6). Register 8 is used as the memory pointer for transferring the data into the graphics memory. Register 6 is used as the data pointer. Once the address for start location is written, cursor movement control is exercised for writing all the points in that column by giving vector shift control (Ref. APPENDIX 8). The cursor will now point to the start location for writing the column of points corresponding to the following integration cycle. This will progress in the leftward direction for new integration cycles, thereby displaying the brightness distribution map as the earth rotates from west to east.