SOME NEW ADDRESSING TECHNIQUES FOR R M S RESPONDING MATRIX LCDs

A Thesis

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PREFACE

The work presented in this thesis has been carried out in the Liquid Crystal Laboratory, Raman Research Institute, Bangalore and is submitted to the Department of Electrical Communication Engineering, Indian Institute of Science, Bangalore, under the external registration programme. The development of 32 x 32 and 64 x 64 matrix LCDs discussed in this thesis was supported by the Electronics Commission (IPAG), Government of India, under the project 'Multiplexed Liquid Crystal Matrix Display Systems'.

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LIST OF ABBREVIATIONS

APT	-	Alt and Pleshko Technique
ASCII	-	American Standard Code for Information Interface
BAT	-	Binary Addressing Technique
BFM	-	Bit-mapped Frame Memory
BPMS	-	Bi-Polar Monopulse Strobe
CD	-	Column Driver
CG	-	Character Generator
CL	-	Control Logic
CMOS	-	Complementary Metal-Oxide Semiconductor
CNPC	-	Cholesteric-Nematic Phase Change
CNPC-GH	-	CNPC-Guest-Host
CSG	-	Column Signal Generator
DAC	-	Digital to Analog Converter
DDF	-	Display Data Formatter
DPC	-	Dye Phase Change
ECB	-	Electrically Controlled Birefringence
EEPROM	-	Electrically Erasable Programmable Read Only Memory
EPROM	-	Erasable Programmable Read Only Memory
FEE	-	Ferro Electric Effect
FIFO	-	First In First Out
FMT	-	Frame Multiplexing Technique (also referred to as SFMT)
GH	-	Guest Host Displays
GHE	-	Guest Host Effect

HAT	-	Hybrid Addressing Technique
HATs	-	Hybrid Addressing Techniques
HST	-	Half-Select Technique
IAPT	-	Improved Alt and Pleshko Technique
IAPT-R	-	IAPT with reduced selection ratio; used for comparing the supply voltage requirement of a technique with IAPT, for the same selection ratio
ICs	-	Integrated Circuits
IHAT	-	Improved Hybrid Addressing Technique
IHAT-S3	-	IHAT - Special case with 3-voltage levels in the column waveforms
IHAT-S4	-	IHAT - Special case with 4-voltage levels in the column waveforms
ITO	-	Indium Tin Oxide
LCDs	-	Liquid Crystal Displays
LM	-	Legend Memory
LSB	-	Least Significant Bit
MIM	-	Metal-Insulator-Metal
MSB	-	Most Significant Bit
NLC	-	Nematic Liquid Crystal
OST	-	One-third Select Technique
PCT	-	Pulse-Coincidence Technique
PRT	-	Pseudo-Random Technique
RAM	-	Random Access Memory
RCR	-	Re-Circulating Register
RD	-	Row Drivers
ROM	-	Read Only Memory
RPAT	-	Restricted Pattern Addressing Technique
RPATs	-	Restricted Pattern Addressing Techniques

RPAT-NC	-	RPAT - Negative Contrast
RPAT-PC	-	RPAT - Positive Contrast
SBAT	-	Switching Bias Voltage Addressing Technique
SBE-Displays	-	Super-twisted Birefringence Displays
SBE-180	-	SBE Display with 180° twist
SBE - 270	-	SBE Display with 270° twist.
SG	-	Sequence Generator
SSE	-	Smectic Storage Effect
STNLCDs	-	Super-Twisted Nematic LCDs (SBE Displays)
TFAT	-	Two Frequency Addressing Technique
TFT	-	Thin Film Transistor
TFMS	-	Two Field Monopulse Strobe
TNFE	-	Twisted Nematic Field Effect
TN-GH	-	Twisted Nematic Guest Host
TNLCDs	-	Twisted Nematic LCDs
UV-EPROM	-	Ultraviolet Erasable Programmable Read Only Memory
VLG	-	Voltage Level Generator
WAM	-	Waveform Acquisition Module
WM	-	Waveform Memory.

LIST OF SYMBOLS

A - number of times a pixel gets a favourable voltage during $2^{(N-1)}$ or $2^{(l-1)}$ time intervals

A_i - number of times a pixel gets a favourable voltage, when C_i row-select patterns with i mismatches are considered.

A_m - see eqn. (3.123) in page 3.55

B - number of times a pixel gets an unfavourable voltage during $2^{(N-1)}$ or $2^{(l-1)}$ time intervals considered.

B_i - number of times a pixel gets an unfavourable voltage, when C_i row-select patterns with i mismatches are considered.

C_i - number of row-select patterns with i mismatches.

C_m^* - see eqn. (3.121) in page 3.55.

D - see eqn. (3.147) in page 3.63.

E - see eqn. (3.148) in page 3.63.

F - see eqn. (3.149) in page 3.63.

G - see eqn. (3.150) in page 3.63.

K - square of the selection ratio (R).

M - number of columns in a matrix display, i.e., number of signal electrodes.

N - number of address lines multiplexed, i.e., number of scanned lines; number of rows in the matrix display.

N_l - Number of leads to the display.

N_{eq} - The number of address lines to be multiplexed using APT or IAPT in order to get the same selection ratio as that of the technique being compared.

P - Pitch

R - Selection ratio

V - Reduced voltage normalized to the V_{th}

V_c - amplitude of the column (signal) voltage

VDD - positive supply voltage

VEE - negative supply voltage

V_i - amplitude of the column voltage when the number of mismatches is i

V_m - amplitude of the column voltage in 1HAT-S3.

V_{m1} - amplitude of the column voltage in 1HAT-S4 (see page 3.52).

V_{m2} - amplitude of the column voltage in 1HAT-S4 (see page 3.52).

V_r - amplitude of the row-select voltage

V_s - supply voltage in BAT.

V_{supply} - supply voltage requirement of the addressing technique.

V_{sat} - saturation voltage (also referred to as V_{90})

V_{th} - threshold voltage (also referred to as V_{10})

W - Number of selected pixels in a column.