Techniques with low hardware complexity of the driver electronics

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Abstract — Demand for high-quality images in mobile phones has set a new standard for displays in such portable devices. Active-matrix liquid-crystal displays (AMLCDs) are replacing passive-matrix LCDs in these applications. One of the reasons is the lack of simple techniques for displaying a large number of gray shades. The goal was to develop new addressing techniques to fill this void, and it has been achieved without increasing the hardware complexity of the drive electronics. Various techniques that are capable of displaying a large number of gray shades with low hardware complexity of the driver circuit are reviewed.

Keywords — *Wavelets, LCD drivers, power dissipation, multiplexing, matrix addressing.*

1 Introduction

Liquid-crystal displays (LCDs) are found in high-volume consumer products such as cell phones, digital cameras, personal computers, and televisions. Unlike CRTs, flat-panel displays have a large number of drivers. In almost all displays, the number of drivers is equal to the sum of the rows and columns in matrix displays, and high-resolution displays have a few thousand electrodes to be connected to the drivers. Although a small percentage of active-matrix displays have drivers incorporated in them, most of the active-matrix liquid-crystal displays (AMLCDs) have standard driver integrated circuits (ICs) that are fabricated separately on crystalline silicon because the mobility of amorphous-silicon in the active matrix is low. It is worthwhile to improve the performance of passive-matrix LCDs because they have a simple structure that is easy to manufacture. It has less number of steps and consumes less power, chemicals, *etc.*, during the manufacturing process compared to AMLCDs. Reducing the hardware complexity of the drivers will reduce cost and power consumption, and enhance the reliability of passive-matrix displays. Adequate research with the aim to improve the performance will yield results similar to the enormous effort that has gone into the research and development of AMLCDs that has paid rich dividends. Some of the steps that will enhance the performance of passive-matrix LCDs are as follows:

1. Incorporating a black matrix into the passive matrix to increase contrast ratio.
2. Development of new materials to achieve fast response of the display.
3. Increasing the viewing angle of the display by using better materials.
4. Exploring the possibility of new electro-optic effects.
5. Increasing the gray-shade capability.
6. Reducing the hardware complexity of the driver circuits.
7. Reducing power consumption.

We have achieved improvements in the image quality of a display by increasing the number of gray shades and reducing the hardware complexity of the drivers by using energy multiplexing as will be described in this paper.

2 Background

It is well known that orthogonal functions are essential for matrix addressing. They play the same role as that of the carrier waves in communication. Conventional addressing techniques such as line-by-line addressing,[1] active addressing,[2] and multi-line addressing[3] are primarily designed to drive the pixels either to the ON or OFF states. Line-by-line addressing is similar to time-division multiplexing. It is the simplest, and the hardware complexity is the lowest of all the addressing techniques. Active addressing is similar to sequency multiplexing because both are based on Hadamard matrices and Walsh functions, and the active addressing is the most-resource-demanding technique. Information to be displayed on the entire screen has to be accessed within one select time, *i.e.*, a frame-buffer memory with an access time of about 1 nsec is necessary in comparison to about 260 nsec for line-by-line addressing, assuming a refresh rate of 50 Hz for a QVGA display having 240 rows and 320 columns. About 983 million additions per second are to be computed to generate the data voltages for the active addressing, whereas no such computation is necessary for the line-by-line addressing. Multi-line addressing is a combination of sequency and time-division multiplexing. Hardware complexity and the demand on resources of multi-line addressing is lower by a factor of N/s compared to that of active addressing and is higher by a factor s compared to the line-by-line addressing. Here, N is the number of address lines multiplexed and s is the number of address lines that are selected simultaneously. Pulse-width modulation[4] and frame modulation[5] were used to add gray-shade capability to the line-by-line addressing techniques, but the number of

Extended revised version of a paper presented at the Asian Symposium on Information Display (ASID '06) held in New Dehli, India, October 8–12, 2006.

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gray shades is limited because the number of time intervals increases linearly with the number of gray shades. Frame modulation and pulse-width modulation need $G - 1$ time intervals for displaying G gray shades. This will result in flicker when the number of gray shades is large. The smallest time interval in pulse-width modulation may be comparable or even less than the RC (resistance of the switches in the driver circuit and capacitance of the pixels) time constant when the number of gray shades is large. Error in the rms voltage across the pixels due to distortion in the addressing waveforms will result in poor brightness uniformity among pixels that are driven to the same state. Amplitude modulation,[6] pulse-height modulation,[7] can result in a large number of gray shades. The number of voltages in the data waveforms is large, *i.e.*, $2(G - 1)$ when the amplitude modulation is used for displaying G gray shades using line-by-line addressing. It is even higher for pulse-height modulation in multi-line addressing. Either the hardware complexity or the power consumption of the data drivers is high for amplitude modulation and pulse-height-modulation techniques. In summary, gray shades are obtained either by modulating the duration or the amplitude of the voltages. It is evident that a different approach is necessary to surmount the problems associated with these techniques. An eight-gray-level drive technique[8] is the first technique that modulated the energy delivered to the pixel, depending on the bits of the gray shade rather than the gray-shade values themselves. Although it was proposed to display just eight gray shades in combination with multi-line addressing, it has the potential to display a large number of gray shades because the number of time intervals increases logarithmically and not linearly with the number of gray shades. The hardware complexity of the drivers is almost the same as that for a bi-level display as demonstrated by successive approximation techniques.[9,10] The eight-gray-level drive method is a good contender for displaying a large number of gray shades, but for the fact that the selection ratio is low and the supply voltage increases rapidly with the number of gray shades. It is possible to achieve the same results without increasing the supply voltage by modulating the data voltages as shown in this paper. But the selection ratio remains low when either the select voltage or the data voltage is modulated to display gray shades. Successive approximation[10] can display a large number of gray shades and achieve the maximum selection ratio with a moderate increase in the number of time intervals (logarithm of the number of gray shades) and supply voltage. Similarly, wavelet-based addressing techniques can display a large number of gray shades. Both these techniques are based on *energy multiplexing* for displaying gray shades, and this approach has led to a drastic reduction in the drive circuit. The principle of energy multiplexing is discussed in the next section.

3 Principle of energy multiplexing

The response time of LCDs is large (in the range of 10–100 msec) and the pixels cannot immediately respond to abrupt changes in the voltage across them. The electro-optic response of an LCD is less sensitive to the shape of the waveforms across the pixels and the state of the pixels is determined by the energy delivered to the pixels. Hence, the rms voltage controls the light transmission through the pixel. Instead of applying a voltage that corresponds to the desired gray shade within one time interval, a quantum of energy that corresponds to one bit of gray shade is delivered to the pixel by energy multiplexing. Addressing is complete when the energy that is proportional to bit weight of all the bits is delivered to the pixels either sequentially as in a successive approximation technique or simultaneously for a few bits (combination of sequential and parallel approach) as in wavelet-based addressing techniques. The number of voltages in the data waveform will be less and the number of time intervals will be more using the sequential approach. Simultaneous application of energies corresponding to a few bits increases the number of voltages in the scanning and data waveforms, but it takes a less number of time intervals to complete a cycle. It is similar to reducing the $2^g - 1$ comparators in flash analog-to-digital (A/D) or reducing the (maximum) conversion time of $2^g - 1$ in a counter-ramp A/D converter to g steps in a successive-approximation A/D converter.

4 Energy multiplexing by modulating the amplitude of the select voltage

An eight-gray-level drive method for fast-responding STN-LCDs[8] proposed by Mano *et al.* uses the idea of energy multiplexing to some extent. The amplitude of the select pulses is chosen to be in the ratio of 1:2:4 (bit weights of a three-bit binary number) to modulate the energy delivered to the pixels in three time intervals. Although this technique was proposed for multi-line addressing, the idea can be used with any addressing technique. An analysis of this technique by generalizing it for displaying 2^g shades using g time intervals in line-by-line addressing is presented to provide some insight of energy multiplexing.

5 Gray shades by modulating the select pulses

Let us consider a matrix display with N scanning lines (rows). Let $2^i\, V_r$ be the select voltage during the time interval-i. The voltage applied to the data lines (columns) during this time interval is determined by the bit-i of the gray shade of the pixel located at the intersection of the selected address line and the data line. It is $+V_c$, *i.e.*, same sign as that of the select voltage when the bit-i = 0, and $-V_c$, *i.e.*, the opposite are opposite polarity to that of the select voltage when the bit-i = 1. Energy delivered to the pixels is given by the following expression:

$$E_{pixel} = \frac{\sum_{i=0}^{g-1}\left(2^i V_r - d_i V_c\right)^2 + (N-1)\sum_{i=0}^{g-1} d_i^2 V_c^2}{gN}, \quad (1)$$

$$E_{pixel} = \frac{\frac{\left(2^{2g}-1\right)}{3} V_r^2 - \sum_{i=0}^{g-1} 2^{(i+1)} d_i V_r V_c + NgV_c^2}{gN}. \quad (2)$$

The middle term in this expression depends on the bits of the gray shade. The rms voltage across ON and OFF pixels are as follows:

$$V_{ON}(rms) = \sqrt{\frac{\frac{\left(2^{2g}-1\right)}{3} V_r^2 + 2\left(2^g - 1\right) V_r V_c + NgV_c^2}{gN}}, \quad (3)$$

$$V_{OFF}(rms) = \sqrt{\frac{\frac{\left(2^{2g}-1\right)}{3} V_r^2 - 2\left(2^g - 1\right) V_r V_c + NgV_c^2}{gN}}. \quad (4)$$

Then, the selection ratio of this technique is a maximum when

$$\frac{V_r}{V_c} = \sqrt{\frac{3gN}{\left(2^{2g}-1\right)}}. \quad (5)$$

The maximum selection ratio is

$$\mathrm{SR} = \frac{V_{ON}}{V_{OFF}} = \sqrt{\frac{gN + \left(2^g - 1\right)\sqrt{\frac{3gN}{\left(2^{2g}-1\right)}}}{gN - \left(2^g - 1\right)\sqrt{\frac{3gN}{\left(2^{2g}-1\right)}}}}. \quad (6)$$

The selection ratio of this technique is lower than the maximum achievable by any technique:

$$\frac{V_{ON}}{V_{OFF}} = \sqrt{\frac{\sqrt{N}+1}{\sqrt{N}-1}}. \quad (7)$$

A plot of the selection ratios are shown in Fig. 1 for several values of g. Another measure for the performance of the technique is given by N_{eq}, the number of lines that can be multiplexed by the techniques with a selection ratio given in Eq. (7) to achieve the same selection ratio of the technique to be evaluated. It is obtained as follows:

$$N_{eq} = \left(\frac{(SR)^2 + 1}{(SR)^2 - 1}\right)^2, \quad (8)$$

$$N_{eq} = \frac{\left(2^g + 1\right) gN}{3\left(2^g - 1\right)}. \quad (9)$$

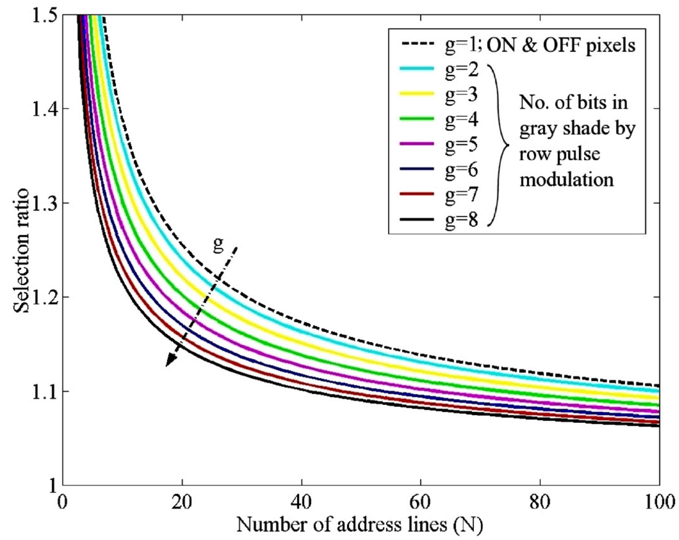

FIGURE 1 — Selection ratio *vs.* number of address lines that are multiplexed; when the select voltage is modulated during g time intervals to display gray shades. The selection ratio decreases with an increase in the number of bits (g), *i.e.,* with the number of gray shades. The g = 1 corresponds to the case of a bi-level display and the selection ratio is $[(\sqrt{N}+1)/(\sqrt{N}-1)]^{1/2}$, the maximum that is achievable in passive-matrix LCDs.

Table 1 shows N_{eq} of this technique for several values of g. A higher N_{eq} implies a lower selection ratio. The N_{eq} will be equal to N for the techniques with the maximum selection ratio. N_{eq} is helpful in selecting the liquid-crystal mixture for passive-matrix displays. A higher N_{eq} demands mixtures with steeper electro-optic characteristics. For example, almost double the number of lines can be multiplexed using the standard technique with the maximum selection ratio compared to the technique of modulating select pulses when g = 6 because N_{eq} is twice N as shown in the table. The supply voltage of this technique is obtained by equating the rms voltage across the OFF pixels to the threshold voltage of the electro-optic characteristics of LCDs.

$$V_{OFF} = V_c \sqrt{\frac{2gN\sqrt{\left(2^g+1\right)} - 2\sqrt{3gN\left(2^g-1\right)}}{gN\sqrt{\left(2^g+1\right)}}} = V_{th}, \quad (10)$$

TABLE 1 — N_{eq} *vs g*, the number of bits of gray shade.

Number of bits of gray shade	$N_{eq} = \frac{(2^g+1).g.N}{3.(2^g-1)}$	$\left(\frac{N_{eq}-N}{N}.100\right)$
1	1	0
2	(10/9)	11.1
3	(9/7)	28.6
4	(68/45)	51.1
5	(55/31)	77.4
6	(130/63)	100.3
7	(301/127)	137.7
8	(2056/768)	168.8
12	(16388/4095)	300.2

$$V_s = V_{th} 2^g \sqrt{\frac{3g^2N^2}{2\left(2^g-1\right)\left(gN\left(2^g+1\right)-\sqrt{3gN\left(2^{2g}-1\right)}\right)}}. \quad (11)$$

The supply voltage of the driver circuit (V_s) increases with g, the number of bits of gray shades as shown in Fig. 2. A low selection ratio and high supply voltage are the two disadvantages of this technique. Hence, modulating the select pulses is not a good approach for displaying gray shades; especially when the number of gray shades is more than eight, *i.e.*, $g > 8$. A low supply voltage that is independent of g for practical values of N can be achieved by modulating the data voltages rather than the select voltage. The resulting supply voltage is about the same as the line-by-line addressing for bi-level displays (*i.e.*, $g = 1$, with pixels driven to either ON or OFF states) as shown in the next section.

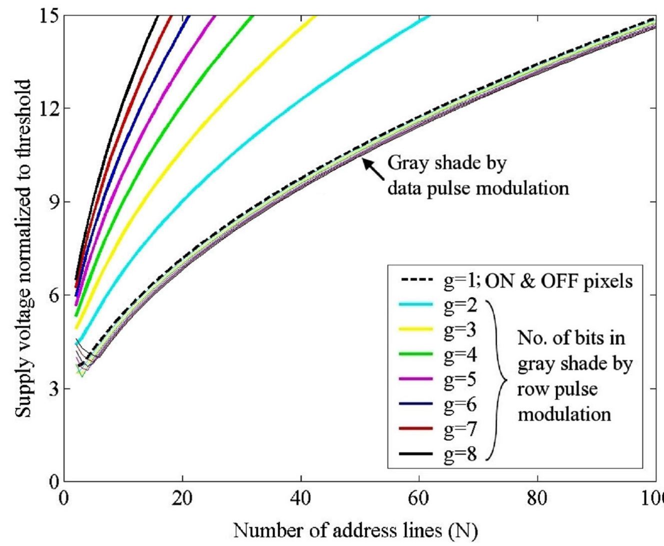

FIGURE 2 — A comparison of supply voltages *vs.* the number of lines that are multiplexed. The dotted line gives the supply voltage of the bi-level technique without gray-shade capability. Supply voltage increases drastically with g, the number of bits of gray-shade when the row pulse (select voltage) is modulated to display gray shades. This is in contrast to the negligible variation in the supply voltage with the number of bits (except for very low values) as shown by the set of gray curves that overlap each other and also lower than that of the bi-level display. Supply voltage is lower than that of the bi-level display in the data modulation technique because the selection ratio is lower than the maximum value of $[(\sqrt{N}+1)/(\sqrt{N}-1)]^{1/2}$.

6 Gray shades by modulating the data voltages

The amplitude of the data voltages is small by a factor $\sqrt{N}$ compared to the select voltage because $V_r/V_c = \sqrt{N}$; the amplitude of the data voltages will be smaller than the select voltage even when g is large, except when just a few lines are multiplexed. Hence, the supply of the driver circuit will not increase with g as evident from the analysis presented here. Energy delivered to a pixel when the amplitude of the data voltages is modulated according to the bit used during that time interval is

$$E_{pixel} = \sum_{i=0}^{g-1} \frac{\left(V_r - 2^i d_i V_c\right)^2 + (N-1)2^{2i}V_c^2}{N}, \quad (12)$$

$$E_{pixel}(ON) = \frac{3gV_r^2 + 2.3\left(2^g-1\right)V_rV_c + \left(2^{2g}-1\right)NV_c^2}{3gN}, \quad (13)$$

$$E_{pixel}(OFF) = \frac{3gV_r^2 - 2.3\left(2^g-1\right)V_rV_c + \left(2^{2g}-1\right)NV_c^2}{3gN}. \quad (14)$$

The selection ratio will be a maximum when

$$\frac{V_r}{V_c} = \sqrt{\frac{\left(2^{2g}-1\right)N}{3g}}. \quad (15)$$

The maximum selection ratio is

$$\frac{V_{ON}}{V_{OFF}}(\text{maximum}) = \sqrt{\frac{\sqrt{\left(2^{2g}-1\right)gN} + \sqrt{3}\left(2^g-1\right)}{\sqrt{\left(2^{2g}-1\right)gN} - \sqrt{3}\left(2^g-1\right)}}. \quad (16)$$

It can be shown that it is equal to the expression in Eq. (6), the selection ratio when the amplitude of the select pulse is modulated depending on the bit used for scanning the display. The supply voltage of the driver circuit is determined as before:

$$V_{OFF} = V_c\sqrt{\frac{2\left(\sqrt{3g}\left(2^{2g}-1\right)N - 3\left(2^g-1\right)\sqrt{\left(2^{2g}-1\right)N}\right)}{3gN\sqrt{3g}}} = V_{th}, \quad (17)$$

$$V_s = \begin{cases} 2^i V_c \text{ for } N \le \left(3g2^{2g}\Big/\left(4\left(2^{2g}-1\right)\right)\right) \\ 2V_r \text{ for } N \ge \left(3g2^{2g}\Big/\left(4\left(2^{2g}-1\right)\right)\right) \end{cases}. \quad (18)$$

For all practical purposes, the supply voltage is determined by V_r and not by $(2^{i-1}V_c)$, *i.e.*, when the value of N is greater than g. The supply voltage is marginally lower than that of the line-by-line addressing for displaying just two shades (*i.e.*, pixels are either ON or OFF) as evident from the plot in Fig. 2. Hence, modulating the data voltages is a better approach than modulating the select pulse when a lower selection ratio is acceptable. However, it is preferable to have a higher selection ratio especially when the matrix display has a large number of rows and columns and the successive approximation technique achieves the maximum selection ratio as will be described in the next section.

TABLE 2 — Equivalent number of address lines, *i.e.*, $N_{eq} = \{3g2^{2g}/[4(2^{2g}-1)]\}$ *vs.* g, when the peak amplitude of the select (row) and data (column) voltages are equal.

g	1	2	3	4	5	6	7	8
$\frac{3g.2^{2g}}{4(2^{2g}-1)}$	1	$\frac{8}{5}<2$	$\frac{16}{7}<3$	$\frac{256}{85}<4$	$\frac{1280}{341}<4$	$\frac{2048}{455}<5$	$\frac{28672}{5461}<6$	$\frac{131072}{2184}<7$

7 Successive approximation techniques (SAT)

The successive approximation technique achieves the maximum selection ratio of $[(\sqrt{N}+1)/(\sqrt{N}-1)]^{1/2}$ by selecting address lines (row) with multiple voltages, with each voltage corresponding to a bit of the gray-shade data.[9,10] The amplitude of the select pulse is $(\sqrt{2})^i V_r$ and it corresponds to bit-i of the gray-shade data. Data voltages of $\pm(\sqrt{2})^i V_c$ are applied during this time interval; the sign of the data voltage is the same as that of the select voltage when the bit-i is logic-0 and opposite to that of the select voltage when the bit-i is logic-1. The remainder of the $N-1$ address lines in a matrix display with N scanning lines (or rows) are held at ground potential. Addressing is completed when all the address lines in the matrix display are selected with voltages corresponding to all the bits, *i.e.*, g voltages for displaying 2^g gray shades. The life of the display is reduced if dc voltages are applied to the pixels. The sign of the select voltage is reversed periodically to ensure dc-free waveforms across the pixels. The display is refreshed continuously by repeating this cycle. The number of voltages is $2g+1$ and $2g$ in the scanning and data waveforms, respectively. However, at any given instant of time just two voltages are applied to the address lines (electrodes) or the data lines. They are as follows:

- One of the select voltages to an address line (row).
- Non-select voltage to the remainder of $N-1$ address lines.
- Data voltage that has the same polarity as the select voltage when the gray-shade bit of the pixel in the selected row is logic 0.
- Data voltage that has the opposite sign compared to the select voltage when the data bit of the pixel in the select address line is logic-1.

Hence, the simple drivers that are used in an alphanumeric display can be used along with four g:1 analog multiplexers that are external to the display as shown in Figs. 3 and 4. It is adequate to have the row and column drivers that are capable of applying one of the two voltages in the internal bus as shown in the figures. The supply voltage of this technique increases with the number of gray shades.[10] It is about twice that of the bi-level (pixels are driven to either

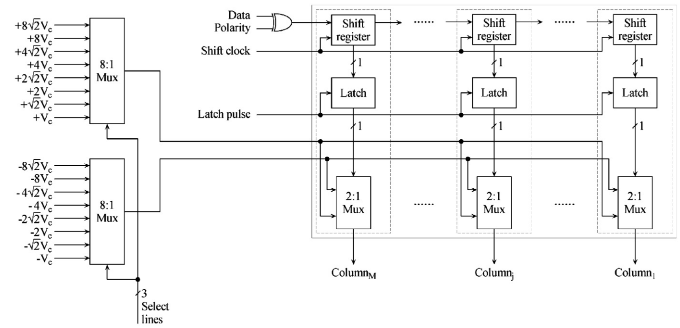

FIGURE 4 — Column drivers of alphanumeric displays can be used to display a large number (256) of gray shades by incorporating two 8:1 analog multiplexers when the successive approximation technique that is based on line-by-line addressing is used to drive the LCDs.

ON or OFF state) displays when the number of gray shades is 256. However it is lower than the case when just the row pulses are modulated as shown in Fig. 5. The supply voltage can be reduced by shifting both the select and data voltages in a polarity so that peak-to-peak voltage in the modified waveforms is confined within the peak-to-peak voltages of the other polarity. This technique is similar to that proposed by Kawakami *et al.*[11] and is based on the fact that the maximum voltage across a pixel is proportional to $2^{(i/2)}(V_r+V_c)$, whereas the peak-to-peak voltage of the select waveforms is proportional to $2[2^{(i/2)}(V_r)]$. About 50% reduction in supply voltage can be achieved by this method when N is large. The supply voltage can also be reduced if the successive approximation is implemented with multi-line addressing.[9] The supply voltage of the drivers decreases with an increase in the number of lines that are selected simultaneously. Advantages of a higher duty cycle associated with multi-line addressing can be obtained at the cost of increasing the number of voltages in the data drivers to $s+1$ when s address lines are selected simultaneously.

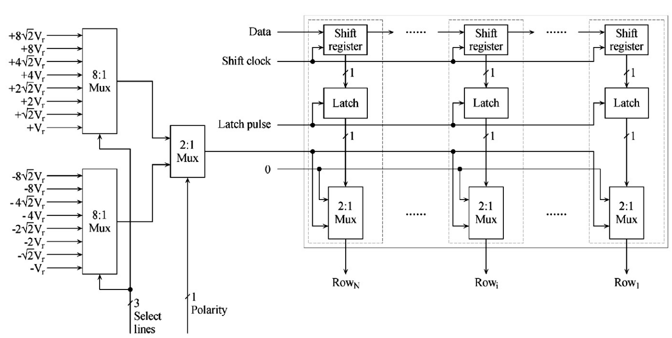

FIGURE 3 — Row drivers of alphanumeric displays can be used to display a large number (256) of gray shades by incorporating two 8:1 and a 2:1 analog multiplexer when the successive approximation technique that is based on line-by-line addressing is used to drive the LCDs.

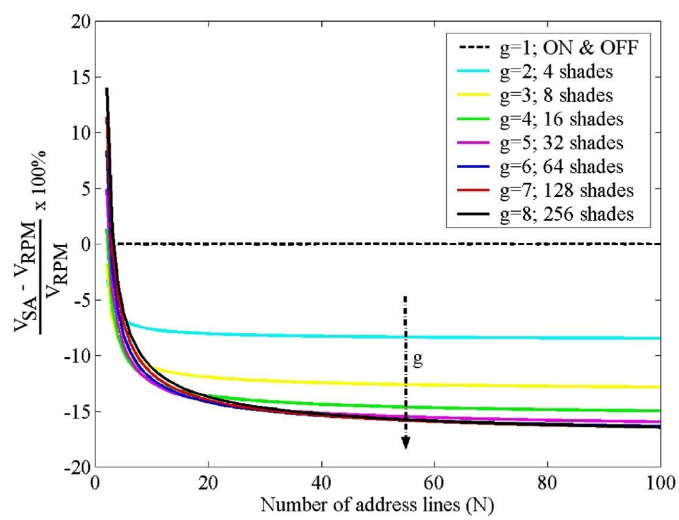

FIGURE 5 — Comparison of supply voltage of the successive approximation (SA) technique with that of row pulse modulation (RPM) for several values of g. Supply voltage of successive approximation technique is lower than that of row pulse modulation for practical values ($N > g$) of N.

8 Salient features of successive approximation

The salient features of successive approximation techniques are as follows:

1. Hardware complexity of the drivers does not increase linearly with the number of gray shades.
2. Drivers that are capable of applying just two voltages (at a given instant of time) are adequate even when a large number of gray shades are to be displayed. Hence, the hardware complexity is about the same as that of simple alphanumeric displays that are capable of driving the pixels to just two states (either ON or OFF).
3. A few multiplexers that are common to the drivers are adequate to increase the number of gray shades from two to any large number (*e.g.*, 256 or more).
4. The number of time intervals increases by a factor $f = \log_2$ (number of gray shades). Increase in the number of time intervals is small compared to the number of gray shades.
5. A flicker-free display is feasible even when a large number of gray shades are displayed.
6. The supply voltage can be reduced either by applying voltage transformations similar to that proposed by Kawakami *et al.*[11] or by using multi-line addressing.

The supply voltage of the drive electronics increases with the number of bits of gray shades. A successive approximation technique with multi-line addressing[9] can reduce the supply voltage of the drive electronics. However, the main advantage, *viz.*, extremely simple row and column drivers, will be lost because the row drivers will have to switch three voltages as compared to two for line-by-line addressing. Hence, row drivers will need a two-bit shift register, two-bit latch, and 3:1 analog multiplexer for each row of the display. Hardware complexity of the column drivers will depend on the number of address lines (rows) that are selected simultaneously. Data waveforms will have $s + 1$ voltages at a given instant of time when s address lines are selected simultaneously. For example, a three-bit shift register, three-bit latch, and 8:1 analog multiplexer is necessary for each column in the display when s ranges from 4 to 7. In summary, the hardware complexity of the multi-line successive approximation technique is the same as that of the multi-line addressing techniques for displaying bi-level images with pixels driven to either the ON or OFF state. An alternate approach is the wavelet-based techniques and salient features of the technique that are presented in the following section.

9 Wavelet-based addressing techniques (WAT)

Each address line in a matrix display can also be selected with a set of wavelets for displaying gray shades.[12] Each wavelet has an energy that is proportional to a bit of the gray-shade data. The number of time intervals will be sum of the time intervals of all the wavelets if the rows are sequentially selected with wavelets. It can be reduced by simultaneous selection of a few address lines with the wavelets. Then it is necessary to have orthogonal wavelets to avoid the crosstalk that will manifest as brightness non-uniformity among pixels that are driven to the same state. The hardware complexity of the drivers will increase as a function of the number of wavelets that are simultaneously used to select the address lines. An orthogonal matrix is constructed using the orthogonal wavelets by taking this factor into consideration. Scanning the matrix display is similar to any other multi-line addressing as described briefly in this section. A detailed description of the technique can be found in Refs. 12–15. The columns of the orthogonal matrix of wavelets are called the select vectors. The address lines (rows) of the matrix display are selected with voltages that are proportional to the elements of a select vector. A data vector is constructed using the bits that correspond to the wavelets that are used at that instant of time to select the address lines. The voltage applied to the data electrodes is proportional to the dot product of the select and data vectors.[12–14] A cycle is complete when all the sets of address lines are selected with all the select vectors and their rotated versions to ensure that each address line has been selected with all the wavelets once. The display is refreshed continuously by repeating this cycle at a rate that is fast enough to eliminate flicker in the display.

A technique for displaying 64 gray shades using integer wavelets was demonstrated.[13] We have shown that drivers that are capable of applying one out of four voltages to the rows and one out of eight voltages to the columns are adequate when a few analog multiplexers are used to select the voltages that are to be connected to the drivers depending on the select vector.[13,14] The same hardware (drivers and the controller) can be used to display 128 gray shades if the integer constraint is not imposed. Typical row and column driver circuits for the wavelet-based techniques are shown in Figs. 6 and 7, respectively. Some simple modifications in the VHDL code of the controller and a new voltage-

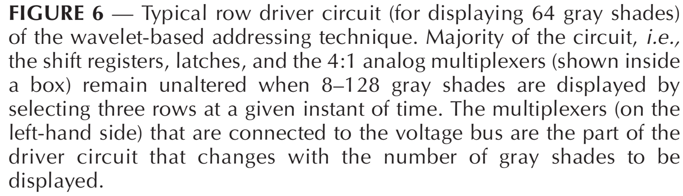

FIGURE 6 — Typical row driver circuit (for displaying 64 gray shades) of the wavelet-based addressing technique. Majority of the circuit, *i.e.*, the shift registers, latches, and the 4:1 analog multiplexers (shown inside a box) remain unaltered when 8–128 gray shades are displayed by selecting three rows at a given instant of time. The multiplexers (on the left-hand side) that are connected to the voltage bus are the part of the driver circuit that changes with the number of gray shades to be displayed.

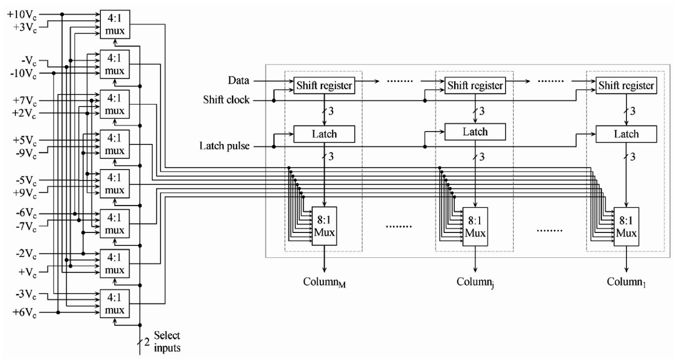

FIGURE 7 — Typical column-driver circuit (for displaying 64 gray shades) of the wavelet-based addressing technique. Majority of the circuit, *i.e.,* the shift registers, latches and the 8:1 analog multiplexers (shown inside a box) remain unaltered when 8–128 gray shades are displayed by selecting three rows at a given instant of time. The multiplexers (on the left-hand side) that are connected to the voltage bus and their input from the voltage-level generator depend on the number of gray shades to be displayed.

level generator is adequate to display 8–128 gray shades without any change in the hardware complexity of the drivers. An example of an orthogonal matrix for displaying 64 gray shades that was constructed using integer wavelets is shown in the following equation:

$$\begin{bmatrix} +4 & +4 & +4 & +4 & -4 & -4 & -4 & -4 \\ +2 & +2 & -2 & -2 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & +4 & +4 & -4 & -4 \\ +4 & -4 & +1 & -1 & +2 & -2 & 0 & 0 \end{bmatrix}. \tag{19}$$

A non-integer orthogonal matrix for displaying 128 gray shades is shown in the following equation:

$$\begin{bmatrix} +4 & +4 & +4 & +4 & -4 & -4 & -4 & -4 \\ +2 & +2 & -2 & -2 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & +4 & +4 & -4 & -4 \\ +4 & -4 & +1 & -1 & +2 & -2 & +\sqrt{2} & -\sqrt{2} \end{bmatrix}. \tag{20}$$

Integer wavelets (and transforms) are preferred to reduce computations in digital signal processing. However, it is not necessary when wavelets are applied to scan matrix LCDs. We have shown that it is not necessary to compute the dot product, and hence wavelets with non-integer elements can also be used without increasing the hardware complexity of the drivers as well as the controller.[14] An example of an orthogonal matrix that is based on slant wavelets with non-integer elements is shown in the following equation:

$$\begin{bmatrix} +4 & -4 & +4 & -4 & +4 & -4 \\ +2\sqrt{6} & 0 & 0 & 0 & -2\sqrt{6} & 0 \\ 0 & +2\sqrt{3} & 0 & 0 & 0 & -2\sqrt{3} \\ +\sqrt{2} & +1 & -2\sqrt{2} & -2 & +\sqrt{2} & +1 \end{bmatrix}. \tag{21}$$

Wavelets are well suited for multi-line addressing wherein several address lines are selected simultaneously. It is also possible to use wavelets and scan the display by selecting one address line at a time.[15]

10 Choice and assignment of wavelets

Simple and easy to generate wavelets are adequate because they are used to multiplex and deliver energies corresponding to the bits of gray shade. LCDs are less sensitive to the shape of the waveforms because they are slow-responding devices and exhibit rms response. The dc-free wavelets are preferred in order to ensure dc-free waveforms across the pixels with a minimum number of time intervals. Energy delivered by a pulse is $E_{pulse} = V^2T$; it is directly proportional to the square of its amplitude and the duration of the pulse. The amplitude is varied while maintaining a constant width of the pulses in the successive approximation technique. Hence, the supply voltage of the driver circuit increases with the number of gray shades. This is in contrast to frame modulation and pulse-width modulation where the number of time intervals increases with the number of gray shades while maintaining constant amplitude. The supply voltage of the driver circuit can be reduced if both the amplitude and duration of the pulse is varied. Orthogonal wavelets are the natural choice for varying the amplitude as well as the duration of the pulses. A wavelet with more time intervals is better suited for delivering a large quantum of energy with smaller amplitude compared to a narrow wavelet. Hence, they are used for the more-significant bits. Similarly, a narrow wavelet is better suited for less-significant bits because the quantum of energy to be delivered is small compared to the more-significant bits. Another advantage of this approach is that the hardware complexity of the drivers reduces drastically. The number of non-zero elements in each of the select vectors, *i.e.,* columns of the orthogonal matrix, decides the maximum number of voltages that are necessary at each instant of time. Hence, limiting the number of non-zero elements ($\bar{z}$) in the columns of the orthogonal matrix to be lower than a specified value will ensure that the maximum number of voltages in the data waveforms for a select vector does not exceed $2^{\bar{z}}$, *i.e.,* at a given instant of time. A great deal of flexibility exists in the construction of the orthogonal matrix. For example, the rows in the orthogonal matrix can range from three to seven as shown by the following matrices:

$$\begin{bmatrix} +4 & +4 & +4 & +4 & -4 & -4 & -4 & -4 \\ +4 & +4 & -4 & -4 & +2 & +2 & -2 & -2 \\ +4 & -4 & +2 & -2 & +\sqrt{2} & -\sqrt{2} & +1 & -1 \end{bmatrix}, \tag{22}$$

$$\begin{bmatrix} +4 & +4 & +4 & +4 & -4 & -4 & -4 & -4 \\ +2 & +2 & -2 & -2 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & +4 & +4 & -4 & -4 \\ +4 & -4 & +1 & -1 & +2 & -2 & +\sqrt{2} & -\sqrt{2} \end{bmatrix}, \tag{23}$$

$$\begin{bmatrix} +4 & +4 & +4 & +4 & -4 & -4 & -4 & -4 \\ +4 & +4 & -4 & -4 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & +2 & +2 & -2 & -2 \\ +4 & -4 & +2 & -2 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & +\sqrt{2} & -\sqrt{2} & +1 & -1 \end{bmatrix}, \tag{24}$$

$$\begin{bmatrix} +4 & +4 & +4 & +4 & -4 & -4 & -4 & -4 \\ +4 & +4 & -4 & -4 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & +2 & +2 & -2 & -2 \\ +4 & -4 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & +2 & -2 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & +\sqrt{2} & -\sqrt{2} & 1 & -1 \end{bmatrix}, \tag{25}$$

$$\begin{bmatrix} +4 & +4 & +4 & +4 & -4 & -4 & -4 & -4 \\ +4 & +4 & -4 & -4 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & +2 & +2 & -2 & -2 \\ +4 & -4 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & +2 & -2 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & +\sqrt{2} & -\sqrt{2} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & +1 & -1 \end{bmatrix}. \tag{26}$$

A matrix of an order eight could be constructed by splitting the wavelet in a row into two rows as shown below:

$$\begin{bmatrix} +4 & +4 & 0 & 0 & -4 & -4 & 0 & 0 \\ 0 & 0 & +4 & +4 & 0 & 0 & -4 & -4 \\ 0 & 0 & 0 & 0 & +2 & +2 & -2 & -2 \\ +4 & +4 & -4 & -4 & 0 & 0 & 0 & 0 \\ +4 & -4 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & +2 & -2 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & +\sqrt{2} & -\sqrt{2} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & +1 & -1 \end{bmatrix}. \tag{27}$$

Although the matrix is not orthogonal, the orthogonal condition will be satisfied because the first row in matrix (26) is split up into two rows and the same data, *i.e.*, MSB, will be used for the first and second rows of matrix (27). The number of time intervals is of the order of N, depending on the value of N/s. The number of rows in the orthogonal matrix can be chosen such that N/s is an exact integer so that the number of time intervals to complete scanning will be exactly equal to the product of the number of select vectors and N.

11 Salient features of WAT

Salient features of wavelet-based addressing techniques are as follows.

1. Number of voltages in the data waveform is less compared to that of amplitude modulation.
2. Number of time intervals is just $8N$, twice that of amplitude modulation for a wide range (16–128) of gray shades.
3. Number of time intervals is small compared to that of frame modulation.
4. Hardware complexity does not increase linearly with the number of gray shades.
5. Hardware complexities of the data drivers can be reduced compared to amplitude modulation and yet a large number of gray shades can be displayed.
6. Hardware complexity of the row and the column drivers can be controlled by the number of non-zero elements in the select vectors.
7. A driver that is capable of applying eight voltages is adequate even when the number of gray shades is 128.
8. It is not necessary to compute the dot product even though a wavelet transform is employed.
9. Voltages corresponding to the dot products are generated in the voltage-level generator.
10. A few multiplexers are used to feed the voltages corresponding to each select vector to the column (data) drivers.
11. Hardware complexity of the controller can be reduced by selecting the number of address lines in a group to be an integer power of 2.
12. Hardware complexity of the drivers and the controller does not depend on the type of wavelets (integer or non-integer types).
13. Wavelets can be used to implement either multi-line or line-by-line addressing techniques.
14. Supply voltage of the wavelet-based line-by-line addressing technique can be reduced by modifying the addressing waveforms.
15. Row drivers that are capable of applying one out of two voltages and column drivers that are capable of applying one out of eight voltages are adequate for displaying 128 gray shades when the display is scanned line by line using wavelets.
16. Number of time intervals to display 128 gray shades is $8N$ in the wavelet-based line-by-line addressing as compared to the $14N$ of successive approximation (including dc-free operation).

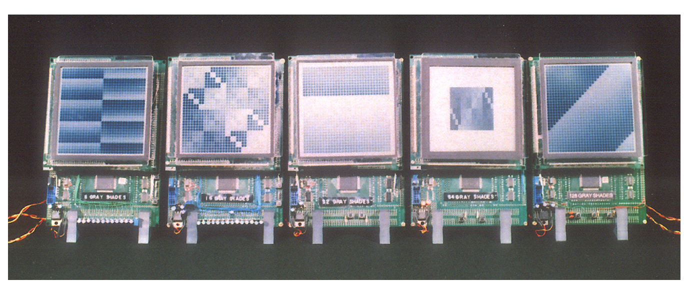

FIGURE 8 — Photographs of the five prototypes of passive-matrix LCDs that are capable of displaying 8–128 (from left to right) gray shades using wavelets. Hardware complexity of the drive circuit is about the same for all the prototypes.

TABLE 3 — A summary of the driver circuits in the prototypes.

Type of Wavelets	Number of gray shades	Row-driver Digital type that can apply	Column-driver Digital type that can apply	External analog multiplexers	Controller (No. of macro cells)
Haar Integer	8 (Multi-line)	1 of 4 voltages	1 of 8 voltages	Nil	111
Haar Integer	16 (Multi-line)	1 of 4 voltages	1 of 8 voltages	2 × (4:1) and 5 × (2:1)	102
Slant	32 (Multi-line)	1 of 4 voltages	1 of 8 voltages	10 × (4:1) and 1 × (2:1)	113
Haar Integer	64 (Multi-line)	1 of 4 voltages	1 of 8 voltages	4 × (8:1) and 8 × (4:1)	84
Haar Non-integer	128 (Line-by-line)	1 of 2 voltages	1 of 8 voltages	9 × (8:1) and 2 × (4:1)	90

Figure 8 shows a photograph of the prototypes that display 8–128 gray shades, but the hardware complexity of the drivers is same in all of them. The only difference is in the VLG in the form of few resistors, few multiplexers to connect the appropriate voltages to the drivers, and some logic circuit in the controller. Table 3 gives the hardware complexity of the driver circuit in these prototypes.

12 Conclusion

The first-generation addressing techniques[1–3] that were proposed 2–4 decades ago were confined to alphanumeric and graphic displays with the aim of driving the pixels either to ON or OFF states. Some gray-shade capability was added in the second-generation techniques[4,5] by modifying the addressing techniques that were primarily aimed at bi-level displays. The third-generation addressing techniques[6–8] were aimed at displaying a large number of gray shades and they have some drawbacks. The hardware complexity of the data drivers is high[6,7] or the selection ratio is low.[8] Apart from surmounting these problems, the fourth-generation techniques[9,10,12–15] have low hardware complexity, some of them having almost the same hardware complexity as that of the bi-level displays, and this trend began with the eight-level gray-shade technique.[8] Successive approximation can be incorporated into any bi-level display with a few minor additions to the voltage generator and the controller. If a high selection ratio is not important, then the gray shades can be achieved even without any increase in supply voltage by modulating the data voltages alone as discussed in this paper. The wavelet-based addressing techniques have the advantage of a lower supply voltage and have a smaller number of time intervals to complete a cycle that is dc-free. Use of complex wavelets does not demand or any computations during the scanning of the display and this is in contrast to applications of wavelets in signal processing. The concept of energy multiplexing has some similarity to "distributed arithmetic" in signal processing. The idea of energy multiplexing is basic in nature and it can be universally applied to all the addressing techniques including active-matrix addressing. Some subtle but important points that contribute to the success of energy multiplexing were discussed in this article. Further research in this field will enhance the use of LCDs.

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