Design and implementation of a wavelet-based addressing technique (WAT)

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Abstract — The design and implementation of a wavelet-based addressing technique capable of displaying gray shades is presented. The hardware complexity of the display drivers has been reduced by adding a few analog multiplexers that are common to the drivers. The controller was implemented by using a low-cost complex programmable logic device (CPLD) and it was demonstrated by displaying 16 gray shades in a liquid-crystal display.

Keywords — *Controller, wavelets, liquid-crystal displays (LCDs), multi-line addressing (MLA).*

1 Background

It is advantageous to use wavelets for displaying gray shades in passive-matrix liquid-crystal displays.[1] Wavelets with energies that are proportional to the binary weight of bits of gray-shade data are used to deliver energies that correspond to the gray shade of the pixels. The hardware complexity of the data drivers is reduced as compared to that of the amplitude modulation.[2] Flicker in the display can be avoided even when the refresh rate is less compared to that of the frame modulation, *i.e.*, frame-rate control.[3]

2 Technique

Consider a matrix liquid-crystal display (LCD) with N rows (also called scanning electrodes) and M columns (also called data electrodes). Let the N rows be arranged to form about N/s sets, with each set consisting of s rows, wherein s is the number of rows in the matrix of orthogonal wavelets. This is similar to forming subgroups in multi-line addressing (MLA). Columns in the matrix of orthogonal wavelets are called select vectors. The rows in a set are selected by applying voltages that are proportional to elements of a select vector. Non-select voltage is applied to the rows in the non-selected sets and to the rows corresponding to the element zero (if any) in the select vector. Each bit of the gray-shade data is associated with a wavelet. A data matrix is formed by selecting the bits of the gray-shade data corresponding to the wavelets. Hence, there is a 1:1 correspondence among the elements of the data matrix and the matrix of the wavelets. Columns of the data matrix are called data vectors. Voltages to be applied to the columns are obtained by computing the dot product of the select and data vectors. Row and column voltages are applied simultaneously to the electrodes in the matrix display for duration T. This time interval is referred to as the select time. Each one of the N/s sets of rows is selected with each one of the select vectors as well as their $(s-1)$ rotated versions to complete a cycle. This will ensure that all the pixels in the display are selected with all the wavelets, and the energy delivered to the pixels will be proportional to the gray-shade data. The select time is chosen to be small enough to avoid flicker in the display. A set of wavelets is chosen such that the energy of each wavelet is proportional to the binary weight of a bit of the gray-shade data. All these wavelets are used to select rows (address lines) in a matrix display. For example, the matrix of orthogonal wavelets is constructed by modifying the Haar wavelets as shown in the following equation:

$$O_{(4\times8)} = \begin{bmatrix} +2 & +2 & -2 & -2 & +2 & +2 & -2 & -2 \\ +2 & -2 & 0 & 0 & +2 & -2 & 0 & 0 \\ +1 & +1 & +1 & +1 & -1 & -1 & -1 & -1 \\ 0 & 0 & +1 & -1 & 0 & 0 & +1 & -1 \end{bmatrix}. \quad (1)$$

Energies of the wavelets in rows 1–4 are 32, 16, 8, and 4, respectively. They correspond to the most significant to least significant bit of the gray-shade data. Data bits that correspond to each element of the matrix in Eq. (1) are shown in Eq. (2).

$$d_{(4\times8)} = \begin{bmatrix} d_3 & d_3 & d_3 & d_3 & d_3 & d_3 & d_3 & d_3 \\ d_2 & d_2 & x & x & d_2 & d_2 & x & x \\ d_1 & d_1 & d_1 & d_1 & d_1 & d_1 & d_1 & d_1 \\ x & x & d_0 & d_0 & x & x & d_0 & d_0 \end{bmatrix}. \quad (2)$$

An x in the data matrix denotes a "don't care" condition because the corresponding element in the orthogonal matrix is zero. The d_3 to d_0 are the data bits, *i.e.*, the most-significant bit (MSB) to the least-significant bit (LSB), in that order.

2.1 Algorithm for scanning the display

A matrix display is scanned as described in the following paragraph.

1. The s rows in a set are selected with voltages corresponding to one of the select vectors.
2. The remainder of the $(N-s)$ non-selected rows in the display are held at 0 V.
3. Data bits that correspond to the select vector are fetched to form the data vector (as shown in the data matrix).

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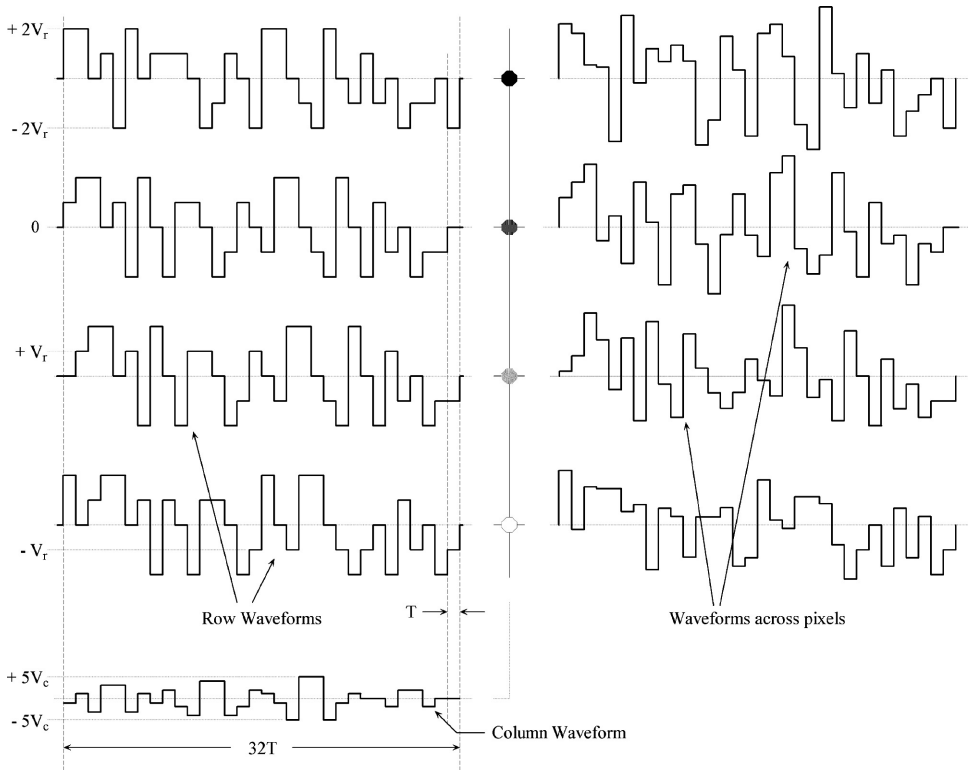

FIGURE 1 — Typical waveforms of the wavelet-based addressing technique (WAT).

4. Dot products of the select and data vectors are computed, and they (referred to as column signal) are shifted in to the shift register of the column driver.
5. Data corresponding to the select and non-select voltages are shifted in to the shift register of the row driver.
6. Data in the shift registers of both the row and column drivers are latched simultaneously. Thus, the select and non-select voltages from the row driver and data voltages from the column driver are applied to the row and column electrodes of the display.
7. Steps 1 to 6 are repeated with a new select vector until all the select vectors in the matrix of the orthogonal wavelets are used once to select a set of rows.
8. The matrix of orthogonal wavelets and the corresponding data matrix are rotated vertically by one position.
9. Steps 1 to 8 are carried out $(s - 1)$ times, so that a set (out of N/s sets) of rows in the matrix display is selected with all the select vectors and their rotated versions.
10. Steps 1 to 9 are repeated N/s times to select all the sets in the display. If N is not an integer multiple of s then a few (less than s) rows are added to ensure that the number of rows in all the sets is equal to s and a zero is assigned as the data to the pixels in these extra rows.
11. The display is refreshed continuously by repeating this cycle at a rate that is fast enough to avoid flicker.

The scanning sequence described here selects a subgroup (a set of N/s rows) with all the select vectors and their rotated versions and then moves on to the next subgroup. However, several other select sequences are possible. For example, one can distribute the select vectors by selecting one set of rows with one select vector and move on to select another set and use the same or different select vector. This will change the frequency spectrum across the pixels and also improve the brightness uniformity. We have distributed the select pulses by selecting each set with 2^i (i is any one of six values in the range of 0 to 5) select vectors consecutively before selecting the next set of rows. Typical waveforms when a set of rows is selected with all the select vectors in Eq. (1) and their rotated versions consecutively (select pulses are clustered together) are shown in Fig. 1.

2.2 Analysis of the addressing technique

Let the unit step of voltages in row and column waveforms be V_r and V_c, respectively. The scanning algorithm ensures that all the pixels in the matrix display are selected with all the wavelets. The root-mean-square (RMS) voltage across the pixels is given by the following equation:

$$V_{\text{pixel}}(\text{RMS}) = \sqrt{\frac{\sum_{k=0}^{g-1} e_k\left(V_r^2 - 2d_{i,j,k}V_rV_c + V_c^2\right)}{Nv}}, \qquad (3)$$

where e_k is the energy of the kth wavelet, g is the number of bits in the gray-shade data, and v is the number of inde-

pendent select vectors. Here, $d_{i,j,k}$ denotes the bit corresponding to the kth wavelet of the gray-shade data of a pixel in the ith row and jth column of the display. The RMS voltage across the ON pixel [V_{on}(RMS)] is obtained by assigning –1 to all the bits in the data.

$$V_{on}(\text{RMS}) = \sqrt{\frac{E\left(V_r^2 + 2V_rV_c + V_c^2\right)}{Nv}}. \quad (4)$$

Here, E denotes the total energy of all the wavelets. Similarly, the RMS voltage across the OFF pixel [V_{off}(RMS)] is obtained by substituting +1 for all the data bits.

$$V_{off}(\text{RMS}) = \sqrt{\frac{E\left(V_r^2 - 2V_rV_c + V_c^2\right)}{Nv}}. \quad (5)$$

The selection ratio, defined as the ratio of the RMS voltage across the ON and OFF pixels, will be maximum when

$$V_r = \sqrt{N}V_c. \quad (6)$$

The OFF pixels are biased near the threshold voltage (V_{th}) of the liquid-crystal mixture, and hence the threshold voltage is equated to the RMS voltage across the OFF pixels.

$$V_{off} = V_{th} = \left(\sqrt{\frac{E\left(2N - 2\sqrt{N}\right)}{Nv}}\right)V_c. \quad (7)$$

Hence,

$$V_c = \left(\sqrt{\frac{Nv}{2E\left(N - \sqrt{N}\right)}}\right)V_{th}. \quad (8)$$

The supply voltage of the drivers is determined by the maximum swing in the row and column waveforms, which depends on N, the number of rows in the matrix display. Let the peak-to-peak voltage in the row waveform be $V_{RW(p\text{-}p)}$; it is equal to twice the maximum value of the element in the matrix of orthogonal wavelets. Similarly, let the peak-to-peak voltage in the column waveform be $V_{CW(p\text{-}p)}$.

$$V_{RW(p-p)} = 2p\left(\sqrt{\frac{v}{E}}\right)\left(\frac{N}{\sqrt{2\left(N - \sqrt{N}\right)}}\right)V_{th}, \quad (9)$$

$$V_{CW(p-p)} = 2q\left(\sqrt{\frac{v}{E}}\right)\left(\frac{\sqrt{N}}{\sqrt{2\left(N - \sqrt{N}\right)}}\right)V_{th}. \quad (10)$$

Here, p is the maximum value in the matrix of the orthogonal wavelets and q is the maximum value of the dot product. $V_{CW(p\text{-}p)}$ is greater than $V_{RW(p\text{-}p)}$ when the number of rows in the matrix is small, whereas $V_{RW(p\text{-}p)}$ is greater than $V_{CW(p\text{-}p)}$ when N is large. Hence, the supply voltage is equal to the peak-to-peak voltage in the column waveform ($2qV_c$) for lower values of N and is equal to the peak-to-peak voltage in the row waveform ($2p\sqrt{N}V_c$) for higher values of N.

2.3 Matrices of orthogonal wavelets

The matrix of wavelets in Eq. (1) is not unique; several matrices for displaying 16 gray shades can be formed as shown in Eqs. (11)–(17). The elements of each wavelet are enclosed within the parenthesis in these matrices.

$$O_{1(4\times8)} = \begin{bmatrix} \left(+\sqrt{2} & +\sqrt{2} & +\sqrt{2} & +\sqrt{2} & -\sqrt{2} & -\sqrt{2} & -\sqrt{2} & -\sqrt{2}\right) \\ 0 & 0 & 0 & 0 & \left(+\sqrt{2} & +\sqrt{2} & -\sqrt{2} & -\sqrt{2}\right) \\ (+1 & +1 & -1 & -1) & 0 & 0 & 0 & 0 \\ (+1 & -1) & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \quad (11)$$

$$O_{2(4\times8)} = \begin{bmatrix} 0 & 0 & (+2 & +2 & -2 & -2) & 0 & 0 \\ (+1 & +1 & -1 & -1 & -1 & -1 & +1 & +1) \\ 0 & 0 & 0 & 0 & 0 & 0 & \left(+\sqrt{2} & -\sqrt{2}\right) \\ (+1 & -1) & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \quad (12)$$

$$O_{3(4\times8)} = \begin{bmatrix} \left(+\sqrt{2} & +\sqrt{2} & +\sqrt{2} & +\sqrt{2} & -\sqrt{2} & -\sqrt{2} & -\sqrt{2} & -\sqrt{2}\right) \\ (+1 & +1 & -1 & -1 & -1 & -1 & +1 & +1) \\ 0 & 0 & 0 & 0 & (+1 & -1 & -1 & +1) \\ (+1 & -1) & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \quad (13)$$

$$O_{4(4\times8)} = \begin{bmatrix} (+2 & +2 & +2 & +2 & -2 & -2 & -2 & -2) \\ \left(+\sqrt{2} & +\sqrt{2} & -\sqrt{2} & -\sqrt{2} & -\sqrt{2} & -\sqrt{2} & +\sqrt{2} & +\sqrt{2}\right) \\ 0 & 0 & 0 & 0 & \left(+\sqrt{2} & -\sqrt{2} & +\sqrt{2} & -\sqrt{2}\right) \\ (+1 & -1 & +1 & -1) & 0 & 0 & 0 & 0 \end{bmatrix} \quad (14)$$

$$O_{5(4\times8)} = \begin{bmatrix} (+2 & +2 & +2 & +2 & -2 & -2 & -2 & -2) \\ \left(+\sqrt{2} & +\sqrt{2} & -\sqrt{2} & -\sqrt{2} & -\sqrt{2} & -\sqrt{2} & +\sqrt{2} & +\sqrt{2}\right) \\ (+1 & -1 & +1 & -1 & -1 & +1 & -1 & +1) \\ 0 & 0 & (+1 & -1 & +1 & -1) & 0 & 0 \end{bmatrix} \quad (15)$$

$$O_{6(2\times8)} = \begin{bmatrix} \left(+\sqrt{2} & +\sqrt{2} & +\sqrt{2} & +\sqrt{2} & -\sqrt{2} & -\sqrt{2} & -\sqrt{2} & -\sqrt{2}\right) \\ \left(+\sqrt{2} & +\sqrt{2} & -\sqrt{2} & -\sqrt{2}\right) & \left(+\sqrt{2} & -\sqrt{2}\right) & (+1 & -1) \end{bmatrix} \quad (16)$$

$$O_{7(2\times8)} = \begin{bmatrix} (+1 & -1) & (+2 & +2 & -2 & -2) & \left(+\sqrt{2} & -\sqrt{2}\right) \\ (+1 & +1 & -1 & -1 & -1 & -1 & +1 & +1) \end{bmatrix} \quad (17)$$

The supply voltage of the drivers depends on the wavelets as well as their amplitudes. A comparison of the matrices of orthogonal wavelets is given in Table 1. It can be seen

TABLE 1 — Comparison of a few matrices of orthogonal wavelets that could be used for displaying 16 gray shades.

Eq. No.	E	Row waveform			Column waveform			N_c	$\frac{V_{supply\ (WAT)}}{V_{supply\ (APT)}}$ $N > N_c$
		n_r	n_{rs}	p	n_c	n_{cs}	q		
(1)	60	5	4	2	11	6	5	7	0.7303
(11)	30	5	4	$\sqrt{2}$	13	6	$2+\sqrt{2}$	6	0.7303
(12)	30	7	3	2	11	4	3	3	1.0328
(13)	30	5	4	$\sqrt{2}$	10	6	$2+\sqrt{2}$	6	0.7303
(14)	60	7	4	2	14	8	$2+2\sqrt{2}$	12	0.7303
(15)	60	7	4	2	18	10	$4+\sqrt{2}$	15	0.7303
(16)	30	5	3	$\sqrt{2}$	7	4	$2\sqrt{2}$	4	0.7303
(17)	30	7	3	2	11	4	3	3	1.0328

n_r and n_c are the number of voltages in the row and column waveforms respectively.
n_{rs} is the maximum number of voltages in the row waveform for a given select vector.
n_{cs} is the maximum number of voltages in the column waveform for a given select vector.

that the number of voltages in row and column waveforms (see n_r and n_c) depends on the arrangement of the wavelets in the matrix. The number of voltages to be applied simultaneously to the display at any point in time (see n_{rs} and n_{cs}) is less than the number of voltages in the row and column waveforms. Hence, the hardware complexity of the drivers can be reduced as described in the Sections 3.1 and 3.2. The matrices in Eqs. (16) and (17) have three wavelets in a row, and their elements are enclosed within parenthesis. All of the four wavelets have been accommodated in just two rows. Data bits to be fetched from the memory depend on the select vector. Data matrix in Eq. (18) corresponds to the matrix of the orthogonal wavelets in Eq. (16).

$$d_{5(2\times 8)} = \begin{bmatrix} (d_3 & d_3 & d_3 & d_3 & d_3 & d_3 & d_3 & d_3) \\ (d_2 & d_2 & d_2 & d_2) & (d_1 & d_1) & (d_0 & d_0) \end{bmatrix}. \quad (18)$$

Although the matrices in Eqs. (12), (16), and (17) have the lowest number of voltages to be applied at any time, the supply voltage is higher when the matrices in Eqs. (12) and (17) are used for scanning the display. The matrix in Eqs. (1) is used in our prototype and has the same supply voltage as that of Eq. (12) but require a column driver that is capable of applying one out of six voltages to the electrodes. The matrix in Eq. (16) is the best among these matrices because the maximum number of voltages that is necessary at a given instant of time is the least, and the supply voltage is also lower when this matrix is used for scanning the display. The matrix in Eq. (1) selects three rows at a time while the matrix in Eq. (16) selects two rows at a time. A comparison of supply voltage normalized to the supply voltage of the Alt and Pleshko technique[4] (APT) is given in the table. Values for the variables E, p, and q in Eqs. (9) and (10) are given in the table, while v is 8 for all the equations. The supply voltage of the wavelet addressing technique (WAT) and APT are given by Eqs. (19) and (20), respectively, while there ratio shown in the table is given by Eq. (21).

$$V_{supply(WAT)} = p\left(\sqrt{\frac{v}{E}}\right)\left(\frac{\sqrt{2}N}{\sqrt{\left(N-\sqrt{N}\right)}}\right)V_{th} \ \forall\ N > N_c, \quad (19)$$

$$V_{supply(APT)} = \left(\frac{\sqrt{2}N}{\sqrt{\left(N-\sqrt{N}\right)}}\right)V_{th}, \quad (20)$$

$$\frac{V_{supply(WAT)}}{V_{supply(APT)}} = \left(p\sqrt{\frac{v}{E}}\right) \ \forall\ N > N_c. \quad (21)$$

Here, N_c is the value of N above which the peak-to-peak voltage of the row waveforms is greater than that of the column waveforms. The number of rows in the display is usually large; hence, it is sufficient to consider supply voltage with respect to peak-to-peak voltage in the row waveforms.

3 Hardware implementation

A block diagram of the prototype that demonstrates the technique is shown in Fig. 2. It is designed to display the images stored in a memory. Data from the memory is fetched using the address generated by the controller. Data for the row and column drivers are also generated in the controller. The design and implementation of each of these blocks is outlined in this section.

3.1 Row driver

The row waveforms have five voltages, *viz.*, $+2V_r$, $+V_r$, $-V_r$, $-2V_r$, and 0 (the non-select voltage) which are coded using 2's complement notation, *i.e.*, a +2 is coded as 010, –2 as 110, +1 as 001, –1 as 111 and 0 is coded as 000. A standard display driver that is capable of applying one of the eight voltages (TMS 57206) (just one of five will be adequate in this application) could be used as the row driver. We have used a standard printed-circuit board (PCB) with similar capability. However, it is possible to use a driver with lower hardware complexity by recognizing the fact that four out of the

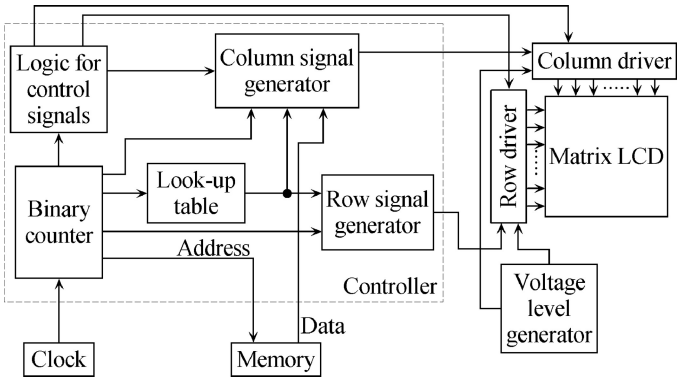

FIGURE 2 — Block diagram of the prototype.

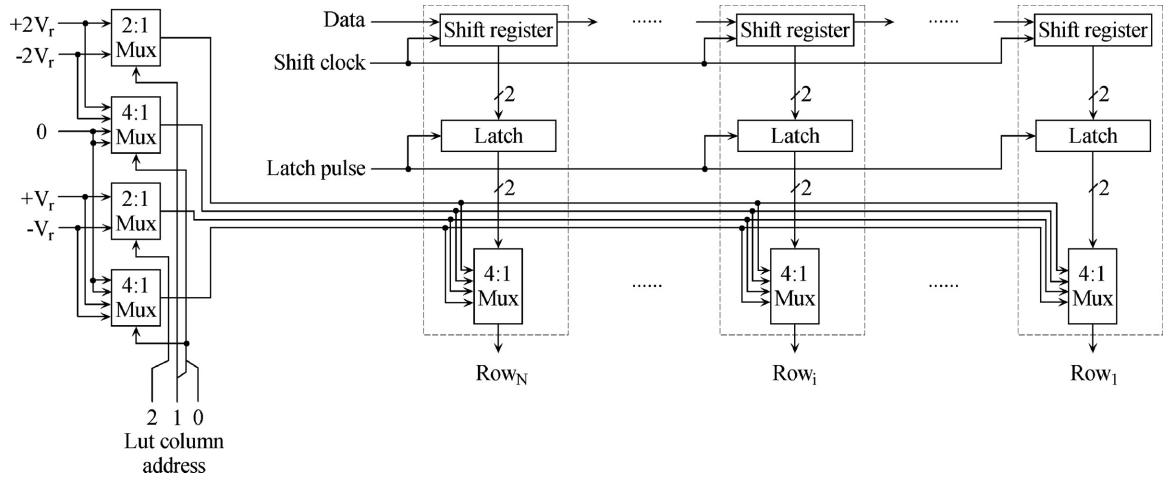

FIGURE 3 — Schematic diagram of a row driver with reduced hardware.

five voltages are adequate at a given instant of time as evident from the matrix in Eq. (1). A custom-built row driver consisting of a 2-bit shift register, a 2-bit latch, and a 4:1 multiplexer in each stage can be used along with a few multiplexers (4:1 and 2:1, two each) that are common to all the stages in the driver as shown in Fig. 3. Elements of the matrix in Eq. (1) are stored in the form of a look-up table (LUT) in the controller. Hence, the column address of the LUT can be used to select one set of four voltages (corresponding to the select vector) as the inputs of 4:1 multiplexers in each stage of the driver. The data in this case will be the LUT row address itself and is shifted into the 2-bit shift register of the driver. In a display with N rows, $2N$ flip-flops (N flip-flops of the shift register and N flip-flops of the latch), and N analog switches and the associated logic to select them can be saved when the driver is custom made. The number of voltages is just three when the matrix in Eq. (16) is used for selecting the rows in the display. Hence, additional N analog switches can be saved if the display is scanned with select vectors of the matrix in Eq. (16).

3.2 Column driver

The number of voltages in the column waveforms is 11, *viz.* ($\pm 5V_c$, $\pm 4V_c$, $\pm 3V_c$, $\pm 2V_c$, $\pm V_c$, and 0). Here, either six or five voltages are necessary at a given instant of time, depending on the select vector. The voltages ($\pm 5V_c$, $\pm 3V_c$, and $\pm V_c$) are used when the first, second, fifth, and sixth columns of the matrix in Eq. (1) are the select vectors. The column voltages are ($\pm 4V_c$, $\pm 2V_c$, and 0) when the rows are selected with the remainder of the select vectors. These two sets of voltages can be multiplexed using multiplexers that are located external to the driver. One possible solution to reduce the hardware in the column driver is shown in Fig. 4. Here, a standard column (data) driver with a 3-bit shift register, a 3-bit latch, and an 8:1 multiplexer for each column is sufficient in place of a driver with a 4-bit shift register, a 4-bit latch, and an 11:1 multiplexer for each output. A PCB with twelve 74595 (8-bit serial-in parallel-out shift register with output latches) and thirty-two 4051 (8:1 multiplexer, one for each output) is used as the column driver. The shift registers are cascaded

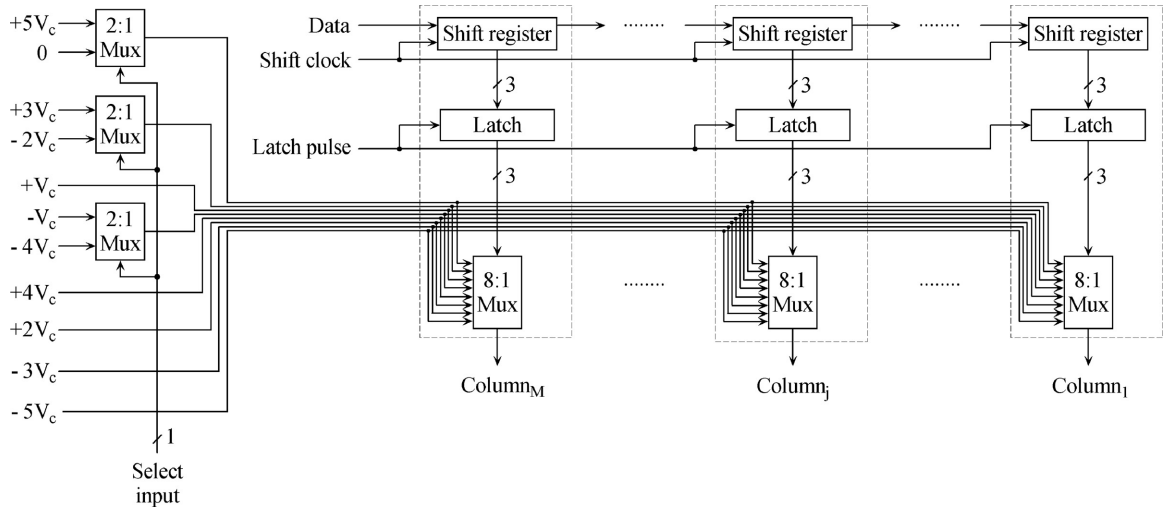

FIGURE 4 — Schematic diagram of a column driver with reduced hardware.

serially by using their serial inputs and outputs. The most significant bit of the 3-bit column signal (data which selects the appropriate voltage for a column) is shifted-in first followed by two other bits. The latched outputs of 74595 are used as the select lines of the 8:1 multiplexers to drive each column with one of five or six voltages. The middle bit of the LUT column address is used for multiplexing these voltages. Because only five or six voltages are necessary at any time, a custom-designed driver with a 3-bit shift register, a 3-bit latch, and a 6:1 analog multiplexer for each column can further reduce the hardware in the driver (two analog switches and necessary logic to select them for each column in the display). The least significant bit of the data (output of the 4-bit dot product) is the select input of the external multiplexers and the other 3 bits are shifted into the shift register of the column driver. In summary, 2M flip-flops and 5M analog switches can be saved in a display with M columns. When the matrix in Eq. (16) is used for scanning, then two sets of voltages, *viz.* $(\pm 2\sqrt{2}V_c, 0)$ and $[+(1 \pm \sqrt{2})V_c, -(1 \pm \sqrt{2})V_c]$, are multiplexed, depending on the select vector. The first set of three voltages is fed to the driver when the first six select vectors are used for scanning the rows. The second set of four voltages is used when the last two columns of the matrix in Eq. (16) are the select vectors. A column driver that is capable of applying one out of four voltages with a 2-bit shift register, a 2-bit latch, and a 4:1 analog multiplexer for each column can be used. Hence, a further reduction of 2M flip-flops and 2M analog switches can be achieved compared to that of the driver that is capable of applying any one of the six voltages.

3.3 Voltage-level generator

The five voltage levels ($\pm 2V_r$, $\pm V_r$, and 0) in the row waveforms, corresponding to the elements of the orthogonal matrix and the 11 voltages in the column waveforms ($\pm 5V_c$, $\pm 4V_c$, $\pm 3V_c$, $\pm 2V_c$, $\pm V_c$, and 0), are generated in the voltage-level generator (VLG). They are fed to the respective drivers through the external multiplexers. The resistor network shown in Fig. 5 is used to generate these voltages. A similar voltage level generator that generates the voltages $(\pm\sqrt{2}\ V_r, \pm V_r, 0)$ and $[\pm 2\sqrt{2}V_c, 0, \pm(1 \pm\sqrt{2})V_c]$ is necessary when the matrix in Eq. (16) is used for scanning the display.

3.4 Address generator

A 16-bit binary counter forms the core of the controller. It is used to generate the address to fetch data from the buffer memory, pick the select vector, route the select vector in to the row driver, generate the column signal, generate control signals to shift and latch data in the row and column drivers, select signals to the multiplexers to connect some voltages from the voltage-level generator to the drivers depending on the select vector, *etc*. The number of rows in a subgroup is chosen to be four (an integer power of two). It is possible

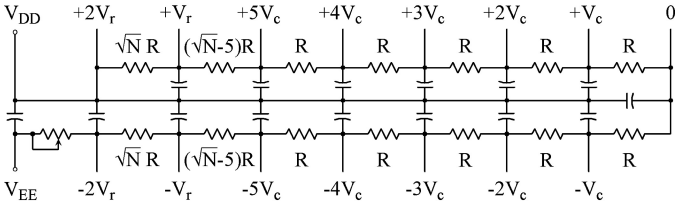

FIGURE 5 — Voltage-level generator.

to achieve the same results by having subgroups with three rows and using the matrix in the following equation.

$$O_{(3\times 8)} = \begin{bmatrix} +2 & +2 & -2 & -2 & +2 & +2 & -2 & -2 \\ +2 & -2 & +1 & -1 & +2 & -2 & +1 & -1 \\ +1 & +1 & +1 & +1 & -1 & -1 & -1 & -1 \end{bmatrix}. \quad (22)$$

However, the hardware necessary to generate the address to fetch the data from the memory will be more complex compared to having four rows in a subgroup. A binary counter can be the central core of the controller, and all other signals can be generated by tapping the appropriate outputs of the counter and by using some simple logic circuit when four rows are grouped in to a subgroup. The generation of control signals *viz.*, shift clock, latch, is simple when the number of rows (N) and number of columns (M) are an integer power of two.

The least-significant bit (C_0) of the master counter is used for generating control signals such as the shift clock, latch pulse, *etc*. Bits 1 and 2 ($C_1 - C_2$) are used as row addresses of any subgroup. The next five bits from bit 3 to bit 7 ($C_3 - C_7$) are the column address lines. Bits 8 to 10 ($C_8 - C_{10}$) can be used for selecting each subgroup with only one of the select vectors and another subgroup is selected next. The controller is designed to select each subgroup with 2^i (i is any one of six values in the range 0 to 5) select vectors consecutively before selecting another subgroup. Hence, the subgroup address is modified using a 3-bit binary switch and three 1-of-6-line data selectors. Three bits out of eight MSBs ($C_8 - C_{15}$) of the master counter are selected from three 1-of-6-line data selectors to be used as the subgroup address of the memory. A single 1-of-6 data selector will be sufficient if we use the output of the data selector as clock to a 3-bit counter whose outputs form the subgroup address. Hence, two 1-of-6 data selectors can be saved by using three flip-flops. Thus, depending on the availability of resources, one can design by using more product terms or alternatively by using registers. Elements of the matrix in Eq. (1) are stored in the form of a look-up table (LUT) in the controller. Each element is addressed with a 5-bit address that is shown in Table 2. A general method of implementing an address for a LUT is shown in Fig. 6(a). Bits 8–15 of the counter chain are used for generating these address lines. Two counters that keep the count of the row and column address of the LUT are loaded with the outputs of the counter chain. Data selectors are used to select the appropriate bits to these counters using the MSB of the binary switch. Counters are loaded at the first subgroup selection when the MSB of the binary switch (B_2) is at logic 0, to apply 1 or 2 or 4 or

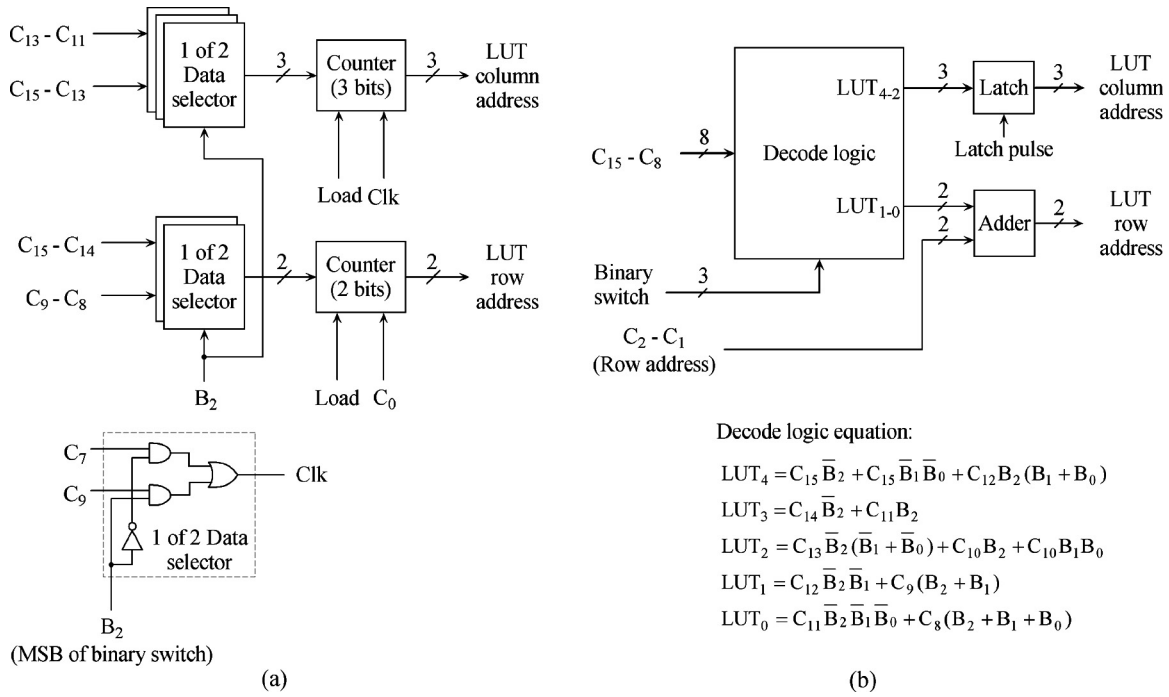

FIGURE 6 — Address generators for the LUT; (a) using data selectors and counters, (b) using decoder and adder.

8 select pulses consecutively for each subgroup. When B_2 is at logic 1, counters are loaded at each latch edge to apply 16 or 32 select pulses subsequently for each subgroup. Since the number of rows in a subgroup is an integer power of two, the address for the LUT can be generated by just selecting the appropriate bits of the counter chain (from bit C_8 to C_{15}) using a decoder and an adder as shown in Fig. 6(b). The two-bit adder that adds row address of the memory with slowly varying 2 bits is used to achieve the rotation of the rows in the matrix. Carry is neglected in this adder. The output of this adder is the the LUT row address. LUT column address is taken after latching the output of the decoder to the latch pulse edge. While the design in Fig. 6(a) requires six registers, the design shown in Fig. 6(b) requires three registers, a half-adder, and a full adder. The generation of data for the row driver is described next.

3.5 Row signal generator

Only one of the subgroups is selected with voltages corresponding to a select vector while the remaining subgroups are grounded. Data corresponding to the non-select voltage is shifted into $(N - 3)$ stages of the shift register in the row driver. Data corresponding to three non-zero select voltages are routed from the three non-zero elements of the select vector to the driver. Elements of the orthogonal matrix are stored in the form of a LUT, and they are read out sequentially. The least-significant three bits of column address are compared to the subgroup address to select the data from LUT as the row signal. Data selectors are used to select the data (corresponding to select and non-select voltages) to the shift register in the row driver. We have shown that a custom-built row driver can reduce hardware (see Fig. 3). Two 1-of-2-line data selectors will be sufficient as the data shifted into the shift register is the 2-bit row address of the LUT. Data selectors feed data corresponding to a select vector for a selected subgroup and gives out data corresponding to the non-select voltage for the remainder of the rows. The generation of the column signal is described next.

TABLE 2 — Look-up table.

MSBs / LSBs	000	001	010	011	100	101	110	111
00	+2	+2	-2	-2	+2	+2	-2	-2
01	+2	-2	0	0	+2	-2	0	0
10	+1	+1	+1	+1	-1	-1	-1	-1
11	0	0	+1	-1	0	0	+1	-1

3.6 Column signal generator

The column voltage is proportional to the dot product of the row select and data vectors. Hence, data for the column driver (also called column signal) can be generated by multiplying the select vector with the sign of the data assigned to the bit (because the data is either a +1 or a –1) and summing it in the accumulator during four clock cycles. A schematic of the column signal generator that uses a multiplier-accumulator circuit is shown in Fig. 7. Here, the accumulator is cleared whenever data of a new column is fetched (*i.e.*, when the row address is 00). This requires a 4-bit accumulator, a 1-of-4-line data selector, and additional

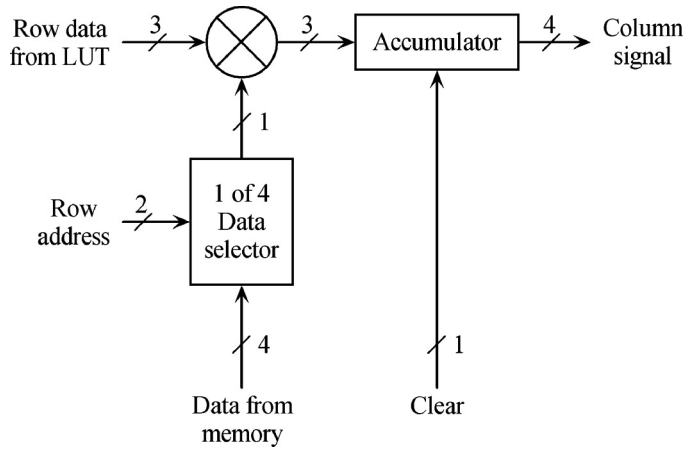

FIGURE 7 — Column signal generator using a multiplier and an accumulator.

logic for the multiplier. The most-significant 3 bits of the column signal are shifted-in to the shift register of the column driver while the least significant bit is used as the select line in the external 2:1 multiplexers. Hardware implementation of the multiplier for multiplying 3 bits of the elements of the select vector by the sign bit (data) using logic circuit is shown in Fig. 8. Another possible implementation is based on the fact that the 1-bit multiplication reduces to just addition or subtraction. Hence, the data bit could be used to add or subtract the value of an element in the select vector during four clock cycles.

An even simpler implementation is possible by recognizing the fact that a voltage corresponding to the dot product has to be applied to the pixels, and information about the select vector and the data of the pixels could be used to select the appropriate voltages that are to be applied to the column electrodes. Hence, it is not necessary to compute the column data as long as the data is routed as select signals to select the appropriate column voltage for a given select and data pattern.[5] We have modified the computation block

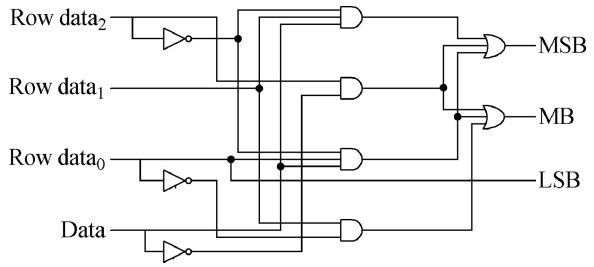

FIGURE 8 — Logic diagram of 3-bit sign multiplier.

with a 1-of-4 AND-OR selector (data selector), an XOR gate, a decoder, logic gates, and a 3-bit register as shown in Fig. 9. The 1-of-4 data selector selects the data bit corresponding to the row-select element as given in matrix of Eq. (2). The XOR gate is used to multiply the sign of the select element with that of the data. The data (column) voltages that are to be applied will be same for a select vector and its rotated vectors. The 1:1 correspondence among the elements of the select vector and the data bits are retained even when the select vector is rotated. A decoder at the output of the XOR gate keeps the order of the bits with its weight so that the data that is being shifted to the driver will be the same for a select vector and its rotations, *i.e.*, A always gets d_3, B gets d_2 when the LUT address bit 3 is low, d_1 otherwise, and C always gets d_1 or d_0 depending on the LUT address bit 3. Outputs of the decoder can be directly routed to register inputs, in which case the number of analog 2:1 multiplexers common to the column driver is eight. The driver hardware has an 8:1 multiplexer in each column (as in Fig. 4). Table 3 shows the voltages that are to be applied to the column electrodes for different combinations of select and data vectors. From the table, we notice that there are two column voltages that are the same for two different data vectors for a given select vector. For example, if the select vector is $[+2V_r, +2V_r, +V_r, 0]$, then the column voltage is $+V_c$, when the data vector is either 010 or 100 and it is $-V_c$, when the data vector is either 011 or 101; the column volt-

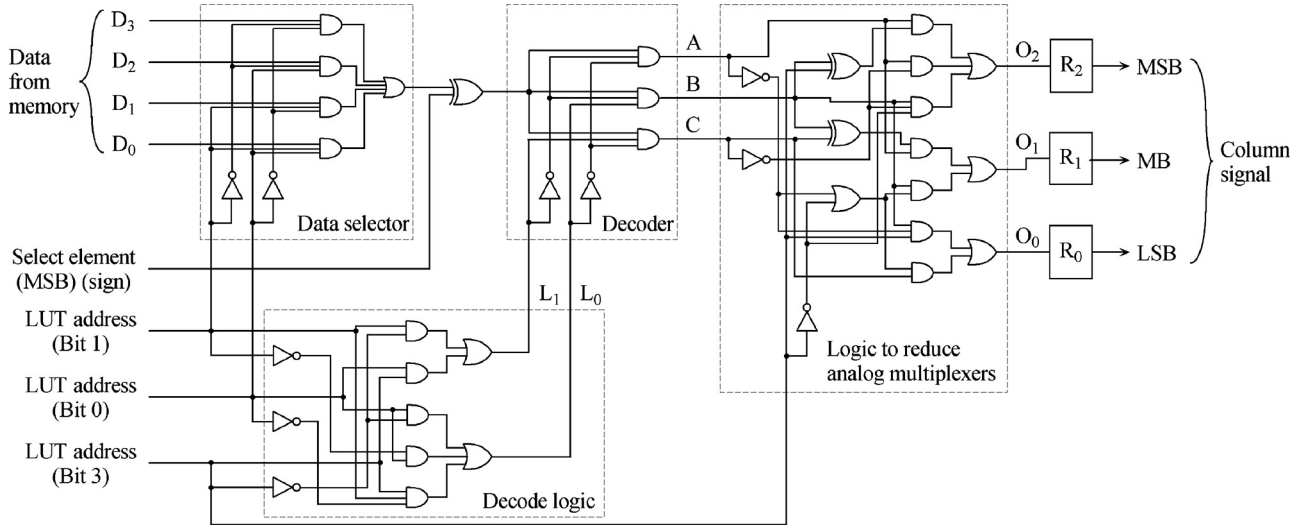

FIGURE 9 — Column signal generator that is based on LUT.

TABLE 3 — Column voltages *vs.* select vectors.

Select vector \ Data vector	000	001	010	011	100	101	110	111
[+2, +2, +1,0]	$+5V_e$	$+3V_e$	$+V_e$	$-V_e$	$+V_e$	$-V_e$	$-3V_e$	$-5V_e$
[+2, -2, +1,0]	$+V_e$	$-V_e$	$+5V_e$	$+3V_e$	$-3V_e$	$-5V_e$	$+V_e$	$-V_e$
[+2, 0, +1,+1]	0	$-2V_e$	$-2V_e$	$-4V_e$	$+4V_e$	$+2V_e$	$+2V_e$	0
[+2, 0, +1,-1]	$-2V_e$	0	$-4V_e$	$-2V_e$	$+2V_e$	$+4V_e$	0	$+2V_e$
[+2, +2, -1,0]	$+3V_e$	$+5V_e$	$-V_e$	$+V_e$	$-V_e$	$+V_e$	$-5V_e$	$-3V_e$
[+2, -2, -1,0]	$-V_e$	$+V_e$	$+3V_e$	$+5V_e$	$-5V_e$	$-3V_e$	$-V_e$	$+V_e$
[+2, 0, -1,+1]	$-2V_e$	$-4V_e$	0	$-2V_e$	$+2V_e$	0	$+4V_e$	$+2V_e$
[+2, 0, -1,-1]	$-4V_e$	$-2V_e$	$-2V_e$	0	0	$+2V_e$	$+2V_e$	$+4V_e$

age is different for the remainder of the data vectors. The number of analog switches in each column of the driver can be reduced from eight to six by eliminating this redundancy, and hence the driver can be custom designed with a 6:1 multiplexer for each column. The number of multiplexers that are external to the driver is also reduced from eight to five with additional logic between the decoder output and register input.

3.7 Control signals

Control signals such as the shift clock and latch are also generated in the controller. The column signal is ready once the data of a column (only four-pixel data belonging to the selected subgroup) is fetched from memory. Three shift clocks are generated to shift the column signal serially each time the row address is 00, 01, and 10. When the row address is 11, the output of the column signal generator is loaded on to the registers. The counter bit 0 (C_0) is used as the shift clock for the row driver when the two MSBs of the column address is 11. The latch pulse is generated after shifting the column signal corresponding to all of the 32 columns and row data corresponding to all the 32 rows.

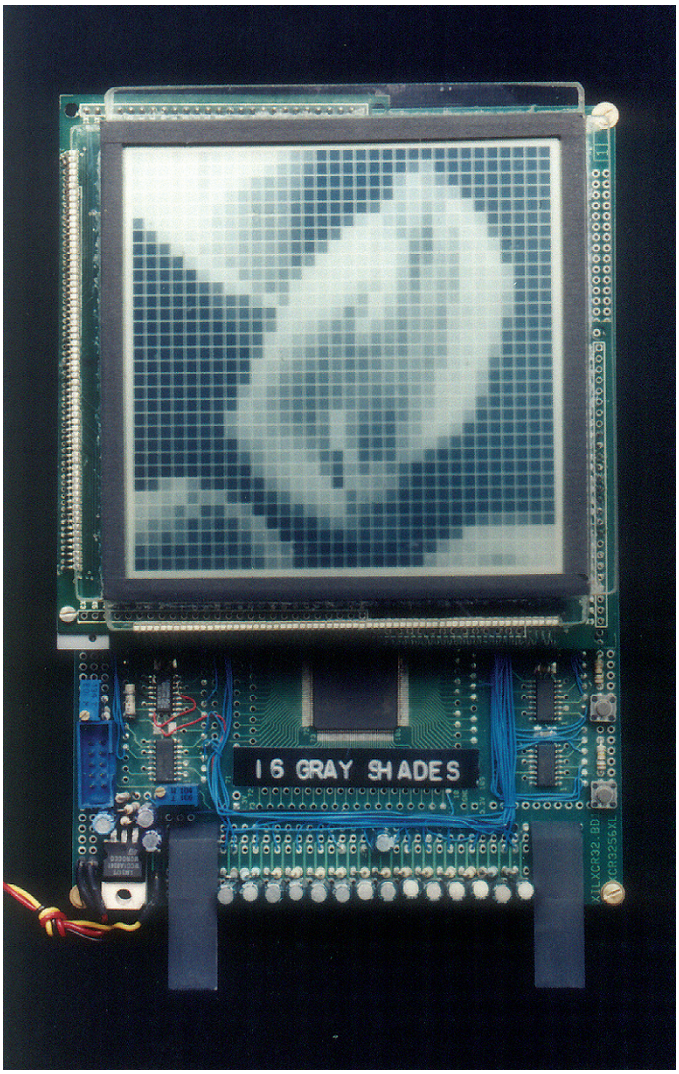

FIGURE 10 — Photograph of the prototytpe. It is capable of displaying 16 gray shades using the wavelet-based addressing technique.

4 Results

A prototype that is capable of displaying 16 gray shades using the wavelet-based addressing technique is demonstrated. A controller has been implemented using 63 macro-cells, 147 product terms, and 49 registers in a low-cost complex programmable logic device (CPLD). The photograph of the prototype is shown in Fig. 10. Typical addressing waveforms that were captured using an oscilloscope are shown in Fig. 11. The top and middle waveforms correspond to the row and column, respectively, while the waveform across the pixel (row waveform minus column waveform) is shown at the bottom. The response times (time to switch the state of pixels in the display from one gray shade to another) were measured using a cell (6.2 μm) filled with RO-TN 605C (liquid-crystal mixture) using the waveforms generated in the prototype. The rise and fall times were measured when the light transmission in the cell crosses 10% and 90% of the total change in transmission while switching from one gray shade to another. Table 4 shows the response times in milliseconds when the pixels are switched from one gray shade to another when all the select patterns are distributed by selecting each subgroup with only one select vector at a time (as in Fig. 11). The response of the cell was also measured

TABLE 4 — Response times of the cell when pulses are distributed.

Gray shade value	0 (OFF)	3	5	7	9	11	13	15 (ON)
0 (OFF)	X	84	80	75	78	74	68	71
3	80	X	67	69	72	68	72	73
5	78	62	X	64	68	66	69	72
7	74	65	60	X	59	67	65	71
9	76	69	64	52	X	58	60	68
11	74	65	62	63	55	X	47	64
13	68	70	66	60	56	50	X	58
15 (ON)	69	69	68	66	64	60	55	X

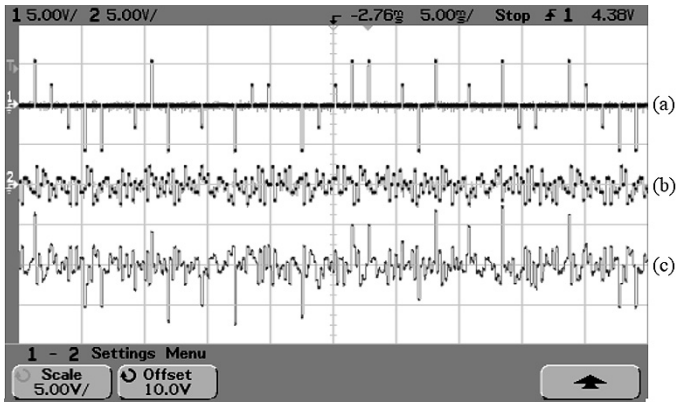

FIGURE 11 — Typical waveforms of the wavelet-based addressing technique, (a) row waveform, (b) column waveform, and (c) waveform across a pixel.

by selecting each subgroup at a time with 2, 4, 8, 16, and 32 select vectors. The sequence of scanning did not change the response times significantly. The measured values when all 32 select patterns are clustered (as in Fig. 1) are given in Table 5. The upper triangle in these tables shows the rise times and the lower triangle shows the fall times. The rise and fall times were measured to be 50 and 15 msec, respectively, when the pixel was switched between the ON and OFF states using square waveforms with RMS voltages of V_{ON} (2.10 V) and V_{OFF} (1.75 V, the threshold of the liquid-crystal mixture), the voltages correspond to 32-line multiplexing. A typical response when the pixel is switched back and forth between the ON and OFF states is shown in Fig. 12. Figure 12(a) shows the response when select vectors are distributed, while the electro-optic response when all the 32 select pulses are applied consecutively to a subgroup is shown in Fig. 12(b).

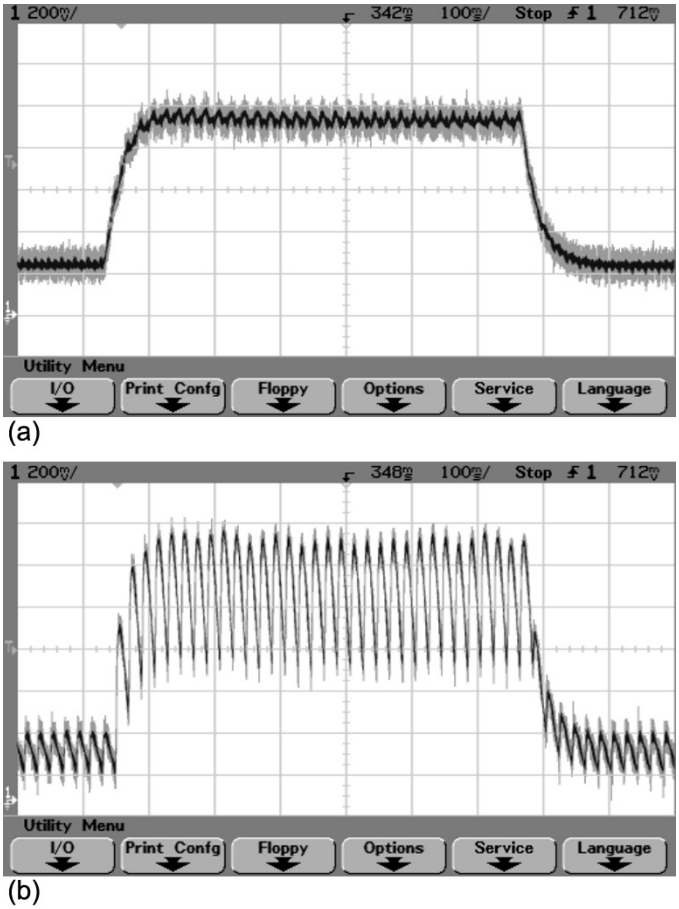

FIGURE 12 — Typical response of a pixel when switched between ON and OFF states, when a subgroup is selected with (a) one select vector and (b) 32 select vectors sequentially.

5 Summary

Amplitude modulation[2] would require three voltages in the row waveform, 30 voltages in the column waveform, and 4*N* time intervals to display 16 gray shades. Successive approximation[6] requires nine voltages on the row side and 13 voltages on the column side when used in combination with the multi-line addressing technique (MLA) by selecting four rows. The wavelet technique described here has five voltages in the row and 11 voltages in the column waveforms. Both successive approximation and wavelet techniques have 8*N* time intervals, and the supply voltage is also the same when the number of rows is above 16. Although there are five and 11 voltages present in the row and column waveforms, at any time interval only four in the row and five or six in the column are applied to the respective electrodes. These voltages have been multiplexed externally, hence there is a significant reduction in the hardware of the row and column drivers. In the row driver, a 20% savings in the analog switches and associated logic and 33% savings in flip-flops for the shift register and latches can be achieved. For the column driver, about 45% savings in the analog switches and associated logic and 25% savings in flip-flops of the shift register and latches can be obtained. Because the number of rows in a subgroup is an integer power of 2, address generation and other control signals generation is simple. We have also shown the possibility of eliminating the computation in the generation of a column signal in the controller. The three data bits in the data vector are routed to the column driver through data selectors that reduce the hardware

TABLE 5 — Response times of the cell when pulses are clustered.

Gray shade value	0 (OFF)	3	5	7	9	11	13	15 (ON)
0 (OFF)	X	60	67	67	65	63	62	60
3	60	X	55	58	66	62	50	58
5	64	40	X	60	63	58	50	50
7	71	59	60	X	59	58	49	49
9	68	71	60	51	X	50	45	43
11	61	62	60	60	55	X	40	46
13	60	68	61	60	42	44	X	50
15 (ON)	60	50	50	48	47	40	40	X

required to compute the column signal. Although the supply voltage and the number of time intervals are comparable to that of the successive approximation technique when the number of gray shades is 16, the wavelet technique has a smaller number of time intervals and lower supply voltage when the number of gray shades is greater than 16.[7] About 30% savings in supply voltage over successive approximation techniques can be achieved when the matrix in Eq. (16) is used to scan the display. Here, successive approximation using two-line multi-line addressing is considered to be a fair comparison to the wavelet technique because the matrix of orthogonal wavelets in Eq. (16) is also used in order to select two rows simultaneously. The successive approximation requires row drivers with three voltage-level selection and column driver with three-voltage-level selection, the wavelet technique requires a row driver with three-voltage-level selection and a column driver with four-voltage-level selection. The clock frequency can also be reduced by 33% when two rows are selected compared to the four-row selection technique. With four rows in a set, the controller requires three memory fetches (because of only three non-zero elements) in generating the column signal of a column where it is two fetches with two rows in the set. However, with two rows in the set, it requires a large number of time intervals when more than 32 gray shades are to be displayed, and hence it may be better to construct a matrix with four rows. Hence, we have described the controller for the wavelet-based technique with four rows in a subgroup. The hardware implementation described in this paper could be used with simple modification for displaying large gray shades using wavelets.

6 Conclusion

Design and implementation of the driver circuit of the wavelet-based addressing technique (WAT) has been presented along with several possible approaches to the implementation of the sub-blocks. Simple techniques for reducing the hardware complexity have been presented. We hope that it will be useful for an efficient implementation of the drive electronics of the wavelet-based addressing techniques.

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