Reducing Power Consumption in Liquid-Crystal Displays

T. N. Ruckmongathan, M. Govind, and G. Deepak

***Abstract*—Power consumption in liquid-crystal displays is analyzed by including frequent polarity reversals and duty-cycle control. A multistep voltage profile is proposed to reduce the power consumption of multiplexed and nonmultiplexed displays. The authors have also shown that the reduction in the power consumption can be achieved with a minimal increase in hardware complexity of the drive electronics.**

***Index Terms*—Addressing, displays, liquid-crystal displays (LCDs), multiplexing and scanning, multisteps, power-consumption.**

I. Introduction

LIQUID-CRYSTAL displays (LCDs) consume less power as compared to other display devices. They are also flat panel devices with negligible depth. LCDs can be operated with low voltage power sources and, hence, are extensively used in portable products. Although LCDs consume less power, it is desirable to reduce the power consumption further so that the frequency of replacing or charging the cells in portable equipment is reduced. It is well known that the power dissipated in a resistor while charging a capacitor in an RC circuit is less, when a staircase waveform with peak amplitude of V is used instead of a step (single) waveform of amplitude V. We have used this fact to reduce the power consumption in LCDs.

II. Background

Marks [1] has shown that the power consumption of nonmultiplexed displays can be reduced to about 50% when the charge across the pixels is discharged by shorting the two electrodes for a short time interval before charging the pixels to a voltage with opposite polarity. He has also analyzed and estimated the power consumption in multiplexed LCDs [2], based on the model of the matrix display shown in Fig. 1. Each pixel in the LCD is represented as a capacitor. One electrode of the pixel is connected to a row address line, and the other electrode is connected to a column address line. The capacitance of the pixel depends on the state of the pixel since the effective dielectric constant is determined by the orientation of the liquid-crystal molecules. The capacitance of the ON pixel C_{ON} is at least twice the capacitance of the OFF pixel C_{OFF} in nematic LCDs because the dielectric constant of the rod-like liquid-crystal molecules is higher when measured parallel to its long axis as compared to the other two perpendicular directions.

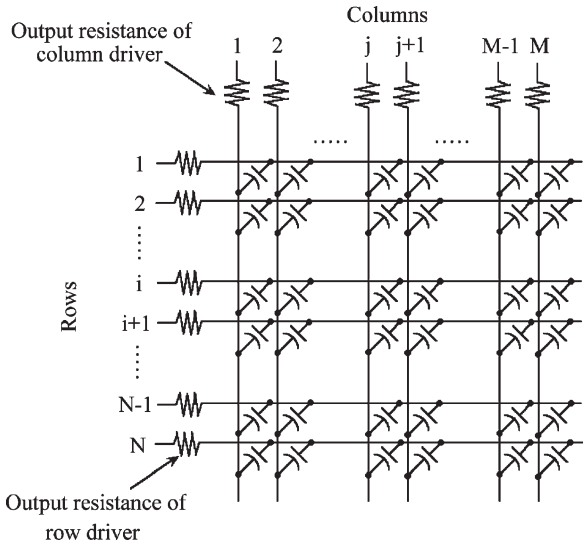

Fig. 1. Model of matrix display used for computing power consumption.

Display drivers are used to apply the waveforms to the rows and columns of the matrix display. The power consumption of the panel is the power dissipated in the resistors while charging and discharging the pixels to voltages as dictated by the addressing technique. Marks [2] has estimated the power consumption in a matrix display driven by the conventional line-by-line addressing [3] when the worst case pattern that consists of alternate ON and OFF pixels is displayed. He has shown that the power consumed by the multiplexed display is proportional to N^2M. Here, N is the number of lines multiplexed, and M is the number of columns in the matrix display. This analysis is restricted to just one polarity inversion per frame. Frequent polarity reversal is introduced in the addressing waveforms to improve the brightness uniformity of the display. It induces transitions in places where there were no transitions and suppresses transitions in some other places. The polarity of the addressing waveforms is changed after scanning the few address lines in most of the passive matrix LCDs. We have extended the analysis of power consumption in the line-by-line addressing technique by including polarity inversion as an additional parameter.

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TABLE I
VOLTAGE TRANSITIONS ACROSS PIXELS IN LINE-BY-LINE ADDRESSING

State of the pixel in		Voltage swing across the pixels in		
row (i)	row $(i+1)$	row (i)	row $(i+1)$	other rows
ON	ON	V_r (V_r+2V_c)	V_r (V_r+2V_c)	0 $(2V_c)$
ON	OFF	V_r+2V_c (V_r)	V_r-2V_c (V_r)	$2V_c$ (0)
OFF	ON	V_r-2V_c (V_r)	V_r+2V_c (V_r)	$2V_c$ (0)
OFF	OFF	V_r (V_r-2V_c)	V_r (V_r-2V_c)	0 $(2V_c)$

III. ANALYSIS OF LINE-BY-LINE ADDRESSING WITH MULTIPLE POLARITY INVERSIONS IN A FRAME

Let V_r and V_c be the amplitudes of the row and column voltages. Let n_p be the number of polarity inversions in a frame (Marks had assumed $n_p = 1$ in his analysis) and f be the frame frequency of the line-by-line addressing. Let $C_{\rm ON}$ and $C_{\rm OFF}$ be the capacitance of the pixels in ON and OFF states, respectively. Table I gives the voltage transition across the pixels based on the two neighboring pixels in a column when row (i) is unselected, and row $(i+1)$ is selected. These transitions depend on the state of the pixels in rows (i) and $(i+1)$, as well as the polarity inversion. The voltage transitions when a polarity inversion is introduced are shown within the parentheses.

Case 1: The power consumed by a blank screen when all the pixels are OFF. The power consumed in a column during a transition, i.e., when row $(i+1)$ is selected, and the polarity of the voltages applied to the two rows remains unchanged is as follows:

$$P_{\rm tran.} = \frac{C_{\rm OFF}V_r^2}{2} + \frac{C_{\rm OFF}V_r^2}{2} + (N-2)C_{\rm OFF}(0) = C_{\rm OFF}V_r^2. \quad (1)$$

The first term corresponds to the power dissipated while discharging the pixel in row (i) from $V_r - V_c$ to $-V_c$, and the second term corresponds to charging the pixels in row $(i+1)$ from $-V_c$ to $V_r - V_c$, while the third term corresponds to the rest of the $(N-2)$ pixels in a column without any change in the voltage across them. Similarly, the power dissipated when the polarity of the select voltage changes is given in (2)

$$P'_{\rm tran.} = \frac{C_{\rm OFF}(V_r-2V_c)^2}{2} + \frac{C_{\rm OFF}(V_r-2V_c)^2}{2} + (N-2)\frac{C_{\rm OFF}(2V_c)^2}{2}. \quad (2)$$

The power consumption in a column during a frame is given by

$$P_{\rm column}({\rm frame}) = (N-n_p)P_{\rm tran.} + n_p P'_{\rm tran.}. \quad (3)$$

The power consumed by the whole display panel is obtained by multiplying (3) by M, the number of columns in the display, and f, which is the frame frequency, as shown in the following equation:

$$P_{\rm ALL\_OFF} = MC_{\rm OFF}V_c^2\left(N^2 + n_p(2N - 4\sqrt{N})\right)f. \quad (4)$$

Case 2: The power consumed by a blank screen, when all the pixels are ON, is given in the following expression:

$$P_{\rm ALL\_ON} = MC_{\rm ON}V_c^2\left(N^2 + n_p(2N + 4\sqrt{N})\right)f. \quad (5)$$

Case 3: The power consumed when a checkerboard pattern is displayed is given in (6). Here, the number of pixels in ON and OFF states is equal, and the neighboring pixels in the vertical as well as the horizontal direction are in the opposite states

$$P_{\rm ON\_OFF} = \frac{MV_c^2}{2}\Big[C_{\rm ON}\left(3N^2 + 4N\sqrt{N} - n_p\,(2N + 4\sqrt{N})\right) + C_{\rm OFF}\left(3N^2 - 4N\sqrt{N} - n_p(2N - 4\sqrt{N})\right)\Big]f. \quad (6)$$

We have also introduced a duty cycle in the pulses of the line-by-line addressing technique. The power consumption after the inclusion of the duty cycle is analyzed and compared in the next section.

IV. LINE-BY-LINE ADDRESSING WITH DUTY-CYCLE CONTROL

The power consumed by the display panel depends on the number of transitions in the voltage across the pixels and the magnitude of these transitions. The number of transitions in turn depends on the image being displayed and the addressing technique. The number of transitions in the addressing waveform can be made independent of the image if the voltage in the row and column waveforms is chosen to be the same for a fraction (T_0) of the row select time T. This introduces transitions in both row and column waveforms, and the voltage across the pixel is zero during the interval T_0. The amplitude of the row and column waveforms has to be increased by a factor $[T/(T-T_0)]^{1/2}$ to ensure that the rms voltage across the pixel is the same as that of the conventional line-by-line addressing technique. This technique will be referred to as line-by-line addressing with duty-cycle control. An introduction of a duty cycle has the advantage of good brightness uniformity of pixels [4]. Although the number of transitions is the same across all pixels, the power consumption depends on the number of pixels in the ON and OFF states because the capacitance of the pixel depends on its state. The power consumption of the multiplexed display driven by line-by-line addressing when 50% of the pixels are driven to ON state is given in (7)

$$P_{\text{line-by-line with duty cycle}} = MV_c^2X\left(\frac{T}{T-T_0}\right)f. \quad (7)$$

Wherein

$$X = \left[C_{\rm ON}(N^2 + N\sqrt{N}) + C_{\rm OFF}(N^2 - N\sqrt{N})\right]. \quad (8)$$

The power consumption (as a function of N) of a display driven by the line-by-line addressing with duty cycle is compared with that of a display driven by the conventional line-by-line addressing in Fig. 2. This comparison is done when the three specific patterns (case 1–3) are displayed. These plots are based on the assumption that $C_{\rm ON} = 2C_{\rm OFF}$ and $T_0 = 0.05T$. Least

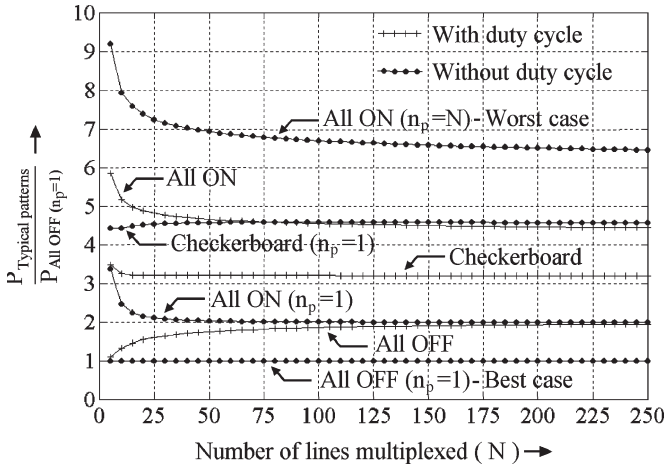

Fig. 2. Plots of normalized power consumption in matrix displays driven by line-by-line addressing with duty-cycle control and the conventional line-by line addressing without duty-cycle control and n_p polarity inversions in a frame.

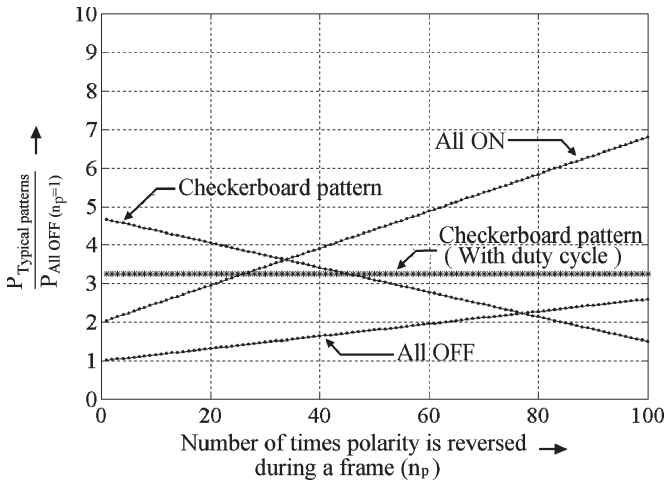

Fig. 3. Plot of normalized power consumption as a function of n_p, the number of polarity inversions in a frame ($N = 100$). These plots are normalized to power consumed when the screen is blank and n_p is one.

amount of power is consumed when all the pixels in the display are OFF, and the number of polarity reversals in a frame (n_p) is one. Hence, the power consumption is normalized to the minimum power in these plots.

The normalized power consumption as a function n_p, the number of polarity inversions in a frame (when N, the number of lines multiplexed, is 100), is plotted in Fig. 3. The power consumption while displaying blank pattern increases with n_p because the number of transitions in the waveforms increases with the n_p. In case of the checkerboard pattern, the power consumption decreases with n_p due to a decrease in the number of transitions with an increase in n_p. The power consumption of the line-by-line addressing technique with duty-cycle control is also shown in Fig. 2. The power consumption of the line-by-line addressing with duty-cycle control also depends on the image because the capacitances of the ON and OFF pixels are not equal, although the number of transitions in the addressing waveforms is equal. An introduction of a duty cycle improves the brightness uniformity of the pixels in the display because

TABLE II
NORMALIZED POWER CONSUMPTION FOR SOME TEST IMAGES

Image	Line-by-line addressing with duty cycle control ($T_0 = 0.05\,T$)	Line-by-line addressing with n_p polarity reversals per frame (without duty cycle)			
		$n_p = 1$	$n_p = 25$	$n_p = 50$	$n_p = 100$
	3.3917	2.3911	2.7849	3.2277	4.0621
	3.8911	2.2777	2.9791	3.7014	5.1211
	2.9960	1.5913	2.2226	2.8566	4.1311
	3.8370	2.2219	2.9283	3.6480	5.1037
	3.3553	1.8255	2.4867	3.2064	4.5881

the waveforms across all the pixels are distorted to the same extent (since the number of transitions is equal), and the reduction in the rms voltage across the pixels can be compensated by just increasing the peak amplitude of the pulses. We have also considered some typical images of size 100 × 100 pixels, and we have estimated the power consumption when these images are displayed. The results are summarized in Table II.

The power consumptions shown in the Table II are normalized to that of the blank pattern with all the pixels in OFF state and having just one polarity reversal per frame. It is evident from the table that the power consumption of line-by-line addressing when the duty-cycle control is introduced is about the same as that of the line-by-line addressing, wherein the polarity is reversed after scanning two-address lines. Analysis presented in this section implies that the introduction of duty cycle will not reduce the power consumption in multiplexed matrix LCDs, although it is quite effective in reducing the power consumption in nonmultiplexed displays. The principle of a new technique to reduce the power consumption in multiplexed as well as nonmultiplexed displays is presented next.

V. PRINCIPLE OF REDUCING POWER CONSUMPTION

It is well known that the power dissipated in the resistor while charging or discharging a capacitor in an RC circuit using a single step of amplitude V_p is given by $CV_p^2/2$. Hence, the total power consumed during a charge–discharge cycle is CV_p^2. Now, if the capacitor is charged and discharged using two steps, each of the amplitude $V_p/2$, then the power consumption will be $CV_p^2/2$, i.e., 50% of the power dissipated as compared

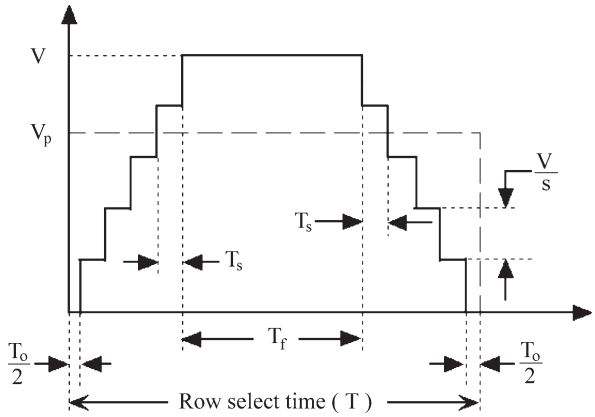

Fig. 4. Multistep voltage profile that will replace a pulse of amplitude V_p in the addressing techniques.

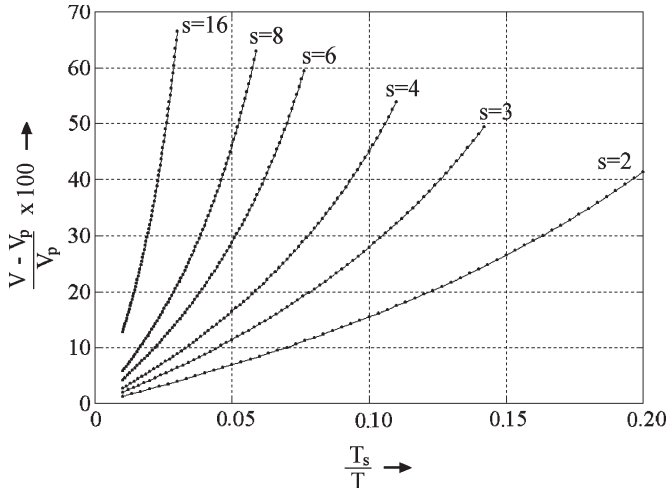

Fig. 5. Plot of the percentage increase in the maximum amplitude of the multistep voltage profile for several values of "s," which is the number of steps in a multistep voltage profile when $T_0 = T_s$, $T_f \geq 2T_s$, and $T_s \geq 0.01T$.

to a single pulse with an amplitude V_p. Similarly, the power consumption can be reduced by a factor "s" by introducing "s" steps to charge a capacitor to a voltage V_p and using an equal number of steps to discharge it to ground potential.

We propose to use the multistep voltage profile shown in Fig. 4 to reduce the power consumption in multiplexed as well as nonmultiplexed displays. It has $(s-1)$ ascending and descending steps of equal duration T_s, while the final step with a maximum voltage of V lasts for the duration T_f. The amplitude of the multistep voltage profile is zero during the period T_o. The step sizes of the ascending and the descending steps are equal (V/s), and the total period is $T = 2(s-1)T_s + T_f + T_0$. This multistep profile reduces to the single pulse of the conventional addressing technique, when $s = 1$ and $T_0 = 0$, as shown in the Fig. 4 using dashed lines. LCDs are slow-responding devices, and their response times are usually in milliseconds. The response depends on the energy delivered to the pixel, and the actual wave shape is not important as long as the period of the waveform is small as compared to the response times. Hence, the rms voltage across the pixel decides the state of the pixel. The peak amplitude (V) of the multistep voltage profile that will deliver the same energy as a pulse of amplitude V_p and of duration T can be obtained equating the RMS voltage of the multistep voltage profile to that of a pulse, as shown in (9)

$$\sqrt{\frac{1}{T}\left\{2\sum_{i=1}^{s-1}\left(\frac{V}{s}\cdot i\right)^2 T_s + V^2 T_f\right\}} = V_p \qquad (9)$$

$$\sqrt{\frac{V^2}{T}\left[\left(\frac{(s-1)(2s-1)}{3s}\right)T_s + (T - T_0 - 2(s-1)T_s)\right]} = V_p. \qquad (10)$$

Hence, the maximum amplitude of the multistep profile is

$$V = \sqrt{\frac{T}{T-T_0}\left(\frac{3s(T-T_0)}{3s(T-T_0)-(4s+1)(s-1)T_s}\right)}\cdot V_p. \qquad (11)$$

Fig. 5 shows the peak amplitude V of the multistep voltage profile as a function of the duration T_s, normalized to T for several values of "s," which is the number of steps. The peak voltage increases with T_s, and it is preferable to choose a small value for T_s. The peak voltage decreases and approaches the magnitude of a single pulse in the conventional line-by-line addressing as T_f; the duration of the maximum voltage is increased. The power dissipated in the resistor while charging and discharging a pixel (capacitor) by applying the waveform shown in Fig. 4 is given in the following expression:

$$P_{\text{multistep}} = sC\left(\frac{V}{s}\right)^2 = C\frac{T}{T-T_0}\left(\frac{3(T-T_0)}{3s(T-T_0)-(4s+1)(s-1)T_s}\right)V_p^2. \qquad (12)$$

The power consumed when a pixel is charged and discharged with a pulse of duration $(T - T_0)$ is given in (13)

$$P_{\text{pulse}} = C\left(\frac{T}{T-T_0}\right)V_p^2. \qquad (13)$$

The reduction in power consumption while using the multistep voltage profile as compared to that of a pulse is given in the following expression:

$$\frac{P_{\text{multistep}}}{P_{\text{pulse}}} = \left(\frac{3(T-T_0)}{3s(T-T_0)-(4s+1)(s-1)T_s}\right). \qquad (14)$$

This ratio of power consumption, as a function of the step width T_s normalized to the select time T, is shown in Fig. 6 for several values of "s," which is the number of steps in the multistep voltage profile.

The power consumption decreases with the increase in the number of steps (s). A good reduction in power consumption can be achieved with just two steps as long as the duration T_s is small. A large value of T_s decreases T_f (the duration of the maximum voltage V) while increasing the amplitude of V, and this is not favorable for reducing the power consumption. A line-by-line addressing technique incorporating the multistep

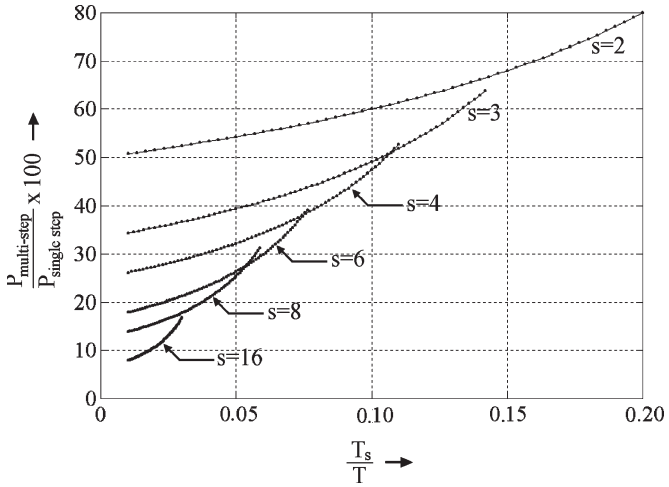

Fig. 6. Plot of ratio of the power consumption for several values of s, which is the number of steps in the multistep voltage profile. The power consumption is normalized to that of a pulse having a duty cycle ($T_0 = T_s$) with $T_f \geq 2T_s$ and $T_s \geq 0.01T$.

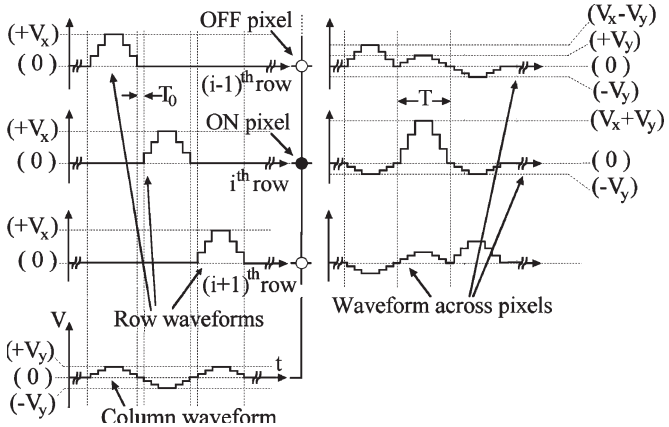

Fig. 7. Typical waveforms when multisteps are introduced in line-by-line addressing.

voltage profile is proposed in the following section to reduce the power consumption in passive matrix LCDs.

VI. Line-by-Line Addressing With Multistep Waveforms

Let us consider the conventional line-by-line-addressing technique and replace the pulses in the row and column waveforms with the multistep profiles, as shown in Fig. 7. Let V_x and V_y be the maximum amplitudes of row and column voltages. The rms voltage across a pixel is as follows:

$$V_{\text{rms}} = \sqrt{\frac{1}{NT}\left[E_{\text{select}} + (N-1)E_{\text{non select}}\right]}. \tag{15}$$

Here, E_{select} is the energy delivered to a pixel during the select interval T. The energy delivered to the pixel during the rest of the $(N-1)$ row select intervals when the other rows in the matrix are selected is given by $E_{\text{non select}}$

$$E_{\text{select}} = 2\sum_{i=1}^{s-1}\left(\frac{(V_x \pm V_y)}{s} i\right)^2 T_s + (V_x \pm V_y)^2 T_f. \tag{16}$$

The instantaneous voltage across an ON pixel is $(V_x + V_y)$, while it is $(V_x - V_y)$ across an OFF pixel. This is shown by the symbol "$\pm$" in (16)

$$E_{\text{non select}} = 2\sum_{i=1}^{s-1}\left(\frac{V_y}{s} i\right)^2 T_s + V_y^2 \cdot T_f \tag{17}$$

$$V_{\text{rms}} = \sqrt{\left(\frac{3s(T-T_0)-(4s+1)(s-1)T_s}{3sT}\right)\cdot\left(\frac{V_x^2 \pm 2V_xV_y + NV_y^2}{N}\right)}. \tag{18}$$

It can be shown that the selection ratio $[V_{\text{ON}}(\text{rms})/V_{\text{ON}}(\text{rms})]$ will be a maximum when the condition $V_x = \sqrt{N}V_y$ is satisfied.

The expression for the rms voltage across a pixel in a display driven by the conventional line-by-line addressing technique is

$$V_{\text{rms conventional}} = \sqrt{\frac{V_r^2 \pm 2V_rV_c + NV_y^2}{N}}. \tag{19}$$

It is similar to (18) except for the first term. We can show that the maximum amplitude of the step voltage profiles are related to that of the conventional line-by-line addressing, as shown in (20) and (21)

$$V_x = \sqrt{\left(\frac{3sT}{3s(T-T_0)-(4s+1)(s-1)T_s}\right)}\cdot V_r \tag{20}$$

$$V_y = \sqrt{\left(\frac{3sT}{3s(T-T_0)-(4s+1)(s-1)T_s}\right)}\cdot V_c. \tag{21}$$

The multiplying factor is the same for both row and column waveforms and is similar to that in (11) of Section V. The number of transitions across the pixels is independent of the image when the duty-cycle control is introduced with a finite T_0. Here, the power consumption depends just on the number of ON and OFF pixels in the image because the capacitances of the ON and OFF pixels are not equal. It does not depend on the number of polarity inversions or the data sequences involved in forming the image. Expressions for the power consumed by ON and OFF pixels are given in (22) and (23), respectively

$$P_{\text{ON pixel}} = \frac{sC_{\text{ON}}}{NT}\left[\left(\frac{V_x+V_y}{s}\right)^2 + (N-1)\left(\frac{V_y}{s}\right)^2\right] \tag{22}$$

$$P_{\text{OFF pixel}} = \frac{sC_{\text{OFF}}}{NT}\left[\left(\frac{V_x-V_y}{s}\right)^2 + (N-1)\left(\frac{V_y}{s}\right)^2\right]. \tag{23}$$

The power consumption of the display is given in (24). Here, x_j is the number of ON pixels in the display with N rows and M columns

$$P = x_j P_{\text{ON pixel}} + (N \cdot M - x_j)P_{\text{OFF pixel}}. \tag{24}$$

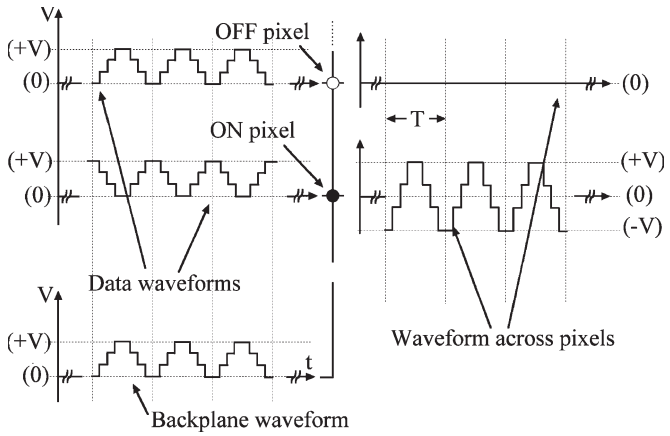

Fig. 8. Typical waveforms when multisteps are introduced in static drive.

The ratio of the power consumption of multistep line-by-line addressing to that of the conventional line-by-line addressing with duty-cycle control is given by

$$\frac{P_{\text{multi-step}}}{P_{\text{pulse}}} = \left(\frac{3(T - T_0)}{3s(T - T_0) - (4s + 1)(s - 1)T_s} \right). \quad (25)$$

This factor is the same as that in (14), and, hence, a comparison of the power consumption shown in Fig. 6 holds good for the line-by-line addressing with the multistep voltage profile.

VII. Static Drive With Multistep Waveforms

A nonmultiplexed display can be treated as a special case of a matrix display having just one row $(N = 1)$. Typical multistep waveforms for a nonmultiplexed display are shown in Fig. 8.

VIII. Hardware Implementation

A typical LCD driver for the line-by-line addressing consists of:

1) shift register with m stages and provision to shift the data serially in to the driver;
2) set of m latches to enable parallel transfer of data from the shift register; and
3) set of m 2:1 analog multiplexers that can select one of the two voltages in an internal bus to the m outputs.

Multiplexers in LCD drivers like HD-44100 are realized using CMOS switches. Hence, any voltage that is within the supply voltage of the driver IC can be applied to the electrodes of the display. Although the multistep waveform profile proposed in this paper has a large number of voltage levels, the same set of drivers can be used to apply the multistep waveform profile because just four voltages (select and nonselect voltages in the scanning and data waveforms) are necessary at a given instant of time.

A. Voltage Level Generator (VLG)

The VLG of the conventional line-by-line addressing is modified, as shown in Fig. 9. The conventional VLG ensures dc-free voltages across the pixels with a minimum supply voltage. Voltages V_1 and V_6 are the positive and negative select voltages,

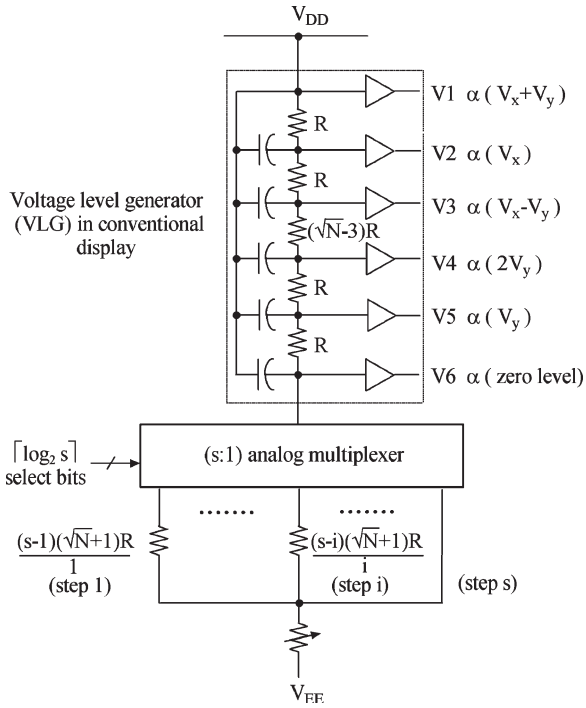

Fig. 9. VLG that generates the six voltages that are inputs to the conventional LCD drivers. The resistor network with buffers (enclosed in a box) is the VLG for the conventional line-by-line addressing. The amplitude of the voltages $(V1$ to $V6)$ is varied by selecting the series resistance (R_s) using an analog multiplexer $(s : 1)$. The value of the series resistance depends on the step size, and one of the resistors from the bank of s resistors is connected to the conventional VLG at a given instant of time using the multiplexer. ON resistance of the analog multiplexer is assumed to be small as compared to the other resistors in the network.

respectively, in the scanning waveforms. They are also the data voltages for the ON pixels during the negative and positive polarities, respectively. Voltages V_5 and V_2 are the nonselect voltages in the scanning waveforms during the positive and negative polarities of a cycle to ensure a dc-free operation. The voltages V_3 and V_4 are the data voltages for the OFF pixels during the negative and positive polarity selection of the address lines. The voltages applied to the LCD can be varied as dictated by the multistep waveform profile with a variable resistor R_s

$$R_s = \frac{(s - i) \cdot \left(\sqrt{N} + 1\right) \cdot R}{i} - R_{\text{ON}}; \qquad i = 1 \text{ to } s. \quad (26)$$

Here, R_{ON} is the ON resistance of the analog multiplexer. The variable resistance (R_s) can be implemented by using an analog multiplexer $(s : 1)$ and s resistors corresponding to the steps in the waveform profile. The ON resistance of the multiplexer has to be accounted for in the practical implementation of the circuit. The VLG in LCDs have capacitors and voltage followers to stabilize the voltages V_1 to V_6. These voltages need some settling time whenever the resistor R_s is varied. Two resistor networks (as shown in Fig. 10) may be used along with six (2:1) analog multiplexers to overcome this problem. One of the resistor networks is connected to the drivers (through the six multiplexers) alternately, while the series resistance in the other network is switched so that the voltages corresponding to the next time interval will have a sufficient time to stabilize.

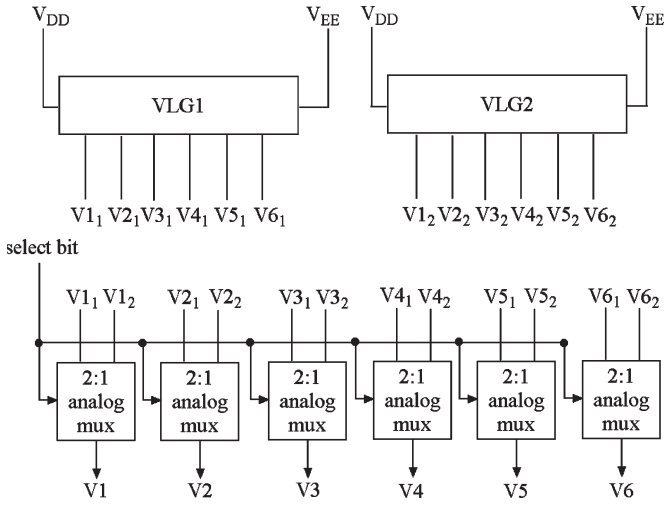

Fig. 10. Schematic diagram illustrating the use of two VLGs to allow the voltages to settle when the resistor R_s is switched (in one of them alternately) using the analog multiplexer that is shown in Fig. 9.

B. Effect of the Increase in Time Intervals in Drive Waveforms

Select time in the scanning waveforms is decided by the frame frequency (f) and the number of lines that are multiplexed (N). It is preferable to have the same select time $[T = 1/(f \cdot N)]$ even when the multistep profile is used because the frame frequency is chosen to be sufficiently large to avoid flicker in the display. Hence, introduction of multistep profile decreases the smallest time interval in the addressing waveforms by a factor (T/T_s) as compared to the single step in the conventional addressing techniques. Ideally, this decrease in time interval should not affect the performance of the display because the LCDs are slow-responding devices, and their electrooptic response depends just on the rms voltage, and it is independent of the shape of the waveform across the pixels. However, the RC time constant (due to the ON resistance of CMOS switches in the driver ICs and the capacitance of the pixels) will become comparable to the smallest time interval (T_s) when one or more of the following conditions are encountered.

1) The number of steps (s) in the waveform profile is large.
2) The flat region (T_f) is comparable to the select time (T).
3) The number of lines multiplexed (N) is large.
4) The size (and hence the capacitance) of the pixels is large.
5) The ON resistance of the CMOS switches in the drivers is large.

The analysis presented in this paper holds good as long as the RC time constant is less than about 20% of T_s. We are planning to bring out a detailed analysis that will include the effect of time constant on the power consumption. The RC time constant limits the number of steps (s) in the multistep waveforms, and it is important to note that a good reduction in the power consumption can be achieved even with a few steps. The increase in the supply voltage can be minimized by increasing the flat region (T_f) in the waveforms. Here, again, a lower RC time constant is preferable to achieve a lower supply voltage.

IX. Conclusion

The fundamental nature of the idea of substituting pulses with multistep voltage profiles to reduce the power consumption ensures that it will hold good in combination with any other addressing technique suitable for driving the rms responding matrix LCDs. The scaling of the amplitude of the row and column waveforms and the reduction in the power consumption, etc., will be the same as the result of the analysis presented in Section V. We have also shown that the addressing technique with multistep waveforms can be implemented with the standard drivers and some simple circuit that is common to all the drivers in the display. Hence, the hardware complexity of the drive electronics does not increase significantly with the introduction of multistep waveform profile in the addressing techniques. The multistep voltage profile reduces to a triangular waveform when $s \to \infty$. The application of such triangular waveforms to drive the matrix display is outside the scope of this paper, and it will be presented elsewhere.

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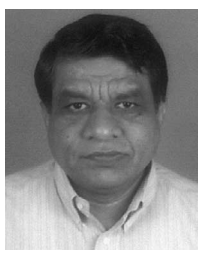

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