Binary Addressing Technique With Duty Cycle Control for LCDs

T. N. Ruckmongathan, M. Govind, S. V. Ashoka, and G. Deepak

***Abstract*—Introduction of duty cycle in the binary addressing technique is proposed to enable integration of liquid crystal display drivers with a digital system in a single chip. An analysis of this technique with duty-cycle control is presented. Effects of duty-cycle control on brightness uniformity of pixels in the liquid crystal display are discussed. A system on chip implementation of the technique is also demonstrated.**

***Index Terms*—Displays, duty-cycle control, liquid crystal display (LCD), matrix addressing and multiplexing.**

I. Introduction

THE CURRENT trend in system design is to integrate the whole system onto a single chip. This approach is popularly known as system on chip (SoC). Display plays an important role in the man machine communication and hence it is a popular output device. It is preferable that display drivers are also integrated along with the digital system in the same chip. Drivers of most flat-panel displays are not integrated onto SoC because either high voltages or high currents are necessary to drive the displays. Liquid crystal displays (LCDs) are low-voltage devices and they consume very little power. Hence, it appears that LCD drivers are well suited for SoC. In fact, some processors have LCD drivers incorporated in them. While integrating drivers of nonmultiplexed displays (displays with static drive) is straight forward, some problems are encountered in the case of drivers for multiplexed displays. Scanning (row) and data (column) waveforms have multiple voltage levels in almost all the addressing techniques employed for driving LCDs. This is in contrast to just two voltage levels in a digital system. For example, the most popular line-by-line addressing technique [1] has four voltage levels in scanning as well as the data waveforms. Conventional line-by-line addressing technique [2] and the multiline addressing techniques like the Improved Hybrid Addressing Technique [3] and Sequency Addressing Technique [4] have three voltage levels in the scanning waveforms and two or more voltage levels in the data waveforms. The Active Addressing Technique [5] has two voltage levels in the row waveforms but a large number of voltages in the column waveforms. Supply voltage of the display drivers also increases with the number of lines multiplexed (N) in the display. Hence, it is not easy to integrate drive electronics and digital system in a single chip. The binary addressing technique (BAT) [6], [7] is an exception. It has just two voltage levels in the scanning as well as the data waveforms. Hence, BAT is compatible with the digital logic circuits. BAT has the lowest power supply voltage as compared to any other addressing technique. Supply voltage of the BAT decreases with increase in the number of lines multiplexed. These advantages come at the cost of a lower selection ratio and a limit on the number of lines that can be multiplexed. However, this not a serious problem when N is small as in alphanumeric and low-resolution graphic displays. Good contrast can be achieved by using liquid crystal mixtures with steep electroopoptic characteristics. Electrooptic threshold voltage $(V_{\mathrm{Threshold}})$ of the liquid crystal mixture and N determine the supply voltage of the display drivers. However, other factors have to be considered while deciding the supply voltage of the system. The technology employed for fabricating the integrated circuit, types of signals to be interfaced with it, etc. will have to be taken into account. Supply voltage of the drive electronics is usually not the same as that of the digital system. It is of course preferable to have just one power supply for both. Binary addressing technique with duty-cycle control is proposed in this paper to achieve a single supply operation of the system. The binary addressing technique is reviewed briefly in the next subsection.

A. BAT

The N lines (rows) in a matrix display are selected with voltages corresponding to an N bit binary word called select pattern $(R_1, R_2 \ldots R_{N-1}, R_N)$. Here, R_j is either logic "0" or "1." The voltage applied to the rows is 0 for logic "0" and V for logic "1." Data to be displayed in a column $(D_1, D_2 \ldots D_{N-1}, D_N)$ is compared with the select pattern bit-by-bit using exclusive-OR gates. Number of mismatches i between these two patterns is determined by counting the number of logic "1" in the output of the exclusive OR gates i.e., $i = \sum_{j=1}^{N} R_j \oplus D_j$. Data voltage applied to the columns (data electrodes) is 0 if i is less than $N/2$. Then the instantaneous voltages across pixels in that column correspond to the select pattern. Hence, voltages across i pixels will not correspond to the desired state, since the number of mismatches is i. In case, the number of mismatches is greater than $(N/2)$ then data voltage is chosen to be V. Instantaneous voltages across the pixels will then correspond to complement of the select pattern. Choice of V as data voltage results in $(N - i)$ errors across the pixels in that column. The number of errors is less as compared to selecting 0 as the data voltage. The condition

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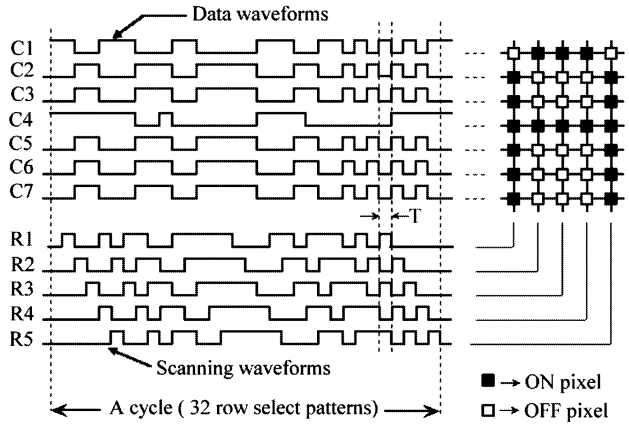

Fig. 1. Typical addressing waveforms of BAT.

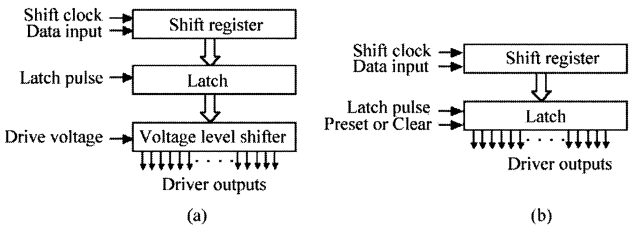

Fig. 2. Schematic of the LCD drivers for (a) static drive for nonmultiplexed displays and (b) BAT with duty-cycle control for multiplexed displays.

$i = (N/2)$ is avoided by choosing N to be odd. Similarly, data voltages for all the columns in the matrix display are determined using this majority decision. Voltages corresponding to the select pattern and the data are applied simultaneously to the matrix display for a time duration T. A refresh cycle is complete when all the 2^N binary words are used as select pattern once and the corresponding scan and data voltages are applied to the matrix display. The display is refreshed continuously by repeating this cycle. Time duration $(2^N \cdot T)$ should be small as compared to the response times, in order to ensure the root mean square (RMS) behavior and avoid flicker in the display. An N-bit binary counter can be used to generate all the 2^N select patterns. Outputs of the counter are square waveforms with ratio of their frequencies in powers of two. They correspond to the Rademacher functions [8]. The output sequences are orthogonal when $+1$ is assigned to logic 0 and -1 is assigned to logic 1. Scanning and data waveforms of the BAT are shown in Fig. 1. These waveforms have just two voltage levels. Thus, standard CMOS gates can be used as drivers provided the amplitude (V) of the drive waveforms can be controlled depending on the threshold voltage of liquid crystal mixture. Duty cycle control in BAT and its advantages are described next.

II. Duty-Cycle Control

A block diagram of a typical LCD driver for nonmultiplexed displays is shown Fig. 2(a). This driver could also be used for the binary addressing technique. Data is shifted into the shift register serially and is latched in parallel after shifting the data corresponding to all the pixels. These drivers have a dedicated voltage level shifter at each output, so that displays with different threshold voltages can be driven by varying the drive voltage. Voltages corresponding to outputs of the latch are applied to the display during the entire select time. The drive voltage is usually independent of the supply voltage to the shift register and latches. Drive voltage is varied, either by using a potentiometer or by using a separate supply voltage. We have introduced duty-cycle control in the waveforms of BAT. Instead of applying the select and data voltages during the entire duration of a select time (T), they are applied only during a fraction of the select time (T_a). Select and data voltages are assigned the same voltage (either 0 or V) during rest of the select time (T_{na}) as illustrated in Fig. 3. Duty cycle (T_a/T) is selected such that the RMS voltage across OFF pixels is near $V_{\text{threshold}}$. Thus, control of duty cycle in binary addressing technique paves way to a single supply operation with flexibility to vary the RMS voltage across the pixels over a range. A latch with an asynchronous preset or clear input eliminates the voltage level shifter in the driver of Fig. 2(a). An asynchronous clear drives all the latch outputs to 0 V during the nonselect period T_{na}. Similarly, all the outputs can be driven to a voltage V during T_{na} with an asynchronous preset to the latch instead of a clear. Presetting or clearing the outputs of scanning and data drivers during the select time, ensures that the voltage across all pixels in the display is 0 during the rest of the select time. Schematic of a driver for BAT with duty-cycle control is shown in Fig. 2(b). The driver circuit is digital after the elimination of the level shifters. Hence, it can be integrated easily into a system on chip (SoC). Duty cycle control has an added advantage of improving brightness uniformity of pixels in the display as discussed in the Section IV.

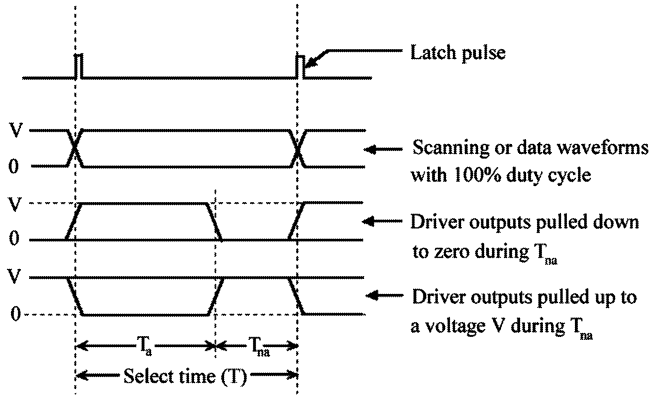

Fig. 3. Duty cycle control in the LCD drivers.

III. Analysis of BAT With Duty Cycle Control

Consider a matrix display with N scanning electrodes and an arbitrary number of data electrodes. A voltage V across a pixel is favorable to an ON pixel and unfavorable to an OFF pixel. Similarly, 0 voltage across a pixel is favorable to an OFF pixel and unfavorable to an ON pixel. The number of

times a pixel gets an unfavorable voltage during a cycle (E) is given by

$$E = 2B = 2\sum_{i=0}^{(N-1)/2} \frac{i\,(N-1)!}{i!(N-i)!}. \tag{1}$$

The number of times a pixel gets a voltage that is favorable to its state during a cycle is given by

$$F = (2^N - 2B) = 2\sum_{i=0}^{(N-1)/2} \frac{(N-1)!}{i!(N-1-i)!}. \tag{2}$$

These equations have been derived in [6]. The expression for the RMS voltage across ON pixels when a display is scanned by BAT with duty-cycle control is

$$V_{\mathrm{ON}}(\mathrm{RMS}) = V\sqrt{\frac{T_a F}{T 2^N}} = V\sqrt{\frac{T_a}{T}\left(\frac{2^{N-1}-B}{2^{N-1}}\right)}. \tag{3}$$

Similarly, a 0 voltage across an OFF pixel is favorable to its state while a voltage V is unfavorable. Thus, the expression for RMS voltage across an OFF pixel is

$$V_{\mathrm{OFF}}(\mathrm{RMS}) = V\sqrt{\frac{T_a E}{T 2^N}} = V\sqrt{\frac{T_a}{T}\left(\frac{B}{2^{N-1}}\right)}. \tag{4}$$

The selection ratio of an addressing technique is defined as the ratio of the RMS voltage across an ON pixel to that across an OFF pixel. The selection ratio is a maximum for BAT when the select and data waveforms have the same amplitude. The expression for selection ratio of BAT is

$$\text{Selection Ratio} = \sqrt{\frac{F}{E}} = \sqrt{\frac{2^N - 2B}{2B}} = \sqrt{\frac{2^{N-1}-B}{B}}. \tag{5}$$

Selection ratio is not affected by the introduction of duty cycle since the RMS voltages across both the ON and OFF pixels are reduced by same factor. Hence, the duty-cycle control acts like a digital potentiometer to change the voltages across the pixels to match the electroopoptic characteristics of the display. Fig. 4 shows RMS voltage (normalized to the supply voltage) versus duty cycle for the ON and OFF pixels. The duty cycle is determined by equating the $V_{\mathrm{OFF}}(\mathrm{RMS})$ to $V_{\mathrm{Threshold}}$

$$\text{Duty cycle} = \frac{T_a}{T} = \left(\frac{V_{\mathrm{threshold}}}{V}\right)^2 \left(\frac{2^{N-1}}{B}\right). \tag{6}$$

Table I gives the duty cycle necessary to achieve the desired RMS voltage across a pixel for typical supply voltages and multiplexing conditions, when the threshold voltage of the liquid crystal mixture is 1 V. Considering the fact that the duty cycle is usually greater than 0.1, the RMS voltage across the pixels can

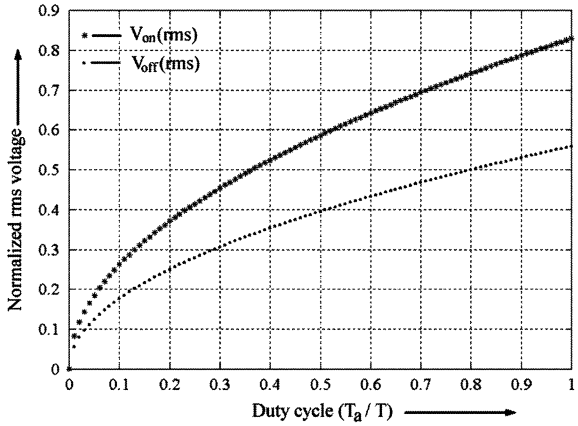

Fig. 4. Plot of the RMS voltage across pixels versus duty cycle.

TABLE I
DUTY CYCLE WHEN THE THRESHOLD VOLTAGE IS 1 V

Number of lines multiplexed (N)	DUTY CYCLE	
	Supply voltage =3.3V	Supply voltage= 5.0V
3	0.3673	0.1600
5	0.2938	0.1280
7	0.2671	0.1164
9	0.2528	0.1101
11	0.2436	0.1061

be controlled to an accuracy of 1% by using an eight bit counter. Since the electroopoptic response is nonlinear, it is important that the RMS voltage across the pixel is controlled in the active region i.e., $V_{\mathrm{Threshold}}$ to $V_{\mathrm{Saturation}}$. Ten bits are adequate to control the light transmission with an accuracy of at least 1%, if the ratio $(\gamma = (V_{\mathrm{saturation}})/(V_{\mathrm{Threshold}}))$, called the steepness parameter is equal to 1.286 (selection ratio of BAT when $N = 11$, a practical limit).

Power consumption of the drive circuit depends on the amplitude of voltage transitions as well as the number of occurrences of these transitions in the waveform across the pixels. Power consumption also depends on the state of the pixels since the capacitance of a pixel in the ON state (C_{ON}) could be twice that of a pixel in the OFF state (C_{OFF}). Power consumption of a display driven by BAT with duty-cycle control is

$$P = 2[\alpha_{\mathrm{OFF}} C_{\mathrm{OFF}} B + \alpha_{\mathrm{ON}} C_{\mathrm{ON}}(2^{N-1} - B)]V^2 f. \tag{7}$$

Here, α_{OFF} and α_{ON} are the number of pixels in OFF and ON states respectively, while f is the number of refresh cycles per second.

This analysis is valid under the assumption that the *RC* time constant (due to output resistance of the driver and capacitance of the pixels) is small as compared to the time T_a and the select time T. However, the pulse width (T_a) may be comparable to the *RC* time constant, when the threshold voltage of the display

is low. Brightness uniformity of the pixels will not suffer since all the waveforms are distorted. The RMS voltages across ON and OFF pixels after considering the *RC* effect is

$$V_{\mathrm{ON}}(\mathrm{RMS}) = V\sqrt{\frac{\beta_{\mathrm{ON}}(2^{N-1}-B)}{T2^{N-1}}} \tag{8}$$

$$V_{\mathrm{OFF}}(\mathrm{RMS}) = V\sqrt{\frac{\beta_{\mathrm{OFF}}B}{T2^{N-1}}} \tag{9}$$

Here, the expression for β_x (x is either ON or OFF) is

$$\beta_x = T_a - RC_x\left(1-e^{\frac{-T_a}{RC_x}}\right) - \frac{RC_x}{2}\left(1-e^{\frac{-T_a}{RC_x}}\right)^2 e^{\frac{-2(T-T_a)}{RC_x}}. \tag{10}$$

These expressions for the RMS voltage across a pixel are valid only when the voltage across the pixel is completely discharged within the select time T. However, the expressions (8) and (9) for RMS voltage are better approximations than (3) and (4), respectively. Power consumption in a display after considering the *RC* effects is

$$P = 2[\alpha_{\mathrm{ON}}C_{\mathrm{ON}}\delta_{\mathrm{ON}}(2^{N-1}-B) + \alpha_{\mathrm{OFF}}C_{\mathrm{OFF}}\delta_{\mathrm{OFF}}B]V^2 f. \tag{11}$$

Here, δ_x (x is either ON or OFF) is given by

$$\delta_x = \frac{1}{2}\left[2\left(1-e^{\frac{-T_a}{RC_x}}\right) - \left(1-e^{\frac{-T_a}{RC_x}}\right)^2 e^{\frac{-2(T-T_a)}{RC_x}}\right]. \tag{12}$$

IV. Brightness Uniformity

Theoretically, the RMS voltage across pixels in BAT is independent of the sequence in which the 2^N select patterns are applied while scanning the display. However, the addressing waveforms are distorted due to the output resistance of the display drivers, the resistance of the indium tin oxide electrodes and the capacitance of the pixels. Distortions in the waveforms reduce RMS voltage across the pixels. Scanning waveforms based on Rademacher functions (R1–R5), a data waveform (C1) and the waveforms across pixels (Ri–C1) in a column are shown in Fig. 5. It can be seen that the number of transitions across pixels is different even when the pixels are driven to the same state. This results as in poor brightness uniformity of pixels. The number of transitions in the scanning waveforms differs by a large factor since the frequencies of Rademacher functions vary by a large factor as their ratios are in powers of two.

The output resistance of the display driver may be decreased; by increasing the size of transistors used as switches to improve the brightness uniformity of pixels. However, this will lead to an increase in the size of the integrated circuit since the number of outputs in a driver IC is large. An alternate approach is to ensure

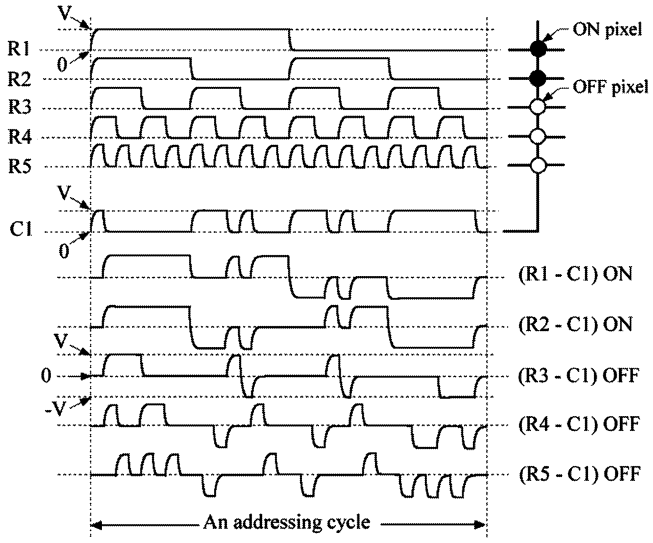

Fig. 5. Distorted waveforms when scanning is based on the Rademacher functions.

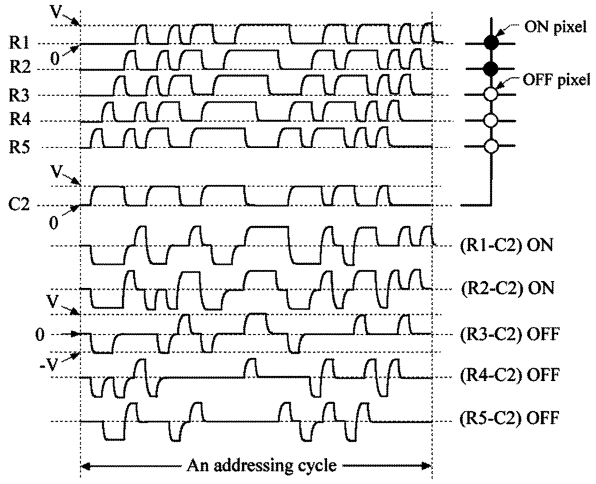

Fig. 6. Distorted waveforms when scanning is based on the modified PRBS sequences.

that the number of transitions is the same across all the pixels in a display. Here, the reduction in RMS voltage across the pixels driven to the same state will be equal. Hence, the brightness uniformity of the display will be good.

The pseudo-random binary sequence (PRBS) and its shifted versions have the same number of transitions. An all 0 state has to be added to this PRBS generator with $(2^N - 1)$ states, so that all the 2^N select patterns may be used to scan the display. Here N is the number of stages in the shift register. The number of transitions in the scanning waveform based on this modified PRBS generator is the same as shown in Fig. 6. Brightness uniformity will be better as compared to using scanning waveforms based on Rademacher functions. However, the variations in number of transitions depending on the data displayed in a column will contribute to some brightness nonuniformity. Duty cycle control introduces equal number of transitions in both scanning and data waveforms.

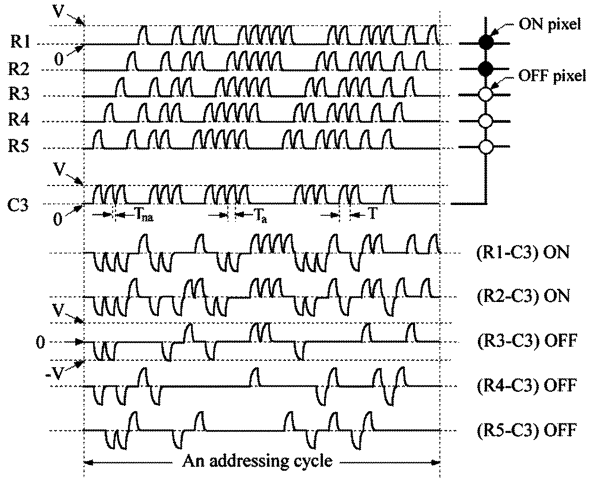

Fig. 7. Distorted waveforms when duty-cycle control is introduced in BAT and the scanning waveforms are based on modified PRBS sequences.

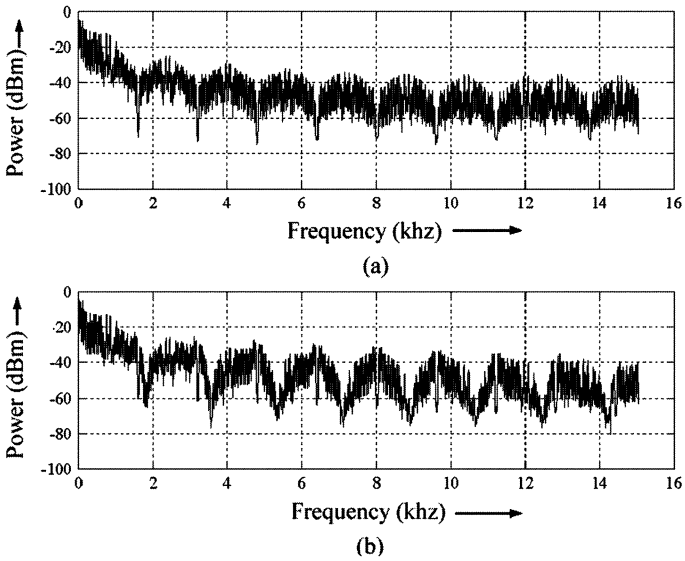

Fig. 8. Typical frequency spectrum across a pixel. (a) Without duty-cycle control and (b) with 90% duty cycle, when scanning waveforms are based on modified PRBS sequences.

Hence, the number of transitions across the pixels will be independent of the data to be displayed in a column and it just depends on the state of the pixel, as shown in Fig. 7. Hence, the displays driven using BAT with duty-cycle control will have good brightness uniformity of pixels. Spectra of the scanning waveforms are almost similar when modified PRBS is used. Hence, a sequence generator based on PRBS is preferred even after the introduction of duty-cycle control to achieve a good brightness uniformity of pixels. Introduction of duty-cycle control itself does not alter the frequency spectrum significantly as evident from Fig. 8.

V. Hardware Implementation

A block diagram of the display system addressed using BAT is shown in Fig. 9. The 2^N select patterns are generated using a modified PRBS Generator (PRBSG) [9]. The feedback F in the PRBSG to obtain all the 2^N states is given by: $F = (R_5 \oplus R_3) \oplus (\overline{R_4} \cdot \overline{R_3} \cdot \overline{R_2} \cdot \overline{R_1})$, when $N = 5$. Here, the symbol $\oplus$ represents an exclusive OR operation. The term $(R_5 \oplus R_3)$ is the feedback in a standard PRBS generator having $(2^N - 1)$ states. The logic circuit used for the implementation of PRBSG is shown in Fig. 10.

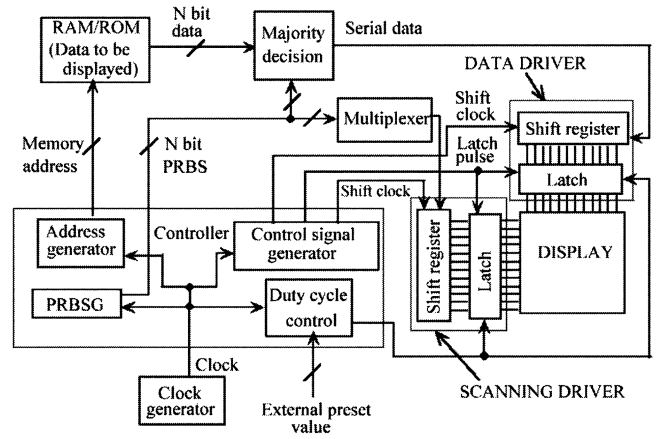

Fig. 9. Block diagram of a display system driven by BAT with duty-cycle control.

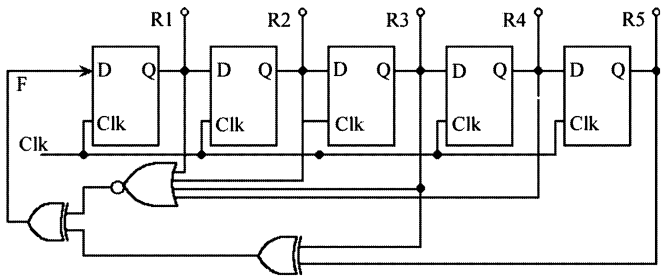

Fig. 10. Logic circuit of modified PRBS generator.

Photographs of two displays driven by BAT with duty-cycle control are shown in Figs. 11 and 12 respectively. An eight-character alphanumeric display using 7×5 dot matrix font is shown in Fig. 11. Alphanumeric characters stored in ASCII format are displayed in 7×5 dot matrix format using a complex programmable logic device (CPLD)-based controller. The character generator for displaying 96 alphanumeric characters and special symbols has been implemented as a lookup table and integrated into the controller. The controller has been implemented on a 5-V Altera CPLD using 168 logic cells. Scanning and data drivers have been implemented using standard CMOS integrated circuits.

Fig. 12 shows the photograph of an analog clock. The whole system including the drivers has been incorporated into a single CPLD to demonstrate the SoC approach. Outputs of the CPLD are directly connected to the LCD. The system has been implemented on a 3.3 V Xilinx CPLD using 181-logic cells.

VI. Conclusion

The duty-cycle control in the Binary Addressing Technique has paved way to SoC implementation without much constraint on the supply voltage or need for multiple voltages. Introduction of duty cycle has also resulted in improved brightness uniformity of the pixels. The effect of *RC* time constant on the ad-

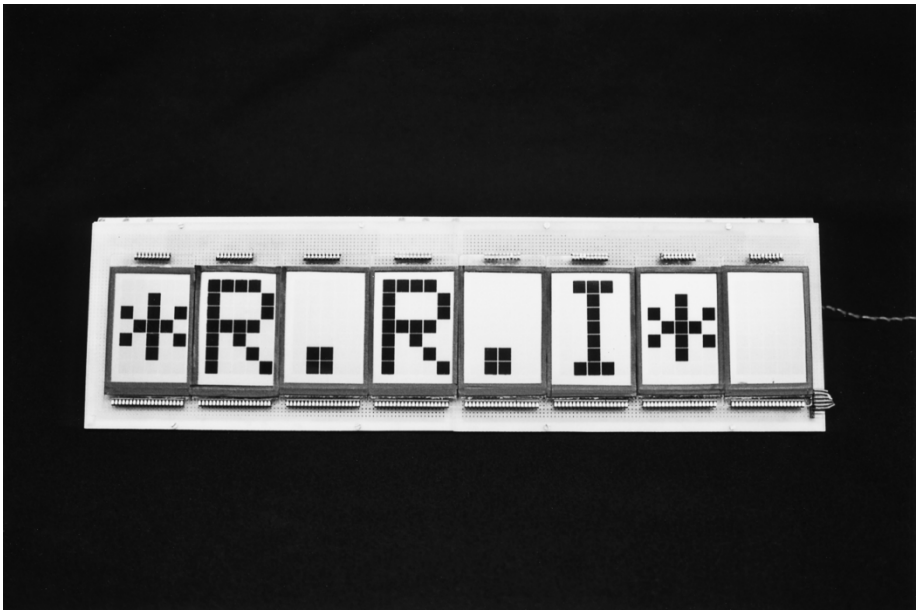

Fig. 11. Photograph of an alphanumeric display driven by BAT with duty-cycle control.

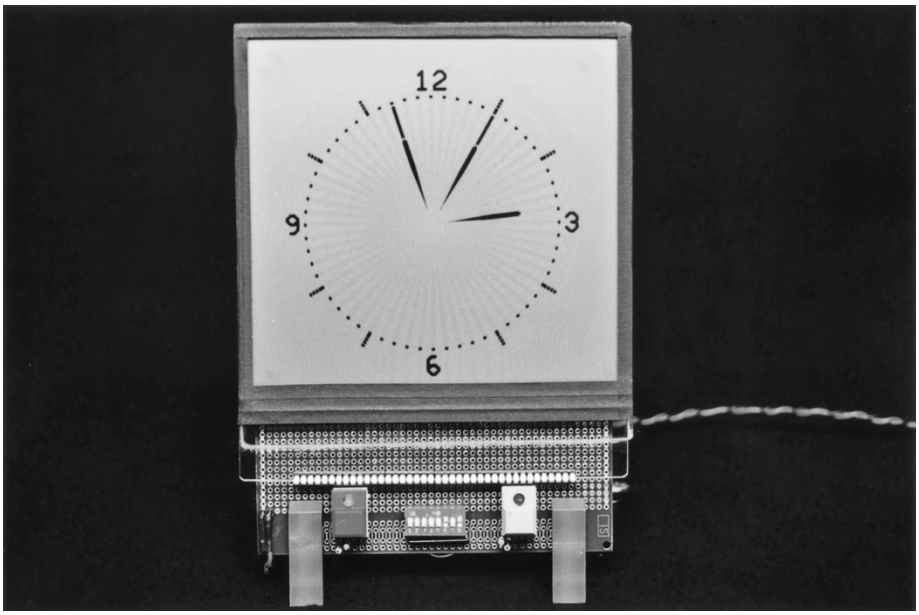

Fig. 12. Photograph of a prototype demonstrating a SOC implementation.

dressing waveforms has been analyzed and an SoC implementation of the technique has been demonstrated.

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