Liquid Crystal Display for an Automobile Dashboard

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ABSTRACT

Dashboard is an information cluster located at the edge of the driver's primary field of view. Although most of the cars have mechanical dashboards, electronic implementation of the same will have enough flexibility to cater to varying customers' choice. Liquid crystal displays are a good choice for electronic dashboards since the format of the display can be modified easily using a different set of masks. We have also integrated the drive electronics into a low cost programmable integrated circuit. Hence, the varying needs (of products or customers) can easily be accommodated in a short duration of time with low tooling cost. Design and development of a liquid crystal display for car dashboard is presented.

Keywords: Dashboard, LCDs, Binary addressing technique, CPLD, SoC

1. INTRODUCTION

Dashboard is an information cluster located at the edge of the driver's primary field of view[1]. It provides the current state of some important parameters like speed, engine rpm, distance travelled, engine coolant temperature etc. to the driver. Although most of the cars use mechanical dashboards, electronic implementation of the same will have enough flexibility to cater to varying customers' choice without too much additional cost. Liquid Crystal Displays (LCDs) are a good choice for the electronic dashboards as they operate at low voltages, consume very little power and are also economical. In fact high-end cars have LCD panels in their dashboards[1]. A different set of masks could be used during photolithographic process to change the format and appearance of the display. The major drawbacks of LCDs are narrow viewing angle and slow response at low temperatures. A wide viewing angle can be achieved when the number of lines multiplexed is small. A heater can be incorporated on the display cell (by using ITO electrodes) to surmount the slow response at low temperatures. The backlight in the dashboard could also be used to heat the display cell in subzero temperatures. It is preferable that the cost of the drive electronics (drivers as well as the controller) is low. This is achieved by using Binary Addressing Technique[2] (BAT). It has simple addressing waveforms with just two voltage levels and needs a lower supply voltage as compared to any other techniques for driving matrix LCDs. We have implemented the drivers as well as the controller for the dashboard display using Complex Programmable Logic Device (CPLD) having two hundred and eighty-eight logic cells. The CPLD can be reconfigured for a new design by reprogramming it with appropriate code. Design and format of the display can also be changed easily. Hence the design of a new dashboard display can be achieved in a short duration without high tooling cost.

2. A LIQUID CRYSTAL DISPLAY FOR THE DASHBOARD

Liquid crystal display is fabricated by sandwiching liquid crystal mixture between two glass plates with electrode patterns. Indium Tin Oxide (ITO), a transparent conductor is coated on the glass plate to form the electrode patterns. Liquid crystal displays are classified as active matrix or passive matrix. Active matrix liquid crystal displays (TFT based displays) have a complex manufacturing process and are expensive. They are well suited to display images. Passive matrix liquid crystal displays are easy to manufacture and are economical. We have used the passive matrix liquid crystal display for the automobile dashboard. Static drive[3] could be employed to achieve high contrast and wide viewing angle in passive matrix LCDs. However, the number of connections to the display from the drivers is usually high as compared to that of multiplexed displays. Hence static drive is not preferred if the dashboard has to be driven using an integrated circuit. The contrast and viewing angle of passive matrix LCDs decrease as we increase the number of lines to be multiplexed. A performance very close to that of static drive can be achieved in the multiplexed displays by a proper choice of the electro-optic effect, addressing (drive) technique and the matrix size.

2.1 Choice of the electro-optic effect

Twisted Nematic (TN) effect is the most popular of all the electro-optic effects using liquid crystal and is used in both active and passive matrix displays. Super Twisted Nematic (STN) effect has a slow response time of a few hundred milliseconds as compared to the TN effect with response time in the range of tens of milliseconds. Hence the STN effect is not preferred for the dashboard display even though it has steeper electro-optic characteristics.

2.2 Choice of the addressing technique

Looks of the mechanical gauges like speedometer, tachometer, etc. can be imitated by using pointer type displays with meandering electrode patterns[4]. Penz[5] has compared the various addressing techniques for driving pointer and bar graph type liquid crystal displays. These techniques achieve a high selection ratio (ratio of rms voltage across ON pixels to that of OFF pixels) by exploiting the restricted nature of bar graph and pointer displays. An infinite selection ratio (just as in case of the static drive) can be achieved in a pointer display by using the auto-correlation properties of the Pseudo Random Binary Sequences[6] (PRBS). All the pixels in a column except one can be driven to ON state (higher rms voltage) using this technique. It needs just two voltage levels in its drive waveforms and hence it is well suited for incorporating into an integrated circuit. Fukumoto design[7] also has two voltage levels in its drive waveforms. It achieves a selection ratio of $\sqrt{3}$ and this ratio is independent of the matrix size. The dashboard also has numeric displays like odometer apart from the pointer (or bar graph) type displays. Hence, both the techniques for displaying restricted patterns are not suitable for the automobile dashboard display. A multiplexing technique to display general patterns is necessary for the numeric displays. The binary addressing technique is the only technique that has just two voltage levels. It can be used to display general pattern as well as restricted patterns (as in pointer and bar graph displays). The binary addressing technique with duty cycle control[8] is well suited for the System-on-Chip (SoC) design. We have used binary addressing technique to drive the dashboard display and this technique is described briefly in Appendix I.

2.3 Choice of the matrix size

The selection ratio of the binary addressing technique against the number of lines multiplexed is shown in Table 1. The ratio $\left(V_{90}/V_{10}\right)$ is a measure of steepness of the electro-optic characteristic of the liquid crystal mixture. It ranges from 1.3 to 1.5 for a large number of mixtures. Here V_{90} is the voltage to be applied to achieve a 90% change in transmission in the display while V_{10} is a voltage necessary to achieve a 10% change in transmission. This ratio has to be less than or equal to the selection ratio to achieve a maximum contrast in the liquid crystal display. Hence, the number of lines multiplexed in the dashboard has to be less than or equal to nine rows as evident from the Table 1. It is preferable to multiplex five or ten lines in the pointer type displays while it is convenient to multiplex seven or five lines (7x5 or 5x3 fonts) in case of the numeric displays. The number of lines multiplexed has to be the same so that all the elements have the same contrast and viewing angle characteristics. We have chosen to multiplex five lines so that good contrast and wide viewing angle can be achieved. Details of the dashboard design are outlined in the next subsection.

Table 1: Selection ratio, supply voltage and duty cycle against number of lines multiplexing in BAT

Number of lines multiplexed	Selection ratio (S.R) $\frac{V_{ON}(rms)}{V_{OFF}(rms)}$	Supply voltage normalized to V_{th} $\frac{V_S}{V_{th}}$	Duty cycle for liquid crystals with V_{th}=1V	
			5V Supply	3.3V Supply
3	1.732	2.000	0.1600	0.3673
5	1.483	1.789	0.1280	0.2938
7	1.382	1.706	0.1164	0.2671
9	1.324	1.659	0.1101	0.2528
11	1.286	1.629	0.1061	0.2436

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2.4 Dashboard design

The liquid crystal display for the automobile dashboard has been designed to display speed, engine rpm, fuel level, coolant temperature, distance travelled and symbols like turn indicators, high beam etc. It has 210 pixels and the size of the display is 24.5 cm x 12.5 cm. All the segments, symbols, legends and pixels of the dashboard display are shown in Figure 1. Electrode patterns on the upper plate form the rows while the electrodes on the lower plate form the columns of a matrix. Intersections of electrode patterns on both these plates form the pixels. Electrode patterns on the upper and lower glass plates are shown in Figure 2 (a) and (b) respectively. Meandering electrode patterns have been used to

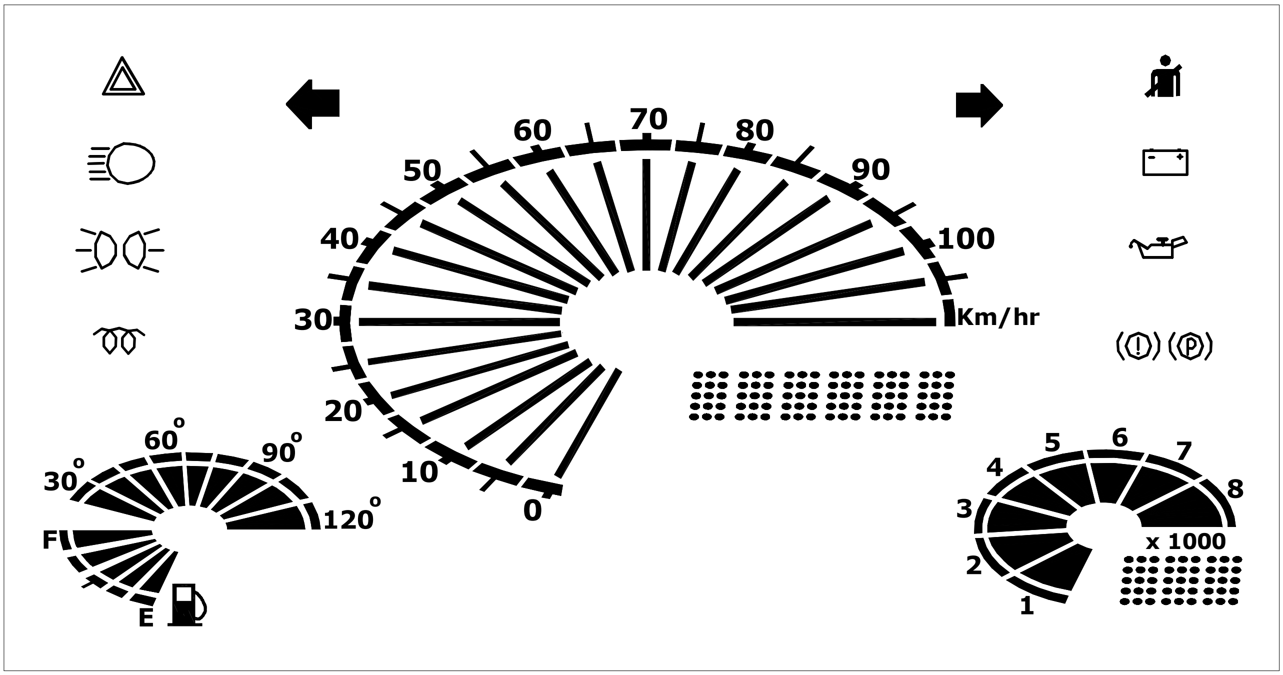
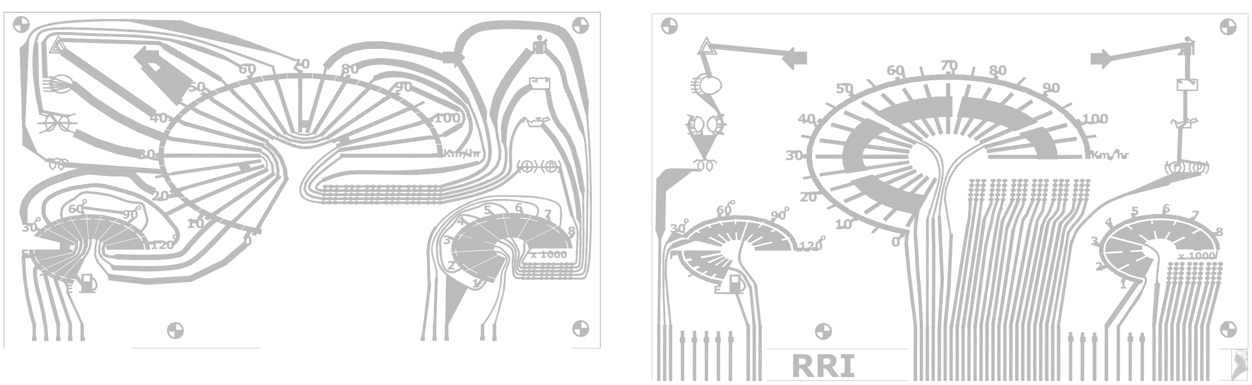


Figure 1: All the picture elements in the dashboard display.



(a) (b)

Figure 2: Electrode patterns on the (a) upper and (b) lower glass plates of the dashboard display.

achieve the looks of an analog instrument panel. The speedometer has twenty-three segments to display speed ranging from 0 to 110 kmph in steps of 5 kmph using a pointer and these segments are accommodated with in a five columns of a matrix with five rows. The tachometer, thermometer and fuel level indicator have been implemented using bar graphs. Tachometer has eight bars to display rpm up to eight thousand in steps of a thousand. Two columns are necessary to address these eight segments. The coolant temperature is also displayed using nine bars to cover the range 30ºC to 110ºC with a step size of 10ºC. Here again the segments are arranged with in two columns of the matrix with five rows. The five bars in the fuel level indicator are interconnected to form a single column. A 5x3 character font is used to display the numbers in the three-digit trip and six-digit odometers. Twenty-seven columns are necessary to drive these nine numeric digits. The ten symbols are interconnected to form two columns. The legends in the display are also interconnected to form four columns and they are always driven to ON state. They form a matrix of five rows and forty-three columns. Hence, there are forty-eight connections between the dashboard display and the drive electronics. Although the resolution and the range of the speedometer and tachometer are adequate, it could be increased by increasing the density of the electrode patterns. This would result in increase in the number of columns in the display. However, the increase will not affect the performance of the display. Design of a controller and drivers for the dashboard display and their implementation in to an integrated circuit are described in the next section.

3. HARDWARE IMPLEMENTATION

The driver and the controller for driving the dashboard display are incorporated into a complex programmable logic device using Finite State Machine (FSM) design. Block diagram of the controller is shown in Figure 3. We have assumed that the parameters have been sampled at suitable rate and digitized. The twenty-six bits input to the dashboard (CPLD) are connected to the seven different functional blocks, viz. speedometer, tachometer, fuel meter, thermometer,

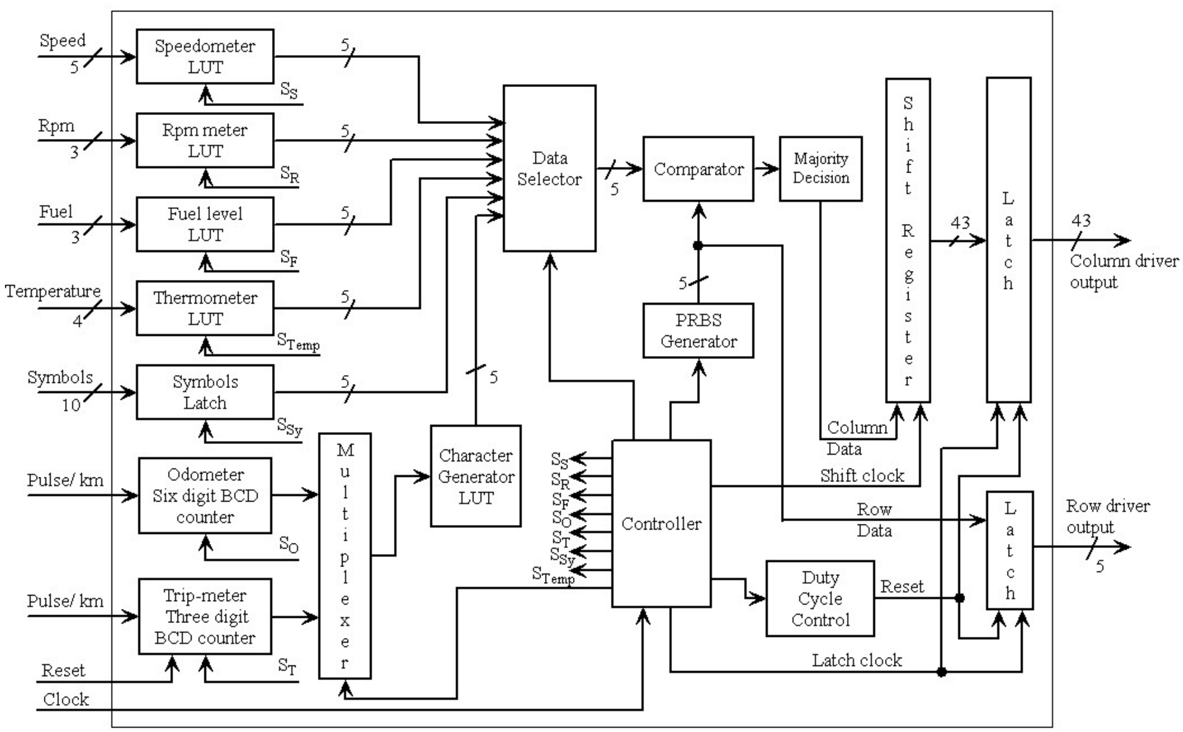


Figure 3: Block diagram of the drive electronics for the dashboard display.

symbols, odometer and trip meter. The input has five bits to represent the speed from 0 to 110 kmph. Three bits are used to input information to the bar graphs of fuel level indicator and tachometer. The temperature indicator needs four bits input. All the ten symbols are controlled individually using ten bits at the input. The odometer with six-digits as well as the trip-meter with three-digits have one bit input to provide a pulse for each kilometer covered. We have assumed that a pulse or multiple pulses are available for each kilometer (or a fraction of it) covered. A Look up Table (LUT) is used to select the pointer to be driven to the ON state for the five bits binary input. This is similar to a character generator for converting ASCII codes to the corresponding character font. Similarly the input binary numbers of the tachometer, thermometer and the fuel level indicator are code converted using LUTs to display them in the form of bar graphs. A character generator for the 5x3 numeric font has also been implemented using LUT. Nine BCD counters have been used to implement the odometer and the trip meter (six for odometer and three for trip meter). The output of these counters are fed serially to the character generator. The output of the character generator is connected to the data selector block. BAT is used for scanning the display and the controller selects a data corresponding to a column from one of the input

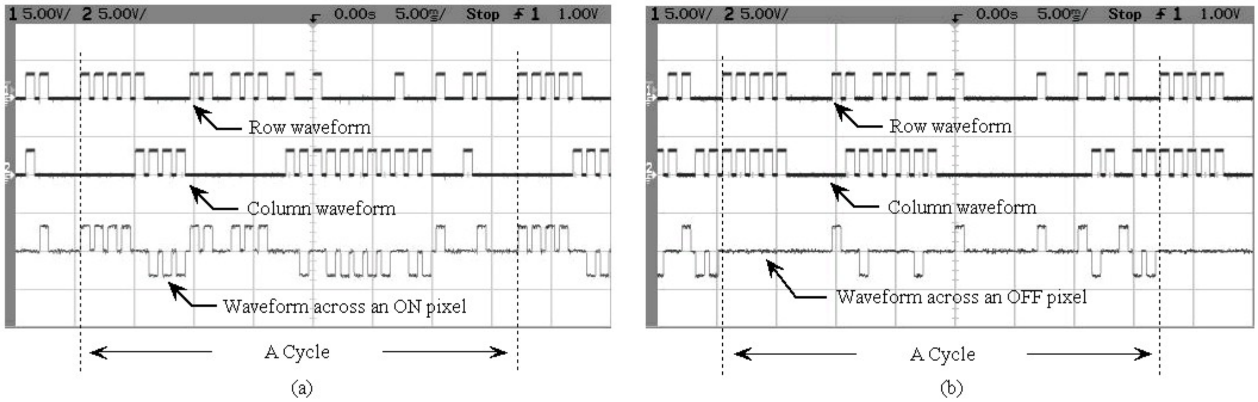


Figure 4: Typical waveforms across (a) ON and (b) OFF pixels.

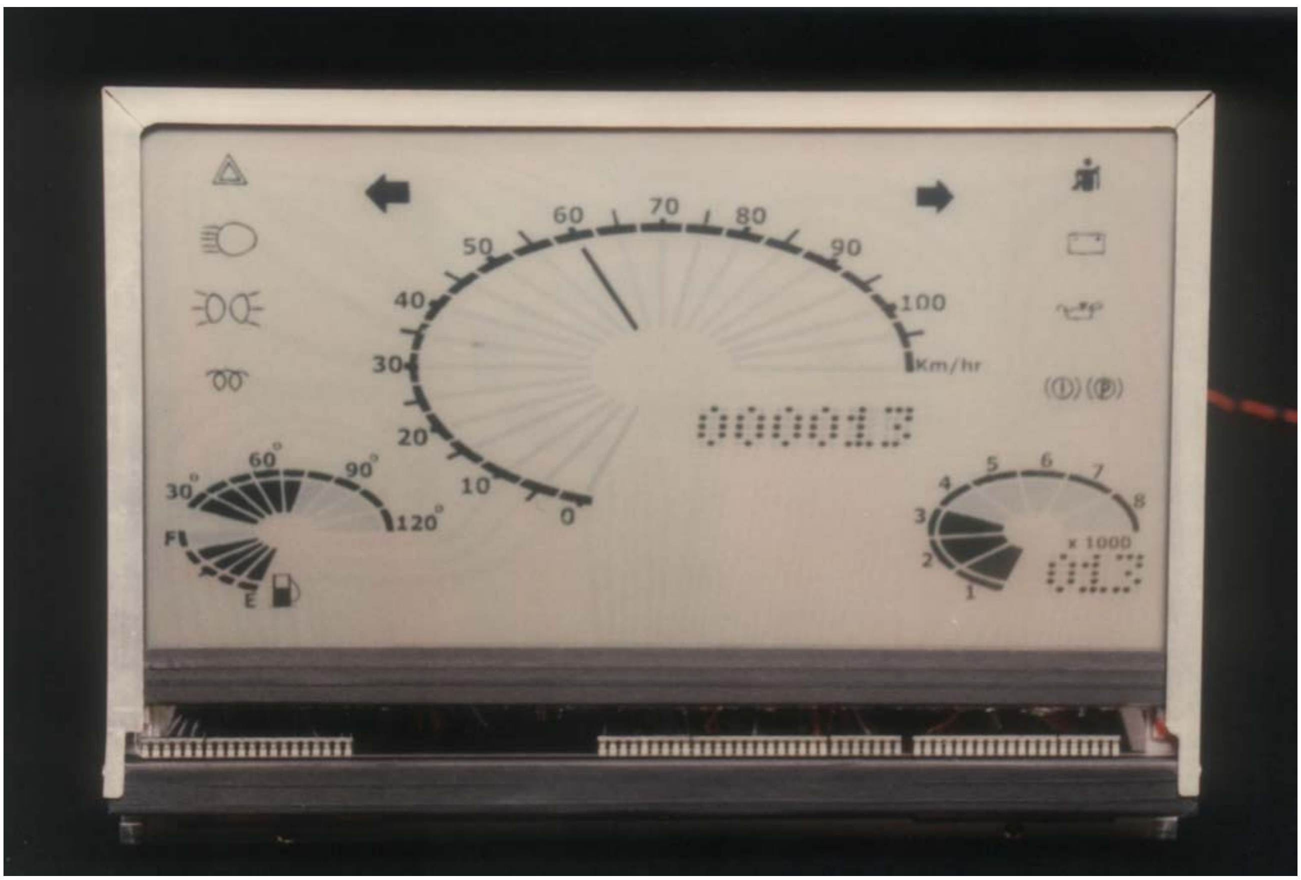


Figure 5: Photograph of the dashboard display.

blocks at a given time using a data selector. This selected output is compared with the select pattern of the PRBS generator bit-by-bit using exclusive-OR gates. A majority decision block generates the data to be shifted into the shift register. The controller generates a latch pulse when the data corresponding to all the forty-three columns have been shifted into the shift register. The latch pulse transfers the contents of the shift register as well as the PRBS generator into the latches. These latches serve as the drivers to the liquid crystal display. The output of the latches can be cleared using an asynchronous reset pulse generated by the controller. The output of the drivers remains low till a new select pattern (for the row drivers) and the corresponding data for all the columns are latched to the output. A cycle is complete when all the thirty-two (2^5) select patterns of the PRBS generator are used to scan the display. Duty cycle is controlled by the position of the reset pulse within the select time. The duty cycle is determined by the threshold of the liquid crystal mixture in the display and the supply voltage of the CPLD. The duty cycle for a display with a threshold of 1 volt is given in Table 1 when the supply voltage is either 3.3V or 5V. An eight-bit counter is used to control the duty cycle. The controller and the drivers have been implemented using two hundred and fifty-two logic cells. The display is refreshed at the rate of 25 Hz to avoid flicker.

4. RESULTS

An automobile dashboard using LCD has been demonstrated. The drive electronics for the display (dashboard) has been implemented using an inexpensive CPLD having two hundred and eighty-eight logic cells. Typical waveforms across ON and OFF pixels are shown in Figure 4 (a) and (b) respectively. Photograph of the prototype dashboard display is shown in Figure 5.

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APPENDIX I

Binary addressing technique

All the lines to be multiplexed are selected simultaneously in the binary addressing technique. This is in contrast to sequential selection of address lines one at a time in the conventional technique[9]. The technique assumes that the pixels are driven to either ON or OFF state. Hence, the data to be displayed in any column of a matrix with N rows is a N-bit binary pattern, d_1, d2………$d_{N-1,}$ d_N wherein d_j = 0 or 1. Here, logic 0 corresponds to OFF state and logic 1 corresponds to ON state. The rows of the matrix are selected with voltages corresponding to the 2^N binary patterns. Select pattern is represented by r_1, r_2,………..$r_{N-1,}$ r_N where r_j is either logic 0 or logic 1. The steps involved in the binary addressing are summarized in the following text.

1. An N-bit word is chosen as row-select pattern (r_1, r_2, r_3… r_N). The voltage applied to a row is zero for logic 0 and V_s for logic 1;
2. EX-OR gates are used to compare the row select pattern with the data pattern bit-by-bit;
3. The number of mismatches (errors) is determined by counting the number of 1s at the output of N EX-OR gates. The number of errors = $i = \sum_{j=1}^{N} d_j \oplus r_j$;
4. The column voltage is decided by a majority decision. The voltage is 0 (for logic 0) if i is less than N/2 and V_s (for logic 1) otherwise. The condition i=N/2 is avoided by choosing N to be odd. Thus the column voltage is $= \begin{Bmatrix} 0 \;\; for \quad i < (N/2) \\ V_s \;\; for \quad i > (N/2) \end{Bmatrix}$;
5. The column voltages for all the columns in the display is determined by repeating the steps 2 to 4;
6. The row and column voltages are applied simultaneously to the display for a time duration T;
7. A new row select pattern is chosen and the steps 2 to 6 are repeated.
8. A cycle is complete when all the 2^N binary patterns are chosen as row select patterns once;
9. The display is refreshed continuously by repeating this cycle fast enough to avoid flicker in the display.

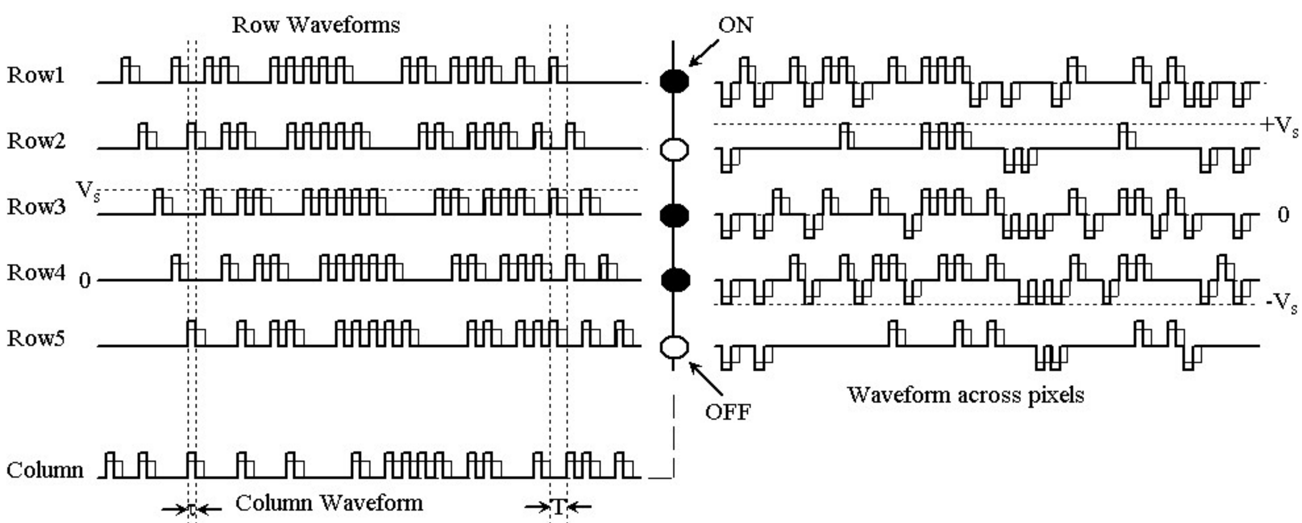

Figure 6: Typical waveforms of the binary addressing technique.

Usually a modified PRBS generator is used to get the 2^N row select patterns[10]. The typical waveforms of the binary addressing technique are shown in Figure 6. The addressing waveforms are inherently dc free and thus polarity inversion is not necessary. The OFF pixel should get an rms very close to threshold voltage in order to achieve maximum contrast in the display. Hence, the amplitude of the pulse (V_s) is determined by equating the rms voltage across OFF pixels to the threshold voltage of the liquid crystal mixture. The supply voltage (V_s) and the selection ratio (SR) in case of binary addressing technique is given by, $V_s = \sqrt{\frac{2^{(N-1)}}{2^{(N-1)} - A}} \times V_{th}$ and $SR = \sqrt{\frac{A}{B}}$ respectively, wherein

$$A = \sum_{i=0}^{\left(\frac{N-1}{2}\right)} \frac{(N-1)!}{i!(N-i-1)!} \quad \text{and} \quad B = \sum_{i=0}^{\left(\frac{N-1}{2}\right)} \frac{i\,(N-1)!}{i!(N-i)!}$$

The amplitude of the drive waveforms is determined by the supply voltage of the CPLD. In the conventional approach the output of the drivers are level shifted to the supply voltage (V_s) of the drive technique. Duty cycle control could be used to avoid this level shifting incase the V_s is less than the supply voltage of the CPLD. The voltages as determined by the addressing technique are applied to the rows and columns of the matrix for a time duration (τ). The output of both row and column drivers are driven to one state corresponding to either logic 0 or logic 1 during rest of the row select time $(T-\tau)$. The rms voltage across the ON and OFF pixels are given by,

$$V_{ON}\,(rms) = \sqrt{\left[\frac{2 \cdot A \cdot (2V_s)^2}{2^N} \times \left(\frac{\tau}{T}\right)\right]} \quad \text{and} \quad V_{OFF}\,(rms) = \sqrt{\left[\frac{2 \cdot B \cdot (2V_s)^2}{2^N} \times \left(\frac{\tau}{T}\right)\right]}$$

It is evident from the above expressions that the display can be driven using a single supply voltage by varying the duty cycle (τ/T).