Sparse Orthogonal Matrices for Scanning Liquid Crystal Displays

T. N. Ruckmongathan and A. R. Shashidhara

***Abstract*—A multi-line addressing technique that is based on sparse orthogonal matrices is proposed to drive the liquid crystal displays (LCDs). Hardware in the column drivers is utilized fully and yet the hardware complexity of the controller is reduced by using sparse matrices to scan the passive matrix LCDs.**

***Index Terms*—Liquid crystal display (LCD) drivers, LCDs, multiplexing, multi-line addressing (MLA), scanning.**

I. Introduction

LIQUID CRYSTAL displays (LCDs) are slow responding devices and hence, their electro-optic response depends on the root mean square (rms) voltage across the pixels. The twisted nematic (TN) and the super twisted nematic (STN) LCDs are examples of such slow responding displays. The picture elements (pixels) in LCDs are arranged to form a two-dimensional array or matrix. Intrinsic nonlinear electro-optic characteristic of the LCD is exploited for multiplexing the passive matrix displays. Techniques that are employed for scanning the matrix LCDs are referred to as matrix addressing or multiplexing. The electrodes that are used to scan the display are referred to as scanning electrodes (or lines). The other set of electrodes are called the data electrodes because the data to be displayed are multiplexed through them. Techniques that are based on selecting several rows simultaneously [1]–[6] are called as multi-line addressing (MLA). Low supply voltage [1], suppression of frame response in the fast responding LCDs [3], [4] and good brightness uniformity of pixels [4], [5] are some of the advantages of MLA as compared to the conventional line-by-line addressing techniques [7], [8]. The MLA techniques are reviewed briefly in the next section.

II. Background

A. Multi-Line Addressing (MLA) Techniques

Scanning electrodes of a matrix display are partitioned in to several subgroups, each consisting of 's' electrodes or address lines. The display is scanned by using waveforms that are derived from orthogonal matrices (or functions). Columns of the orthogonal matrices are referred to as select vectors. Voltages ($+V_r$ or $-V_r$) that are proportional to the elements ($+1$ or -1) of a select vector are applied to the electrodes in the selected subgroup while the unselected scanning electrodes are connected to a mid-voltage corresponding to zero. A voltage that is proportional to the column signal is also applied simultaneously to all the data electrodes in the display. (Dot product of the data vector and the select vector will be referred to as column signal in this paper. Elements of the data vector represent the state of the pixels in a column of a selected subgroup). Subgroups are selected sequentially and a cycle is complete when all the subgroups are selected once with all the select vectors in the orthogonal matrix. Polarity of the scanning and data waveforms is reversed periodically to ensure long life of the display. The display is refreshed by repeating this cycle at about 50 Hz to avoid flicker.

B. Hardware Complexity of MLA Techniques

Hardware complexity of the drivers depends on the number of voltage levels in the addressing waveforms. Orthogonal matrices derived from Walsh, Rademacher functions and Hadamard matrices have elements with just two values i.e., either -1 or $+1$. These orthogonal matrices are preferred to minimize the number of voltage levels in the scanning waveforms and to simplify the computation of column signals.

1) Row Drivers: Scanning (row) waveforms have three voltage levels when the Hadamard matrices are used. Hence, the row drivers of MLA techniques are designed to select one of the three voltages i.e., ($+V_r$ or $-V_r$) corresponding to elements ($+1$ or -1) of the select vector and a mid voltage (0) corresponding to the unselected rows.

2) Column Drivers: Number of voltage levels in the data (column) waveforms depends on the orthogonal matrix employed for scanning the display as well as the number of lines in each subgroup. For example, the number of voltages is $(s+1)$ when "s' scanning electrodes are selected simultaneously with voltages corresponding to the columns of a Hadamard matrix. A schematic diagram of a typical integrated circuit (IC) of the data driver for the MLA techniques is shown in Fig. 1. If N_c is the number of voltage levels in the data (column) waveforms then, the number of data bits is an integer (x) that is greater than or equal to $\log_2 N_c$. A data driver IC with M outputs has M stages of shift register and latch. Every stage of the shift register and latch in the data driver IC has 'x' bits each. Data corresponding to each output of the driver is serially shifted in to the shift register. Contents of the shift register are transferred simultaneously to the latches (in parallel) by using a latch pulse after shifting the data corresponding to all the data electrodes in the display. Hence, the data voltages can be applied simultaneously to all the data electrodes even though the dot products are computed sequentially. Outputs of each

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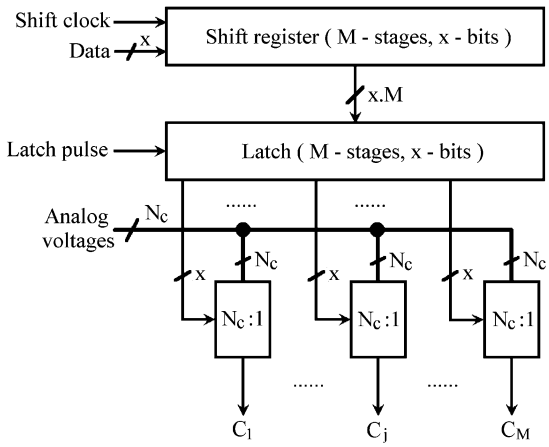

Fig. 1. Schematic diagram of a data driver IC used for MLA.

latch (x-bits) are connected to a decoder (x to N_c) and outputs of the decoder control N_c analog switches. One of the N_c analog voltages is applied to the data electrodes depending on the column signals in the latch. The number of voltage levels in a typical data (column) driver is usually an integer power of two and they have a large number of outputs. For example, data drivers (HD66310T and TMS57206) are capable of selecting any one of the eight voltages using three bits of data in the latch. Although these drivers are primarily designed for active matrix LCDs, they can also be used as data drivers in the passive matrix LCDs.

C. Selection of Number of Rows in a Subgroup

Number of lines that are selected simultaneously (s) is an important parameter of the MLA. The factors that are considered while choosing 's' are outlined here before proposing the technique based on sparse matrices.

1) Based on Parameters of the Addressing Technique: Duty cycle of the addressing waveforms increases with 's'. Although it is advantageous, the hardware complexity of the data driver and the number of times the memory is accessed to fetch the data increases linearly with 's'. Supply voltage of the drive electronics is a minimum when $s = \sqrt{N}$. Although the suppression of frame response is also more effective with increase in 's', the rate of suppression decreases with increase in 's' (diminishing return). It has been shown that 's' in the range of four to eight is adequate to suppress the frame response effectively with a moderate increase in hardware complexity of the drivers [5].

2) Based on the Hardware Complexity of the Controller: Design and implementation of a controller to scan the display by selecting multiple address lines is simple if 's' is an integer power of two. The controller has to generate address to fetch data of pixels in the selected subgroup. It may be generated by multiplying the subgroup (ranges from 0 to N/s) by 's' and adding it to the row number in a subgroup (this ranges from 0 to $(s-1)$. Modulo 's' and modulo (N/s) counters can be used to count the row in a subgroup and the subgroup number. In case 's' is an integer power of two, then these counters are modulo 2^{i} and they can be concatenated. The multiplication as well as the addition necessary for generating the address is eliminated. Similarly, address to fetch the select vector can also be tapped from a binary counter. However, when the number of address lines in a subgroup is an integer power of two then the number of voltage levels in the data waveforms is $(s+1)$ i.e., (2^x+1). Therefore, $(x+1)$ bits are necessary to represent (2^x+1) voltages. Nearly half the capacity of $(x+1)$ bits is not utilized since an additional (2^x-1) voltage levels could be selected with them.

3) Based on Hardware Utilization in the Data Drivers: Hardware in the data drivers must be used efficiently because the number of data electrodes (columns) in the display is large (a few hundreds). The x bits of the shift register as well as the latch, the logic in the x to N_c decoder and the switches in the analog multiplexer in each stage of the driver are fully utilized only when the number of voltage levels in the data waveforms is an integer power of two i.e., $N_c = 2^x$. This in turn implies that 's', the number of electrodes in each subgroup is (2^x-1). This solution is usually not preferred because the generation of address to fetch the image from the memory is complex as compared to the case when $s = 2^x$. The hardware utilization in the data drivers will be better if the data drivers are designed and manufactured for a specific 's'. Then the redundancy in the analog multiplexer can be eliminated. However, under-utilization of bit in each stage of the shift register and latch cannot be avoided even if data drivers are custom designed for a specific 's'.

III. Motivation for Further Research

Either the hardware complexity of the controller can be reduced or the hardware in the data drivers can be used effectively by a proper choice of 's' but not both while using conventional MLA to scan the display. The following factors motivated us to look for new methods.

1. Even in a custom designed data driver, one bit in each stage of the shift register and latch is under-utilized for each column in the matrix display and the number of columns is usually large.
2. Reduction in supply voltage (especially for higher values of N), better suppression of frame response as well as flicker can be achieved by increasing 's'. These advantages should not be lost especially when the data driver has the necessary hardware to drive the display when the number of rows in a subgroup (s) is increased.
3. Advantages of having a simple controller cannot be ignored.

Hardware complexity of the controller has been reduced and the hardware in the data (column) drivers have been fully utilized by using sparse matrices. The MLA technique based on sparse orthogonal matrices is presented next.

IV. MLA Technique Based on Sparse Matrices

A. Principle

Two Hadamard matrices of order 4 are shown in (1) and (2). Elements of these matrices are either $+1$ or -1

$$H_4 = \begin{bmatrix} +1 & +1 & +1 & +1 \\ +1 & -1 & +1 & -1 \\ +1 & +1 & -1 & -1 \\ +1 & -1 & -1 & +1 \end{bmatrix} \tag{1}$$

$$H_4(dig) = \begin{bmatrix} +1 & +1 & +1 & -1 \\ +1 & +1 & -1 & +1 \\ +1 & -1 & +1 & +1 \\ -1 & +1 & +1 & +1 \end{bmatrix} \tag{2}$$

Similarly, the elements of the data vectors represent the state of the pixels. The ON and OFF states are represented by -1 and $+1$ respectively in the data vectors. The column signal has $(s+1)$ distinct values when all the select vectors and the 2^s data vectors are considered. The dot products will have 's' distinct values when a zero is introduced in each column of the orthogonal matrix. For example, the result of dot products of two vectors of order 4 (with $+1$ or -1 as their elements) is one of the five numbers i.e., -4, or -2, or 0, or $+2$, or $+4$. However, the outcome of the dot product is one of the four numbers, viz. -3, or -1 or $+1$, or $+3$ if a zero is introduced in any one of the two vectors. A zero can be introduced in all the select vectors. Introduction of a zero in each column of the orthogonal matrix should be such that the orthogonal property of the matrix is preserved. Otherwise, the modified matrix cannot be used to scan the display.

B. Sparse Orthogonal Matrices of Order 4

We have introduced four zeros in the matrices of (1) and (2) without affecting the orthogonal property. Some matrices that are symmetric as well as orthogonal are shown in (3)–(9). They are not unique and several orthogonal matrices can be found easily.

$$\begin{bmatrix} 0 & +1 & +1 & +1 \\ +1 & -1 & +1 & 0 \\ +1 & +1 & 0 & -1 \\ +1 & 0 & -1 & +1 \end{bmatrix} \tag{3}$$

$$\begin{bmatrix} +1 & 0 & +1 & +1 \\ 0 & -1 & +1 & -1 \\ +1 & +1 & 0 & -1 \\ +1 & -1 & -1 & 0 \end{bmatrix} \tag{4}$$

$$\begin{bmatrix} 0 & +1 & +1 & +1 \\ +1 & 0 & +1 & -1 \\ +1 & +1 & -1 & 0 \\ +1 & -1 & 0 & -1 \end{bmatrix} \tag{5}$$

$$\begin{bmatrix} +1 & 0 & +1 & +1 \\ 0 & +1 & +1 & -1 \\ +1 & +1 & -1 & 0 \\ +1 & -1 & 0 & +1 \end{bmatrix} \tag{6}$$

$$\begin{bmatrix} 0 & +1 & +1 & +1 \\ +1 & 0 & +1 & -1 \\ +1 & +1 & -1 & 0 \\ +1 & -1 & 0 & +1 \end{bmatrix} \tag{7}$$

$$\begin{bmatrix} 0 & +1 & +1 & +1 \\ +1 & 0 & -1 & +1 \\ +1 & -1 & +1 & 0 \\ +1 & +1 & 0 & -1 \end{bmatrix} \tag{8}$$

$$\begin{bmatrix} 0 & +1 & +1 & -1 \\ +1 & +1 & -1 & 0 \\ +1 & -1 & 0 & -1 \\ -1 & 0 & -1 & -1 \end{bmatrix}. \tag{9}$$

C. Sparse Orthogonal Matrices of Order 8

The sparse matrices obtained by modifying Hadamard matrix of order 8 are shown in (10)-(15). Two matrices are shown in each of these equations and a compact notation of '$+$' and '$-$' are used to represent '$+1$' and '-1' repectively.

$$\begin{bmatrix} + & 0 & + & + & + & + & + & + \\ 0 & - & + & - & + & - & + & - \\ + & + & - & - & + & + & 0 & - \\ + & - & - & 0 & + & - & - & + \\ + & + & + & + & 0 & - & - & - \\ + & - & + & - & - & + & - & 0 \\ + & + & 0 & - & - & - & + & + \\ + & - & - & + & - & 0 & + & - \end{bmatrix} \tag{10}$$

$$\begin{bmatrix} + & + & 0 & + & + & + & + & + \\ + & 0 & + & - & + & - & + & - \\ 0 & + & - & - & + & + & - & - \\ + & - & - & + & + & - & - & 0 \\ + & + & + & + & - & 0 & - & - \\ + & - & + & - & 0 & + & - & + \\ + & + & - & - & - & - & 0 & + \\ + & - & - & 0 & - & + & + & - \end{bmatrix} \tag{11}$$

$$\begin{bmatrix} + & + & + & + & + & + & + & 0 \\ + & 0 & + & + & - & - & - & - \\ + & + & 0 & - & - & - & + & + \\ + & + & - & - & + & 0 & - & - \\ + & - & - & + & + & - & 0 & + \\ + & - & - & 0 & - & + & + & - \\ + & - & + & - & 0 & + & - & + \\ 0 & - & + & - & + & - & + & - \end{bmatrix} \tag{12}$$

$$\begin{bmatrix} + & + & + & + & + & + & 0 & + \\ + & 0 & + & + & - & - & - & - \\ + & + & 0 & - & - & - & + & + \\ + & + & - & - & 0 & + & - & - \\ + & - & - & 0 & + & - & - & + \\ + & - & - & + & - & + & + & 0 \\ 0 & - & + & - & - & + & - & + \\ + & - & + & - & + & 0 & + & - \end{bmatrix} \tag{13}$$

$$\begin{bmatrix} + & + & 0 & + & + & + & + & + \\ + & - & - & 0 & + & - & + & - \\ 0 & - & + & + & + & + & - & - \\ + & 0 & + & - & + & - & - & + \\ + & + & + & + & - & - & 0 & - \\ + & - & + & - & - & + & + & 0 \\ + & + & - & - & 0 & + & - & - \\ + & - & - & + & - & 0 & - & + \end{bmatrix} \tag{14}$$

$$\begin{bmatrix} + & + & + & + & + & + & + & 0 \\ + & + & + & 0 & - & - & - & - \\ + & + & - & - & 0 & - & + & + \\ + & 0 & - & - & + & + & - & - \\ + & - & 0 & + & + & - & - & + \\ + & - & - & + & - & 0 & + & - \\ + & - & + & - & - & + & 0 & + \\ 0 & - & + & - & + & - & + & - \end{bmatrix}. \tag{15}$$

The sparse matrix that was obtained by modifying a Hadamard matrix with -1 as the diagonal elements is shown in (16)

$$\begin{bmatrix} -1 & +1 & +1 & +1 & 0 & +1 & +1 & +1 \\ +1 & +1 & -1 & 0 & +1 & +1 & -1 & +1 \\ +1 & -1 & 0 & +1 & +1 & -1 & +1 & +1 \\ +1 & 0 & +1 & -1 & +1 & +1 & +1 & -1 \\ 0 & +1 & +1 & +1 & +1 & -1 & -1 & -1 \\ +1 & +1 & -1 & +1 & -1 & 0 & +1 & -1 \\ +1 & -1 & +1 & +1 & -1 & +1 & -1 & 0 \\ +1 & +1 & +1 & -1 & -1 & -1 & 0 & +1 \end{bmatrix}. \quad (16)$$

It is possible to generate sparse matrices of higher order (greater than eight). We are not considering them here because it has been shown that 's' in the range of four to eight is adequate to suppress the frame response effectively [5] in fast responding LCDs. Sparse matrix of order 2 is an unit matrix and this corresponds to the conventional line by line addressing [7]. Although the term 'sparse matrix' is used to refer matrices with just a few nonzero elements, we have used it for matrices with a few zeros in it due to lack of better terminology. In fact, all the MLA techniques are based on sparse matrices if the unselected subgroups are also taken into consideration. The voltage applied to the unselected rows corresponds to zero. Hence, the orthogonal matrix for scanning the display is a matrix with N rows, having $(N-s+1)$ zeros in each column. It is a sparse matrix because of the number of unselected rows is usually large. For example, a matrix for scanning a display with eight rows that are divided into two subgroups each consisting of four rows is shown in (17)

$$\begin{bmatrix} 0 & +1 & +1 & +1 & 0 & 0 & 0 & 0 \\ +1 & -1 & +1 & 0 & 0 & 0 & 0 & 0 \\ +1 & +1 & 0 & -1 & 0 & 0 & 0 & 0 \\ +1 & 0 & -1 & +1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & +1 & +1 & +1 \\ 0 & 0 & 0 & 0 & +1 & -1 & +1 & 0 \\ 0 & 0 & 0 & 0 & +1 & +1 & 0 & -1 \\ 0 & 0 & 0 & 0 & +1 & 0 & -1 & +1 \end{bmatrix}. \quad (17)$$

D. Technique

The technique for scanning matrix LCDs using sparse matrices is similar to the MLA described in Section II. A. Let us consider a matrix display with N scanning electrodes and arbitrary number of data electrodes. Subgroups are formed by grouping 's' scanning electrodes in each of them. A few (less than 's') dummy rows that are not physically connected to the display may be added if N is not an exact multiple of 's'. Performance of the display will not be affected by the introduction of dummy rows if zero is assigned as the data to the pixels in the dummy rows. Columns of the sparse orthogonal matrices are referred to as select vectors. The scanning is performed by selecting one subgroup at a time with voltages corresponding to the elements of a select vector. Hence, a voltage $+V_r$, or $-V_r$ or zero is applied to the rows in the selected subgroup and a zero is applied to the unselected rows. The corresponding data voltages are also applied to the data electrodes simultaneously. Data voltages $(d.V_c)$ are proportional to the column signal (d),

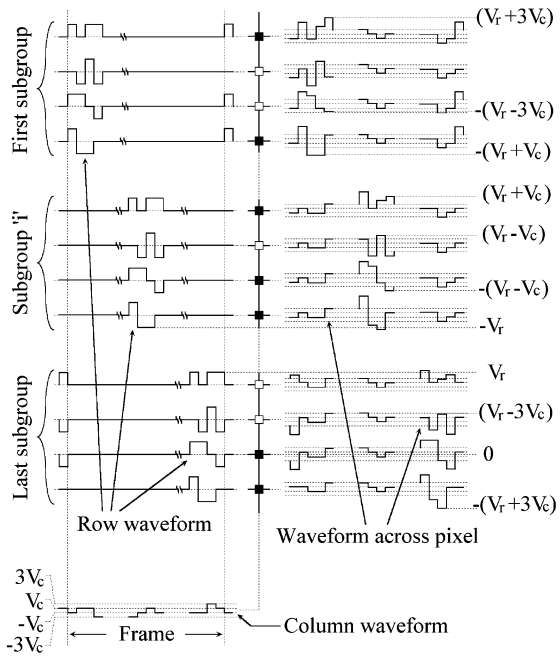

Fig. 2. Typical waveforms when each subgroup is selected with all the select vectors during consecutive time intervals.

the dot product of the select and data vectors. The display is refreshed continuously by selecting all the subgroups with voltages corresponding to all the select vectors at a rate that is fast enough to avoid flicker. Polarity of the scanning and data waveforms is reversed periodically to ensure a dc free operation of the display. Typical addressing waveforms that are applied to the matrix display during a frame (to complete addressing of all the pixels in the display) are shown in Fig. 2. These waveforms could be made dc free by reversing the polarity of all the scanning and data waveforms in the following frame. An analysis of the MLA technique based on sparse matrix is presented in the next section.

E. Analysis

The rms voltages across ON and OFF pixels are given in the following expressions:

$$V_{\mathrm{ON}}(\mathrm{RMS}) = \sqrt{\frac{(s-1)\left(V_r^2 + 2V_rV_c + \mathrm{NV}_c^2\right)}{N}} \quad (18)$$

$$V_{\mathrm{OFF}}(\mathrm{RMS}) = \sqrt{\frac{(s-1)\left(V_r^2 - 2V_rV_c + \mathrm{NV}_c^2\right)}{N}}. \quad (19)$$

The selection ratio of an addressing technique is defined as the ratio of RMS voltages across ON pixels to that across the OFF pixels.

$$\text{Selection ratio} = \frac{V_{\mathrm{ON}}(\mathrm{RMS})}{V_{\mathrm{OFF}}(\mathrm{RMS})} = \sqrt{\frac{\sqrt{N}+1}{\sqrt{N}-1}}. \quad (20)$$

It is equal to the maximum selection ratio that is achievable by any addressing technique [9].

Supply voltage of a technique is decided by the maximum swing in the addressing waveforms and it is obtained by equating the RMS voltage across the OFF pixels to the threshold

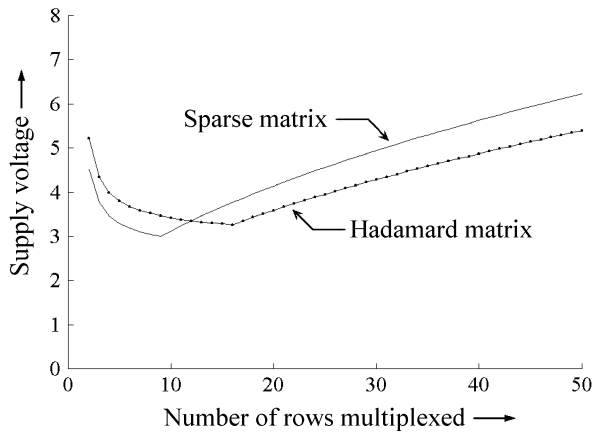

Fig. 3. Supply voltage—A comparison $(s = 4)$.

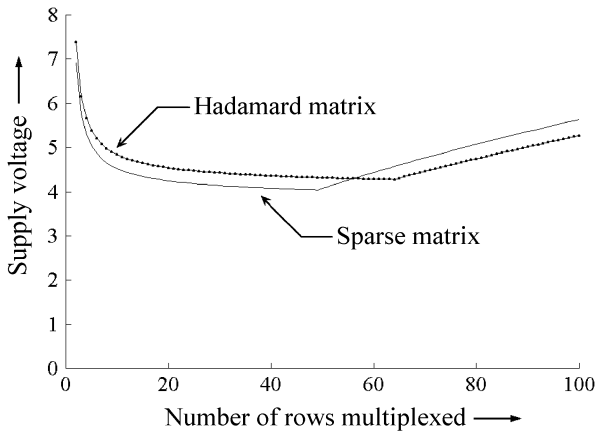

Fig. 4. Supply voltage—A comparison $(s = 8)$.

voltage $(V_{\text{threshold}})$ of the LCD. Supply voltage of this technique depends on the number of scanning electrodes (N) as well as the number of electrodes in each subgroup (s). Amplitude of the waveforms applied to the data electrodes is greater than that of the scanning electrodes when $N \leq (s-1)^2$ and the amplitude of the waveforms applied to the scanning electrodes is higher if $N \geq (s-1)^2$. Expressions for the supply voltage of the MLA technique based on sparse matrices are given in (21) and (22)

$$V_{\text{supply}} = \sqrt{\frac{2(s-1)N}{(N-\sqrt{N})}}V_{\text{threshold}}, \qquad \forall \quad N \leq (s-1)^2 \tag{21}$$

$$V_{\text{supply}} = \frac{\sqrt{2}NV_{\text{threshold}}}{\sqrt{(s-1)(N-\sqrt{N})}}, \qquad \forall \quad N \geq (s-1)^2. \tag{22}$$

Supply voltage of the MLA when Hadamard matrix of order 's' is used to select the subgroups is given in (23) and (24)

$$V_{\text{supply}} = \sqrt{\frac{2sN}{(N-\sqrt{N})}}V_{\text{threshold}} \quad \forall \quad N \leq s^2 \tag{23}$$

$$V_{\text{supply}} = \frac{\sqrt{2}NV_{\text{threshold}}}{\sqrt{s(N-\sqrt{N})}} \qquad \forall \quad N \geq s^2. \tag{24}$$

Supply voltages (normalized to the threshold voltage of the LCD) are compared in Figs. 3 and 4 when the number of lines in a subgroup (s) is 4 and 8, respectively. Supply voltage of the MLA technique using sparse matrices is the same as that of selecting $(s-1)$ address lines in MLA with Hadamard matrices. Supply voltage of the technique based on sparse matrix of order 's' is less by a factor $\sqrt{(s-1)/s}$ as compared to that of MLA technique based on Hadamard matrix of order 's' when $N \leq (s-1)^2$. The supply voltages are equal when $N = s(s-1)$. It is higher by a factor $\sqrt{s/(s-1)}$ for the technique based on sparse matrices when $N \geq s^2$.

F. Selection of Scanning Sequences

The term scanning sequence refers to the manner in which the subgroups are selected with select vectors. A subgroup may be selected by using a subset of select vectors before moving on to another subgroup. The new subgroup may be selected using the same subset of select vectors or a different subset of select vectors. A cycle is complete when all the subgroups are selected once with all the select vectors. Theoretically, the RMS voltage across the pixels driven to the same state should be independent of the scanning sequence. However, the distortion in the addressing waveforms due to the finite resistance of the switches in the analog multiplexers of the driver IC and capacitance of the pixels cannot be ignored. The rms voltage across the pixels decreases as the number of transitions in the addressing waveforms increases. Therefore, the pixels driven to the same state will appear different and this is referred to as brightness nonuniformity of pixels. Hence, the scanning sequence plays an important role in the brightness uniformity of pixels. Although the brightness uniformity can be improved by reducing the resistance of switches, it cannot be reduced beyond a point because the number of devices per unit area in the driver IC will decrease. Good brightness uniformity can be achieved if the number of transitions in the waveforms across the pixels is equal for all the pixels that are driven to the same state. Number of transitions in the scanning waveform is same if each subgroup is selected with just one select vector before moving on to another subgroup. The brightness uniformity will be excellent if the number of transitions in the waveform across the pixels is independent of the image (data being displayed). This could be achieved to some extent if the select vectors are different for the two consecutive subgroups i.e., the select vector is also changed when a new subgroup is selected. This scanning sequence has been used in our prototype and the waveforms are shown in Fig. 9. On the other hand the scanning sequence shown in Figs. 2 and 5 are not good from the point of brightness uniformity because, the number of transitions in the row waveforms are not equal.

V. Implementation

The technique has been demonstrated using a 32×32 matrix LCD by selecting eight rows at a time. Some aspects of the

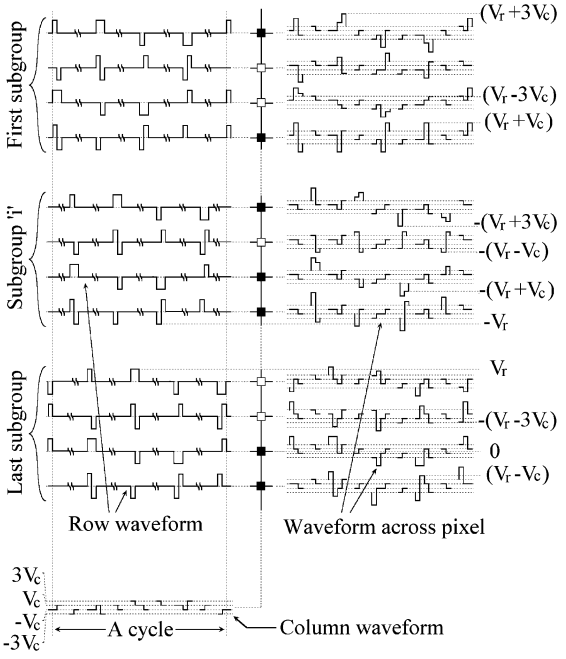

Fig. 5. Typical waveforms of MLA technique based on sparse matrix with distributed row select pulses.

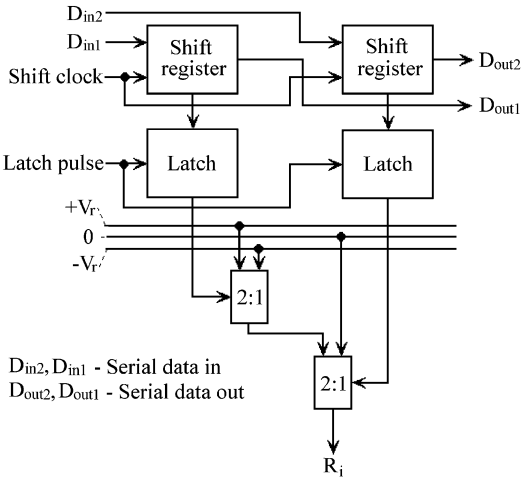

Fig. 6. Schematic diagram of single stage of the row driver printed circuit board for the MLA technique.

hardware implementation of the prototype are discussed in this section.

A. Row Driver for the Scanning Electrodes

Row driver has to select one out of three voltages and the complexity of the row driver is same as that of MLA. The row driver has been implemented using sixty-four 2:1 analog multiplexers (CD-4053) and eight numbers of serial in parallel out shift register with latches (HC-74 595). Schematic diagram of a stage in the row driver board is shown in Fig. 6. The elements of the select vector are shifted in as D_{in1} and the corresponding 2:1 multiplexer selects $+V_r$ or $-V_r$. The D_{in2} is the mask bit and the corresponding 2:1 multiplexer selects either the out of the first 2:1 multiplexer or a '0'. The mask bit ensures that '0', a mid-voltage is applied when the element of the scanning matrix is zero. These zeros correspond to the unselected rows or the

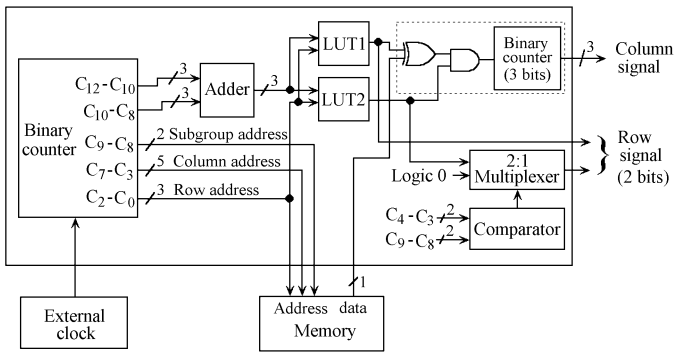

Fig. 7. Block diagram of a controller.

zeros in the sparse matrix. This driver can be used for the MLA technique based on either the sparse or the Hadamard matrices.

B. Column Driver for the Data Electrodes

Thirty-two numbers of CD-4051 (8:1 analog multiplexers) and two SED-1180 (LCD drivers) are used to implement the column driver. Forty-eight stages in each SED-1180 are used to shift and latch the column signals. Output of these stages selects one of the eight voltages using a CD-4051. Output of each analog multiplexer is connected to a data electrode.

C. Controller for Scanning the Display

Block diagram of a controller is shown in Fig. 7. An orthogonal sparse matrix of order 8 is stored in the form of lookup tables (LUTs). The orthogonal matrix of order 8 is stored in LUT-1 while the mask bits are stored in LUT-2. The mask bit is logic zero for a '0' in the sparse matrix and it is logic one otherwise. The image is stored in a bit mapped memory. A binary counter is used to generate address bits for the memory, select inputs for the look-up tables and other control signals as described in this section. Data corresponding to the state of eight pixels in each column of the selected subgroup are used to generate column signals. Bits (C_2 to C_0) of the binary counter are used for this purpose and they are the least significant bits of the row address of the bit-mapped memory. There are thirty-two columns in the display and bits (C_7 to C_3) are the column address of the memory. The bits (C_9 to C_8) correspond to the four subgroups in the display and they are the most significant bits of the row address. Bits (C_{12} to C_{10}) of the binary counter may be used to choose a select vector from the memory. This ensures that each subgroup is selected once during a scan but with the same select vector. It is preferable to change the select vector whenever a subgroup is selected and this can be achieved by adding (C_{12} to C_{10}) to (C_{10} to C_8) and using the output bits (just the sum outputs and the carry bit is ignored) to choose a select vector from LUT-1. This ensures that a new select vector is used whenever a subgroup is selected. A good brightness uniformity of pixels is ensured when this sequence is used to scan the display as discussed in Section IV-F. The select inputs of the LUT-2 are the same as that of LUT-1 because LUT-2 is used to introduce the zero in the orthogonal matrix to obtain the elements of the sparse matrix. The Column signals are generated serially using an ex-or gate and a counter with three-bits. The row address bits (C_2 to C_0) are also used to obtain the elements

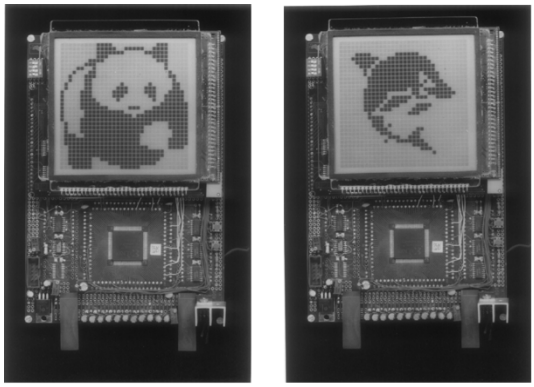

Fig. 8. Photographs of the prototype of a matrix LCD that is scanned using sparse matrix of order 8.

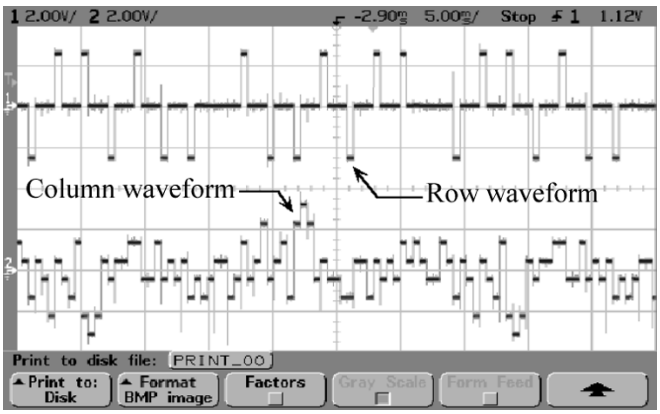

Fig. 9. Typical waveforms applied to the row (scanning) and column (data) electrodes.

of the select vector. Generation of the control signal to fetch, compute, shift and latch data in to the drivers is also simple since the number of rows and columns in the matrix LCD are also integer powers of two. The controller has been implemented using 90 logic macro-cells, 39 registers, and 404 product terms in a complex programmable logic device (CPLD).

VI. Results

The photographs of the prototype that demonstrates the technique are shown in Fig. 8. Typical addressing waveforms, i.e., scanning (row) and data (column) waveforms are shown in Fig. 9. The waveform across an ON pixel is shown in Fig. 10. A plot of rms voltages across ON and OFF pixels as a function of supply voltage is shown in Fig. 11. We have verified that the response times are not affected by the new addressing technique. Response of the display was measured using a cell filled with ZLI-2701 liquid crystal mixture and the switch ON and turn OFF characteristics when 32 rows are multiplexed using sparse matrix by selecting eight rows at a time is shown in Fig. 12. The response was also measured when the pixel is driven by selecting eight rows simultaneously using the conventional MLA. The response times were same as that when sparse matrix was used. Response times were also measured for the line by line addressing technique and we found that the response times did not change significantly as long as the number of lines multiplexed is same.

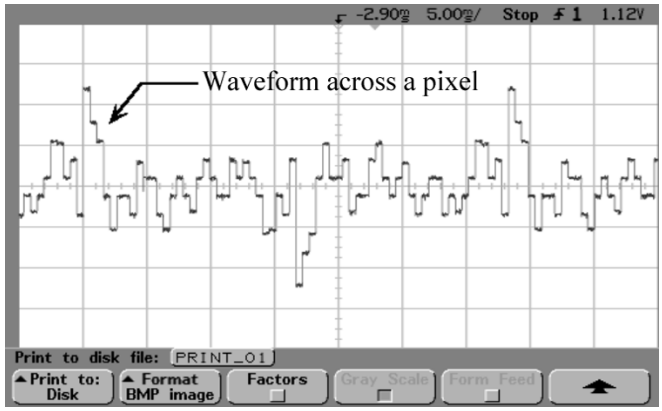

Fig. 10. Typical waveform across a pixel in the matrix display that is driven using a sparse matrix.

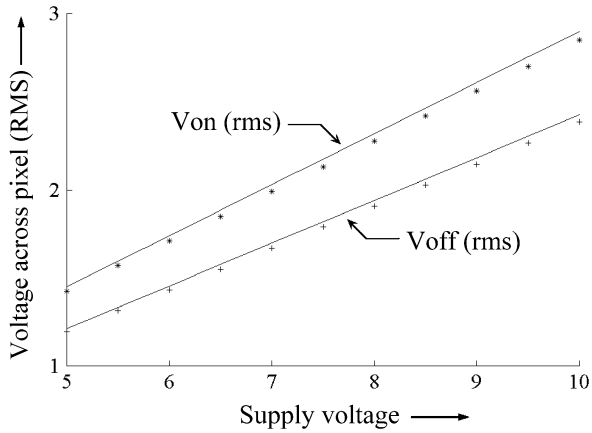

Fig. 11. The rms voltage across pixels versus Supply voltage.

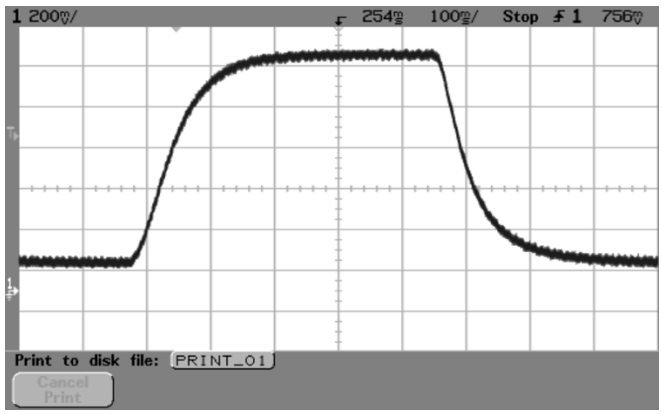

Fig. 12. Typical response of a pixel when 32 rows are multiplexed by selecting eight rows at a time using sparse matrix of order 8.

VII. Impact

As discussed earlier, either the hardware complexity of the controller can be reduced or the hardware in the data driver can be utilized fully but not both when conventional MLA technique is used. We have achieved full utilization of the circuit elements in the column drivers (shift register, latch, decoder as well as

analog switches) even when $s = 2^x$. Hence, the controller to scan the display is simple and most of the control signals are derived from a binary counter using some logic gates. A higher 's' is useful to suppress frame response and reduce the supply voltage. Supply voltage and the suppression of frame response will be equivalent to that of selecting seven rows $(s = 7)$ simultaneously in the conventional MLA when a sparse matrix of order 8 is used. Supply voltage is less by about 25% (if N, the number of lines multiplexed is greater than 50) and efficiency of suppression of frame response better by 15% to 25% [5] if a sparse matrix of order 8 is used instead of Hadamard matrix of order 4 to scan the display. The hardware complexity of the controller is the same when 's' is four or eight (integer powers of two).

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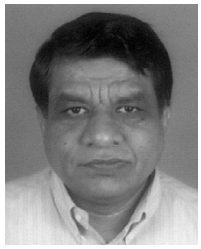

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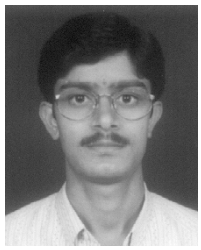
Prof. Ruckmongathan is a member of the Society for Information Display.



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