Gray shades in LCDs using Amplitude Modulation

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ABSTRACT

Gray shades are essential to reproduce images on displays. Amplitude modulation technique allows a large number of gray shades to be displayed in liquid crystal displays (LCDs). Number of voltage levels in the addressing waveforms of amplitude modulation is at least twice the desired number of gray shades. Hence, hardware complexity of the column driver is high as compared to other techniques for displaying gray shades. We propose a technique to reduce hardware complexity of the column driver for amplitude modulation by about 50%. The design of a controller for amplitude modulation based on line-by-line addressing is also discussed.

Keywords: Gray shades, matrix LCDs, Amplitude modulation, controller, LCD drivers

1. INTRODUCTION

Liquid crystal displays are low power devices and find application in a wide range of portable products such as mobile phones, calculators, cameras etc. Gray shades are essential to reproduce images faithfully on the display. There are several techniques to display gray shades in passive matrix LCDs and they are briefly discussed here. These techniques may be used with line-by-line addressing[1] and multi-line addressing techniques[2]. Slow response of LCDs can be exploited to display gray shades by driving the pixel either to ON or OFF states in successive frames. This technique is referred to as frame rate control (FRC)[3] or frame modulation. It can be used to display $(k+1)$ gray shades using k frames. However, the number of frames to complete a cycle increases while displaying a large number of gray shades, and this may result in flicker. Another method to display gray shades is pulse width modulation[4], wherein voltages corresponding to ON state are applied to the pixels during a fraction of the row select time and voltages corresponding to OFF state are applied during the remaining time. The duty cycle of the ON voltage can be varied to display gray shades. Pulse widths are narrow when the number of gray shades is large and this may result in poor brightness uniformity of pixels in the display. Number of frames (or time intervals) required to complete a cycle is reduced to the logarithm of the number of gray shades displayed, in row pulse height modulation[5] as well as successive approximation[6] techniques. Hence, 2^k gray shades can be displayed using k frames by assigning a frame to each bit and scanning the display by modulating the amplitude of the waveforms. In row pulse height modulation the amplitude of the row waveforms are modulated by the binary weight $2^{(b-1)}$ corresponding to the bit $b(1 \le b \le k)$ used to scan the display. The selection ratio of this technique is lower than the maximum selection ratio that can be attained by the matrix addressing schemes. Successive approximation technique overcomes this disadvantage and achieves the maximum selection ratio by modulating amplitudes of both row and column waveforms by a factor $\sqrt{2^{(b-1)}}$, when bit b is used for scanning the display. Two time slots are adequate to display gray shades in line-by-line addressing using amplitude modulation [7,8] (also referred to as pulse height modulation [9]). This is achieved at the cost of increased hardware complexity since the number of voltages necessary to display gray shades is large. The amplitude modulation scheme is described in the following section.

2. AMPLITUDE MODULATION

Amplitude modulation[7, 8], also referred to as pulse height modulation[9] is a technique for displaying a large number of gray shades using minimum number of time intervals. Let us consider a pixel with gray shade g_{ij} at the intersection of the i^{th} row and the j^{th} column. The gray shade g_{ij} is normalized and lies in the range of +1 and –1. Here +1 corresponds to OFF state and –1 corresponds to ON state respectively. Rows of the matrix are selected sequentially with a pulse of amplitude V_r in amplitude modulation based on line-by-line addressing, while the unselected rows are

grounded. Each row select time is divided into two equal time slots. A voltage of amplitude $(g_{ij} + \sqrt{1-g_{ij}^2})V_c$ is applied to the j^{th} column during one slot and a voltage of amplitude $(g_{ij} - \sqrt{1-g_{ij}^2})V_c$ is applied during the other slot when the i^{th} row is selected. All rows in the matrix are selected sequentially to complete scanning of a frame. The display is refreshed at a rate (~50Hz) that is fast enough to avoid flicker. The root mean square (rms) voltage across a pixel during a frame is given by

$$V_{i,j}\ (rms) = \sqrt{\frac{\left[V_r - (g_{ij} + \sqrt{1-g_{ij}^2})V_c\right]^2 + \left[V_r - (g_{ij} - \sqrt{1-g_{ij}^2})V_c\right]^2 + \sum_{\substack{k=1 \\ k\neq i}}^{k=N}\left\{\left[(g_{kj} + \sqrt{1-g_{kj}^2})V_c\right]^2 + \left[(g_{kj} - \sqrt{1-g_{kj}^2})V_c\right]^2\right\}}{2N}}$$

$$V_{i,j}(rms) = \sqrt{\frac{V_r^2 - 2\,g_{ij}V_rV_c + NV_c^2}{N}} \qquad (2)$$

The rms voltage across the pixel depends on the gray shade g_{ij} of the pixel as evident from equation (2). Selection ratio of an addressing technique is defined as the ratio of the rms voltage across ON pixels to that across OFF pixels. The selection ratio of line-by-line addressing is a maximum when $V_r = \sqrt{N}\,V_c$. The waveforms across the pixels must be dc free for long life of the display. Hence, the polarity of the row and column waveforms are reversed periodically to ensure a dc free operation. Several variants of the amplitude modulation scheme have also been reported[8]. The row and column voltages of the amplitude modulation scheme[8] and two of its variants are listed in Table 1. Voltages to be applied upon reversing the polarity are indicated within the parenthesis. All the voltages in Table 1 are normalized with respect to V_c, which is the magnitude of the voltage to be applied to obtain the extreme gray shades i.e. ON and OFF states. Typical addressing waveforms of schemes I and II are shown in figures 1 and 2 respectively The row waveforms in the schemes II and III are dc free within a row select time and hence only the column voltages contribute to a dc voltage across the pixels during a frame. The net dc voltage to be compensated during polarity reversal is much smaller when schemes II or III are used since the column voltages in line by line addressing are smaller in amplitude than the row voltages.

Table 1. Variants of the amplitude modulation scheme

	Scheme I		**Scheme II**		**Scheme III**	
Time slot	**First**	**Second**	**First**	**Second**	**First**	**Second**
Row voltage	$\sqrt{N}$ $\left(-\sqrt{N}\right)$	$\sqrt{N}$ $\left(-\sqrt{N}\right)$	$\sqrt{N}$ $\left(-\sqrt{N}\right)$	$-\sqrt{N}$ $\left(\sqrt{N}\right)$	$\sqrt{N}$ $\left(-\sqrt{N}\right)$	$-\sqrt{N}$ $\left(\sqrt{N}\right)$
Column voltage	$g_{ij} + \sqrt{1-g_{ij}^2}$ $\left(-g_{ij} - \sqrt{1-g_{ij}^2}\right)$	$g_{ij} - \sqrt{1-g_{ij}^2}$ $\left(-g_{ij} + \sqrt{1-g_{ij}^2}\right)$	$g_{ij} + \sqrt{1-g_{ij}^2}$ $\left(-g_{ij} - \sqrt{1-g_{ij}^2}\right)$	$-g_{ij} + \sqrt{1-g_{ij}^2}$ $\left(g_{ij} - \sqrt{1-g_{ij}^2}\right)$	$g_{ij} - \sqrt{1-g_{ij}^2}$ $\left(-g_{ij} + \sqrt{1-g_{ij}^2}\right)$	$-g_{ij} - \sqrt{1-g_{ij}^2}$ $\left(g_{ij} + \sqrt{1-g_{ij}^2}\right)$

Power consumption of the amplitude modulation techniques can be computed based on a model proposed by Burton Marks[10]. The pixels in the matrix display are modeled as capacitors. The power consumption of the drive electronics is the power dissipated in the output resistance of the drivers while charging the pixel capacitances to the voltages as specified by the addressing technique. Let us consider a single column of a matrix with N rows. Let the gray shades in rows $(i-1)$ and (i) of the matrix be $g_{(i-1)}$ and g_i respectively. The waveforms across pixels in a column while selecting the $(i-1)^{th}$ and $(i)^{th}$ rows in schemes I and II are shown in figures 1 and 2 respectively. Power consumption of the drive electronics while using scheme III will be same as that of scheme II.

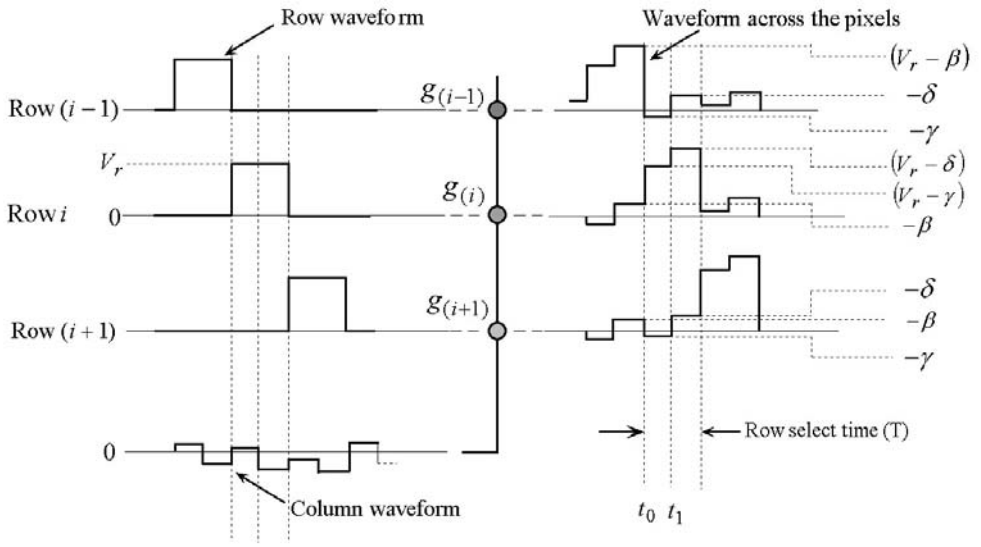

Figure 1. Typical addressing waveforms for amplitude modulation using scheme I

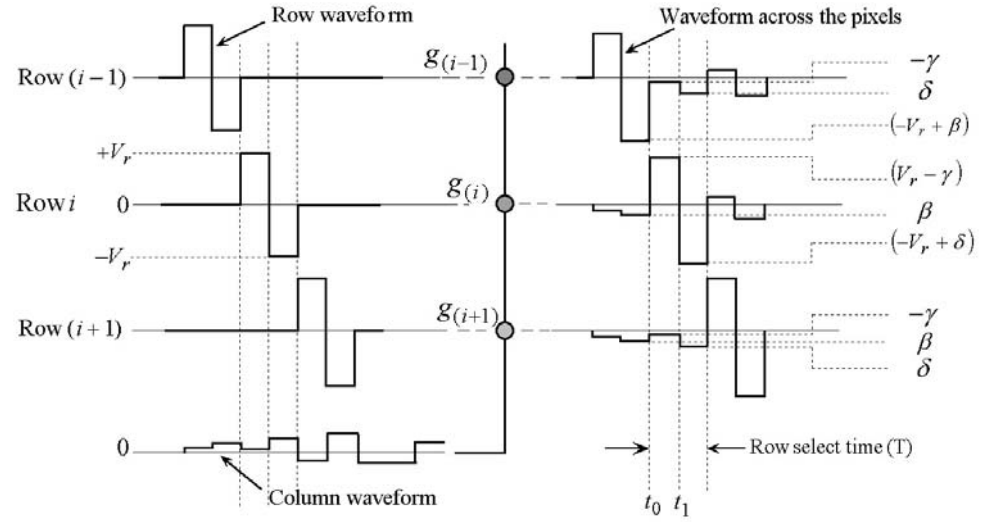

Figure 2. Typical addressing waveforms for amplitude modulation using scheme II

The power consumption of these schemes during a row select time (T) is computed by taking into account the transitions in the waveforms across all pixels in the column during T, i.e. voltage transitions at time t_0 and t_1. The expressions for power consumption of scheme I and II during the row select time are given in equation 3 and 4 respectively.

$$P1 = CV_c^2\left[N + \frac{N}{2}\left(\beta^2 + 2\gamma^2 + \delta^2 - 2\beta\gamma - 2\gamma\delta\right)\right] \tag{3}$$

$$P2 = CV_c^2\left[3N - 2\sqrt{N}\left(\beta + 2\gamma + \delta\right) + \frac{N}{2}\left(\beta^2 + 2\gamma^2 + \delta^2 + 2\beta\gamma + 2\gamma\delta\right)\right] \tag{4}$$

Wherein $\beta = g_{(i-1)} - \sqrt{1 - g_{(i-1)}^2}$, $\gamma = g_{(i)} + \sqrt{1 - g_{(i)}^2}$ and $\delta = g_{(i)} - \sqrt{1 - g_{(i)}^2}$. Although the capacitance of the pixels depends on the gray shade it is driven to, we have used an average value (C) in these equations. The power consumption while displaying a specific pattern of gray shades in a column can be obtained by summing the power consumption during the N row select intervals for the specific values of gray shades ($g_{(i-1)}$ and g_i). The power consumption of a panel with M columns can be obtained by summing up the powers computed separately for each of these M columns. Scheme I consumes less power for about 50% of all the combinations of $g_{(i-1)}$ and g_i while scheme II is advantageous for the remaining combinations. Hence there is no distinct advantage while using one scheme over the other with regard to power consumption.

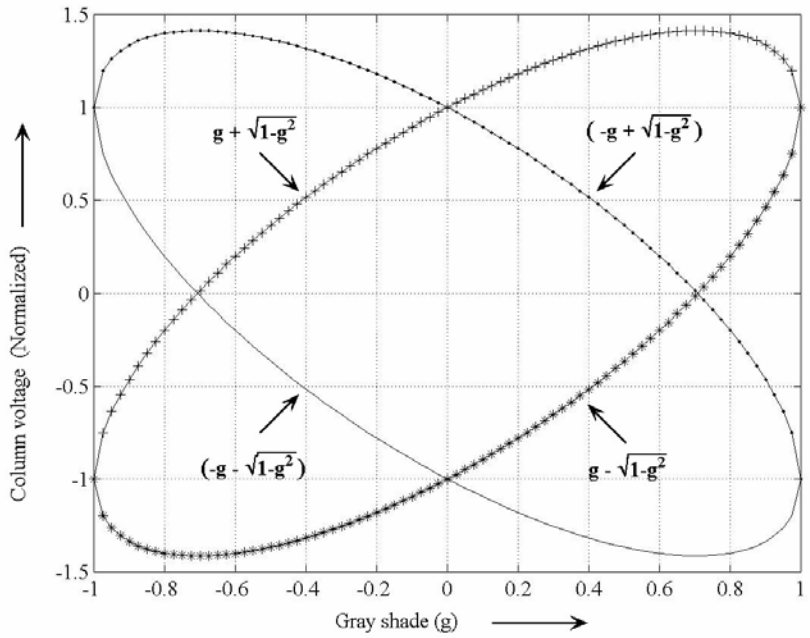

Figure 3. Column voltages for various gray shades

In the amplitude modulation schemes described above, each output of the row driver has to select one of three voltages i.e. $(+V_r)$, (0) and $(-V_r)$. The number of column voltages depends on the number of gray shades to be displayed. Plots of column voltages to be applied during the two time slots are shown in figure 3 for the scheme I. Column voltages used during the polarity reversal have also been plotted. Column voltage in each slot traces a segment of an ellipse for various values of gray shades (g_{ij}) . The two segments meet when the gray shades have extreme values i.e. $(g_{ij} = -1)$ or $(g_{ij} = +1)$ which correspond to ON and OFF states respectively. Each of the g gray shades needs four distinct column voltages when the polarity reversal is also taken into consideration. This results in a total of $(4g - 4)$ voltages for g gray shades. However if the gray shades are symmetrically spaced between +1 and –1 then a pair of symmetrically spaced gray shades viz. (k and $-k$) share a common set of four voltage levels. Thus the number of voltages required for g gray shades reduces to $(2g - 2)$. It is approximately equal to $2g$ when a large number of gray shades are displayed. Drawback of the amplitude modulation scheme is that a large number of voltages are necessary to display the gray shades. The driver stage of each column has to select one out of $2g$ voltages to display g gray shades. However the technique needs just g voltages corresponding to either $\left(g_{ij} + \sqrt{1 - g_{ij}^2}\right)$ or $\left(g_{ij} - \sqrt{1 - g_{ij}^2}\right)$ during a time slot as evident from figure 3. Thus only g voltages are necessary at a given instant of time to display g gray shades. This fact has been used to reduce the complexity of the column driver to about 50%. The column voltages (normalized to V_c) for displaying eight gray shades using the amplitude modulation schemes are listed in Table 2. Volatges to be applied upon polarity reversal are shown in

parenthesis. It is evident from Table 2 that only eight out the fourteen voltages are necessary during any time slot. This information is used to simplify the column driver for the amplitude modulation schemes. Reduction in the hardware complexity of the drivers and details of a prototype that has been developed to demonstrate this technique are presented in the next section.

Table 2. Column voltages for displaying eight gray shades in amplitude modulation schemes

		Column voltages					
		Scheme 1		Scheme 2		Scheme 3	
Gray shade (g)	**Data code**	$g_{ij}+\sqrt{1-g_{ij}^2}$ $\left(-g_{ij}-\sqrt{1-g_{ij}^2}\right)$	$g_{ij}-\sqrt{1-g_{ij}^2}$ $\left(-g_{ij}+\sqrt{1-g_{ij}^2}\right)$	$g_{ij}+\sqrt{1-g_{ij}^2}$ $\left(-g_{ij}-\sqrt{1-g_{ij}^2}\right)$	$-g_{ij}+\sqrt{1-g_{ij}^2}$ $\left(g_{ij}-\sqrt{1-g_{ij}^2}\right)$	$g_{ij}-\sqrt{1-g_{ij}^2}$ $\left(-g_{ij}+\sqrt{1-g_{ij}^2}\right)$	$-g_{ij}-\sqrt{1-g_{ij}^2}$ $\left(g_{ij}+\sqrt{1-g_{ij}^2}\right)$
-1	000	-1 (1)	-1 (1)	-1 (1)	1 (-1)	-1 (1)	1 (-1)
$-\left(\frac{5}{7}\right)$	001	-0.0144 (0.0144)	-1.4141 (1.4141)	-0.0144 (0.0144)	1.4141 (-1.4141)	-1.4141 (1.4141)	0.0144 (-0.0144)
$-\left(\frac{3}{7}\right)$	010	0.4750 (-0.4750)	-1.3320 (1.3320)	0.4750 (-0.4750)	1.3320 (-1.3320)	-1.3320 (1.3320)	-0.4750 (0.4750)
$-\left(\frac{1}{7}\right)$	011	0.8470 (-0.8470)	-1.1326 (1.1326)	0.8470 (-0.8470)	1.1326 (-1.1326)	-1.1326 (1.1326)	-0.8470 (0.8470)
$+\left(\frac{1}{7}\right)$	100	1.1326 (-1.1326)	-0.8470 (0.8470)	1.1326 (-1.1326)	0.8470 (-0.8470)	-0.8470 (0.8470)	-1.1326 (1.1326)
$+\left(\frac{3}{7}\right)$	101	1.3320 (-1.3320)	-0.4750 (0.4750)	1.3320 (-1.3320)	0.4750 (-0.4750)	-0.4750 (0.4750)	-1.3320 (1.3320)
$+\left(\frac{5}{7}\right)$	110	1.4141 (-1.4141)	0.0144 (-0.0144)	1.4141 (-1.4141)	-0.0144 (0.0144)	0.0144 (-0.0144)	-1.4141 (1.4141)
$+1$	111	1 (-1)	1 (-1)	1 (-1)	-1 (1)	1 (-1)	-1 (1)

3. HARDWARE IMPLEMENTATION

The row driver for the amplitude modulation technique is discussed first for the sake of completeness.

3.1. Row driver

A single stage of a row driver for the amplitude modulation technique is shown figure 4a.This stage comprises of a shift register, a latch and a 3:1 analog multiplexer. The output of the analog multiplexer is the row waveform that is used to select or unselect a row. A signal Q_1 is used to control the periodic reversal of the polarity of the addressing waveforms to achieve a dc free operation. The signal Q_2 is used to indicate the sign of the row select voltage during the two time slots. Since the sign of the row select voltage is the same during a row select time in scheme I, the signal Q_2 is assigned

logic ‘0’. Sign of the row select voltage changes from the first slot to the second in the schemes II and III. Hence the signal Q_2 is logic ‘0’ during the first time slot and changes to logic ‘1’ during the second time slot. The signals Q_1 and Q_2 are EX-ORed to generate a polarity signal P that selects the row select voltage ($+V_r$ or $-V_r$) at any given instant of time. The voltage for unselected rows is independent of this control signal and equal to zero volts for all the amplitude modulation schemes described here. Each output of the latch selects one of two voltages corresponding to either selected or unselected states. Logic ‘0’ at the output of the latch corresponds to unselected row while a logic ‘1’ corresponds to a selected row. The popular line-by-line addressing scheme (Improved Alt and Pleshko Technique[11]) uses four row voltages of which only two are used at a given instant of time. Most of the standard row drivers for this technique make use of this fact and have a common bus providing the select and unselect voltages to all the stages of the driver. Voltages on this bus are switched using two 2:1 analog multiplexers. These multiplexers are controlled by the polarity signal P. As a result of this common selection, the output stage has 2:1 analog multiplexers instead of 3:1 analog multiplexers. The schematic of this driver is shown in figure 4b. The output of the last stage of the shift register is available on a pin, so that a number of drivers could be cascaded when a single driver IC is not sufficient for a given application. These standard drivers may be used for amplitude modulation by connecting both the unselect inputs to zero volts. SED1190F, a common driver is used as the row driver in our prototype. The column driver is discussed in the next subsection.

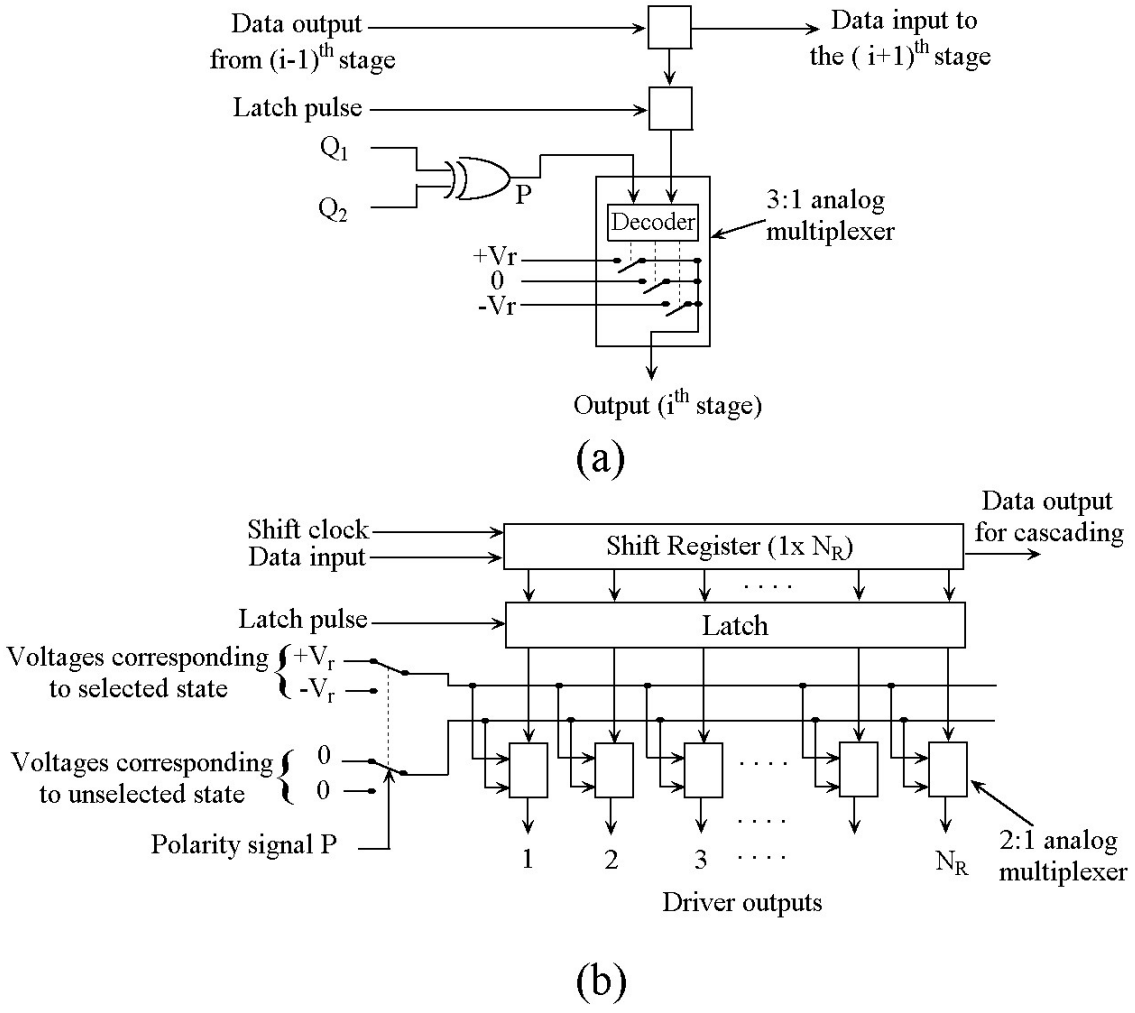

Figure 4. Schematic of a row driver

3.2. Column driver

A single stage of a typical column driver is shown in figure 5. The driver comprises of a shift register, latch and an analog multiplexer. The shift register indicated in figure 5 allows x data bits to be shifted in parallel; wherein x indicates the number of bits required to represent q_v i.e. $x = \lceil \log_2(q_v) \rceil$. These data bits can be latched and used to select one of q_v analog inputs to the multiplexer.

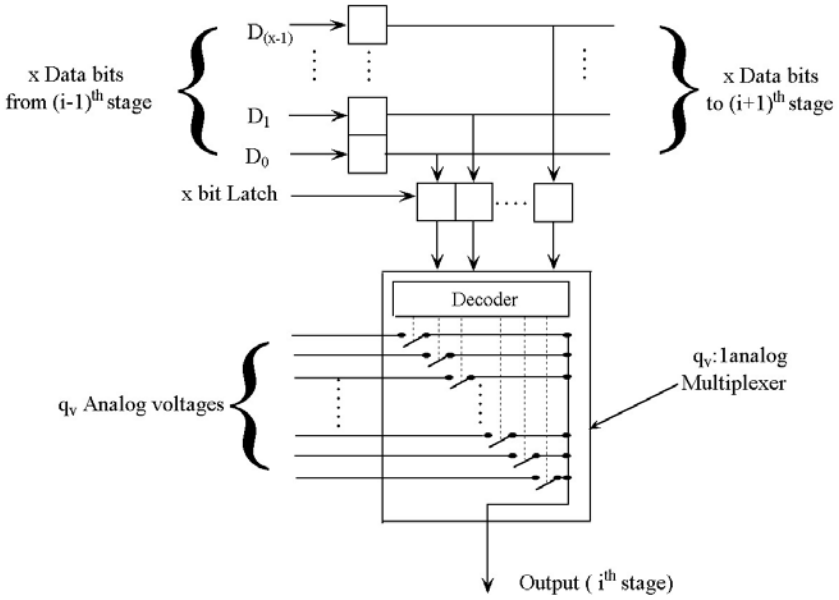

Figure 5. Single stage of a typical column driver

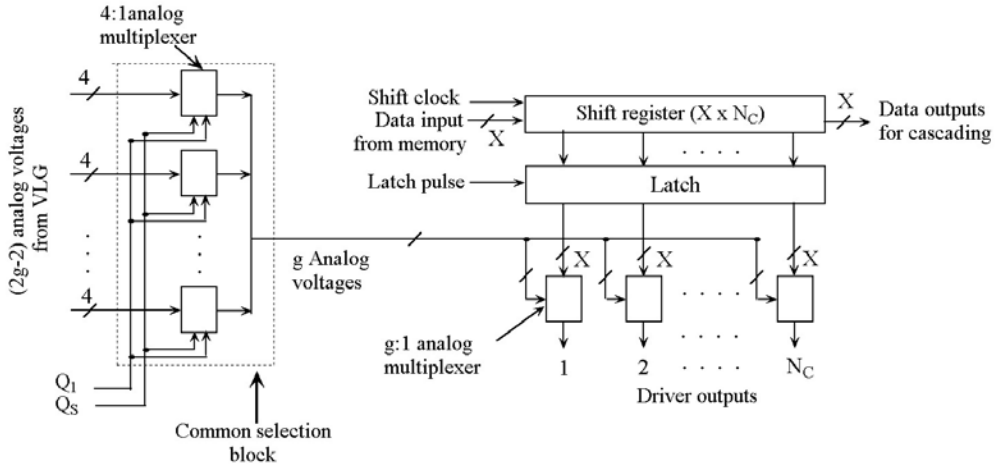

Figure 6. Schematic of a column driver for amplitude modulation

The signal Q_1 is used to control the periodic reversal of the polarity of the addressing waveforms to achieve dc free operation. The signal Q_S is used to distinguish between the two time slots. The signal Q_S is logic '0' during the first time slot and logic '1'during the second time slot for all the amplitude modulation schemes. As discussed in section II, $(2g-2)$ voltages are necessary to display g gray shades using amplitude modulation. However just g voltages (one corresponding to each gray shade) are adequate during a time slot. The signals Q_1 and Q_S are common to all the columns in the display. Hence a set of voltages corresponding to any specific time slot and polarity are connected to all the output stages in the driver using a common bus as shown in figure 6. The analog multiplexer for each output selects one out of the g voltages (figure 6) as compared to selecting one of the $(2g-2)$ voltages in the absence of the common selection block. This results in a saving of $(g-2)$ analog switches for each column in the display. Since the number of columns in a matrix display is generally large there is a significant reduction in the hardware complexity of the column driver. The common block consists of 4:1 analog multiplexers that are used to select the voltages on the bus in the column driver. These voltages are selected using the signals Q_1 and Q_S.

Table 3. Column voltages leading to simplification of the common selection block

Gray shade (g)	Data code	Column voltages for Scheme I		Column voltages when Schemes II and III are combined	
		First slot	Second slot	First slot	Second slot
-1	000	-1 (1)	-1 (1)	-1 (1)	1 (-1)
$-\left(\frac{5}{7}\right)$	001	-0.0144 (0.0144)	-1.4141 (1.4141)	-0.0144 (0.0144)	1.4141 (-1.4141)
$-\left(\frac{3}{7}\right)$	010	0.4750 (-0.4750)	-1.3320 (1.3320)	0.4750 (-0.4750)	1.3320 (-1.3320)
$-\left(\frac{1}{7}\right)$	011	0.8470 (-0.8470)	-1.1326 (1.1326)	0.8470 (-0.8470)	1.1326 (-1.1326)
$+\left(\frac{1}{7}\right)$	100	-0.8470 (0.8470)	1.1326 (-1.1326)	-0.8470 (0.8470)	-1.1326 (1.1326)
$+\left(\frac{3}{7}\right)$	101	-0.4750 (0.4750)	1.3320 (-1.3320)	-0.4750 (0.4750)	-1.3320 (1.3320)
$+\left(\frac{5}{7}\right)$	110	0.0144 (-0.0144)	1.4141 (-1.4141)	0.0144 (-0.0144)	-1.4141 (1.4141)
$+1$	111	1 (-1)	1 (-1)	1 (-1)	-1 (1)

The common selection block can be further simplified depending on the scheme used for amplitude modulation. In scheme I the row select voltage is same during the two time slots. Hence the order in which the voltages $(g+\sqrt{1-g^2})$ and $(-g+\sqrt{1-g^2})$ are applied to the column is not important. The order can be changed for half the number of gray shades. Table 3 lists the voltages applied to a column in scheme I when the order is changed for all the gray shades with

positive values. Voltages during polarity reversal are indicated in parenthesis. A voltage corresponding to a gray shade g in one time slot is same as that used for the gray shade $(-g)$ when the polarity is reversed (see Table 3). Hence a pair of symmetrically spaced gray shades can be represented using complementary binary patterns and the signal Q_I can be used control the complementing of data bits in the controlled inverter. The common block has a set of 2:1 analog multiplexers controlled by the signal Q_S instead of the 4:1 analog multiplexers. This reduction in hardware is marginal since there are only g common multiplexers in the driver. The schematic of the column driver with simplified common block is shown in figure 7. Since polarity is generally reversed after a frame or after selecting a few rows the data bits need to be loaded into the column driver only once over each row select time. The sign of the correction term $(\sqrt{1-g^2})$ is the same during both the time slots in schemes II and III. The sign of this term is thus independent of time slot and depends only on Q_I. Hence the voltage applied to the column for a gray shade g during one time slot will be same as the voltage to be applied for a gray shade $(-g)$ during the other time slot. The signal Q_S can be used to control the complementing of data bits. Each 4:1 analog multiplexers in the common block can be replaced with a 2:1 analog multiplexer controlled using the signal Q_I. Schemes II and III however require updating of data in the column driver during every time slot. This can be avoided if the driver provides the flexibility to internally complement the outputs of the shift register. In the absence of such a flexibility, an alternate method is obtained by combining schemes II and III. Scheme II can be used for negative gray shades i.e. for values of g in the range of –1 to 0 while scheme III can be used for positive gray levels ranging between 0 and 1 and vice versa. The column voltages necessary for displaying eight gray shades using the resulting scheme are listed in Table 3. Voltage applied to the column that corresponds to a gray shade g during a time slot is also used for gray shade $(-g)$ when polarity is reversed. This is similar to the symmetry seen in scheme I and hence the hardware structure indicated in figure 7 can be used for this scheme. The prototype for displaying eight gray shades uses a column driver board assembled using CD4051 (8:1 analog multiplexer) ICs for each column. A standard column driver SED1180F IC has been used for shifting and latching the data bits. This driver has a provision to shift in four bits of data simultaneously. Three bits of this data are used for each stage of the column driver. The outputs of the SED1180F are connected to the select inputs of 8:1 CMOS analog multiplexers. The display system and the controller details are discussed in the next section.

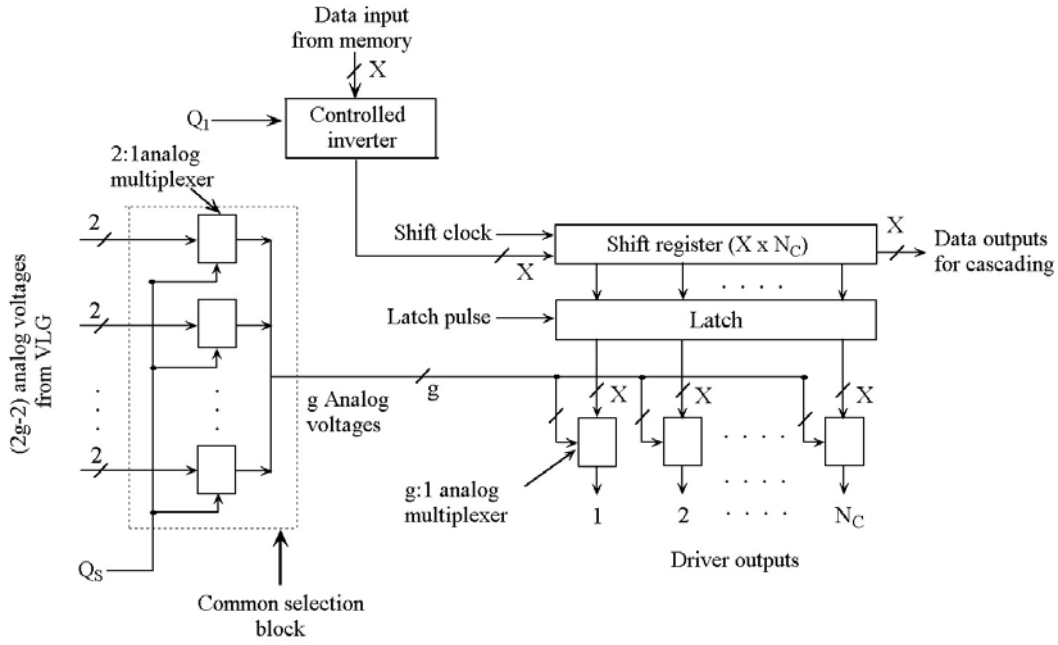

Figure 7. Schematic of the column driver with simplified column block

3.3. Controller

The block diagram of the display system to demonstrate the amplitude modulation technique is shown in figure 8. The image to be displayed is stored in memory. The controller generates addresses to access data corresponding to pixels in the first row of the matrix. The data bits are complemented when the polarity is reversed using a controlled inverter. The outputs of the controlled inverter are then shifted into the shift register in the column driver. While the column data is being shifted into the column driver, the row driver is cleared and a single logic '1' is shifted into the first stage of the shift register to select the first row. The contents of the shift registers in both row and column drivers are simultaneously loaded into latches in the respective drivers using a synchronous latch pulse generated by the controller. The voltages selected by the output of the latches are applied to the row and column electrodes of the matrix display during a row select time. While the voltages are applied to the display, gray shade data of the pixels in the second row are shifted into the shift register of the column driver. A zero is also shifted into the shift register of the row driver to ensure that the logic'1' shifted into the first stage moves to the second stage of the shift register. The data corresponding to the selection of the second row is latched next. The frequency of the shift clock used in the row driver is M times slower than that of the column driver. Here M is the number of columns in the display. In fact one edge of the latch pulse can also be used to shift in the contents of the row driver. The controller generates shift clocks of row and column drivers. Scanning a frame is complete when all the rows of the display have been selected once. This cycle is repeated and the display is refreshed fast enough (~50Hz) to avoid flicker. The controller also generates a signal P to invert the polarity of the row and column waveforms. This signal can be controlled through external inputs to invert polarity of the addressing waveforms after a frame or after selecting a few rows. We have developed CPLD based controller to demonstrate the technique. The controller provides flexibility to address matrix displays of varying size subject to a maximum of 256 rows and columns. The controller generates all the control signals for scanning the display and provides flexibility to reverse the polarity of the row and column waveforms at the end of a frame or after selecting a few rows. The controller has been implemented using 91 logic cells in a CPLD.

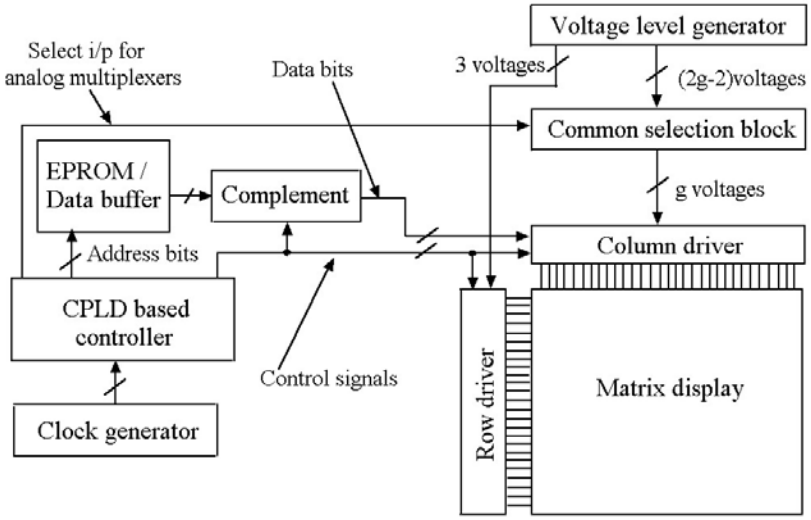

Figure 8. Block diagram of the display system

4. RESULTS AND CONCLUSIONS

A photograph of the prototype displaying eight gray shades using amplitude modulation is shown in figure. 9. Typical addressing waveforms that are applied to the display in the prototype are shown in figure 10. Plots of the rms voltage measured across the pixels for various values of supply voltage and eight gray shades are shown in figure 11. The selection ratio has also been plotted in the same figure. The measured value of selection ratio agrees with the theoretical value of 1.29 within ± 1.5%.

Figure 9. Photograph of the developed prototype

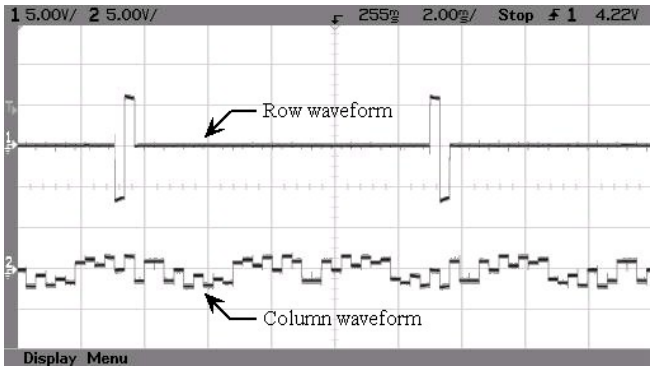

Figure 10. Typical addressing waveforms of amplitude modulation based on line-by-line addressing

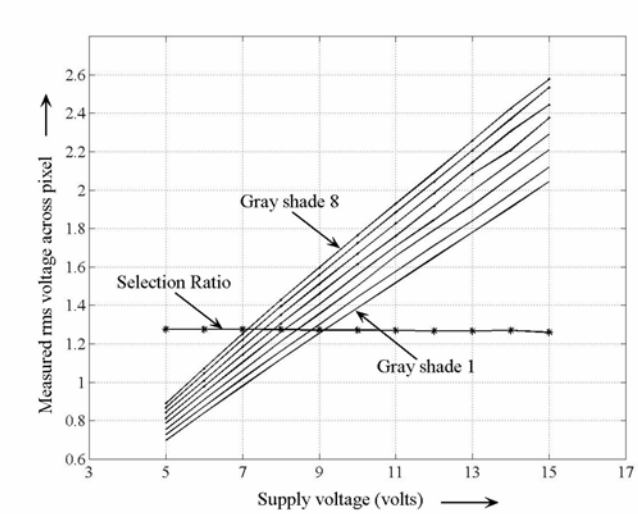

Figure 11. The measured rms voltage across a pixel for various gray shades

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