Two-Line Addressing Technique for SSFLC Displays

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Abstract

A new approach to speed up the addressing of Surface Stabilized Ferroelectric Liquid Crystal (SSFLC) displays by selecting two rows at a time is proposed. It combines the ideas from fast addressing modes of SSFLC with multiline selection of root-mean-square responding devices. The technique has been verified experimentally.

1 Background

Surface-Stabilized Ferroelectric Liquid Crystal (SSFLC) displays exhibit fast response times, wide viewing angle and flicker free operation. These advantages are due to linear coupling, in-plane switching and inherent bistability of ferroelectric LCDs. So far, line by line addressing is the only approach for driving passive SSFLC displays. As the display resolution increases a higher addressing speed is desirable. Hence, there has been a continuous effort to decrease the addressing time, both by developing faster liquid crystal materials and by speeding up the addressing. Fast addressing modes [1] have line addressing times that are shorter than the response time of the pixel. However, the distortion in driving waveforms due to the resistances and capacitances in the matrix panel limits the maximum refresh rate and hence the addressing speed. Increasing the addressing speed further by driving several lines at a time would help in driving large matrices at video rate as well as displaying grey shades using temporal dithering.

1.1 RMS responding devices

Multiline addressing techniques are popular for driving Super Twisted Nematic (STN) and Twisted Nematic (TN) liquid crystal displays [2,3]. Addressing times here are always shorter than the response times. Row waveforms in multiline techniques are a set of orthogonal functions [4]. These orthogonal functions are independent of the information on the display. Column waveforms, on the other hand, depend on the image and are orthogonal transform of the column data. Each pixel in a rms responding device is a demultiplexer. The multiplication and the integration necessary for demultiplexing are inherent in the rms response of the device. This approach is very similar to multiplexing and demultiplexing in communication engineering. **Figure 1** illustrates the waveforms of Improved Hybrid Addressing Technique (IHAT) in case of two rows driven simultaneously.

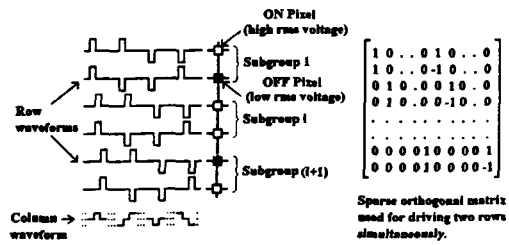


Fig. 1 Typical row (selection) and column (data) waveforms of a multiline addressing technique IHAT for nematic LCDs.

1.2 Ferroelectric devices

Fast addressing modes for the SSFLC devices are based on the fact that the dielectric torque ($\sim E^2$) counteracts the switching in its initial phase and accelerates it in the final phase of switching. The actual switching, although, is governed by the ferroelectric torque ($\sim E$). Control window of addressing (CW) is a small, but decisive, part of the switching process conducted by data independent write pulse and an AC field stemming from the cross-talk. The CW corresponds to the line addressing time and is much shorter than the actual switching time of a pixel.
The Split Writing scheme [5,6] shown in **Figure 2** represents a family of hold-back fast addressing schemes, where the dielectric torque in the initial stage of the

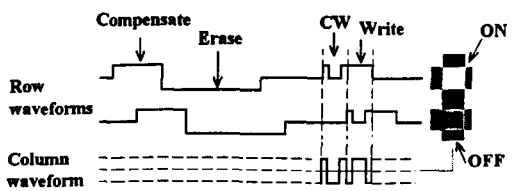


Fig. 2 An example of a fast addressing mode of a ferroelectric LCD – the Split Writing scheme.

switching process has the decisive role. The writing pulse is preceded by a long erase pulse. It ensures that the pixels are in a well-defined and repeatable state of the pixel prior to writing. The time gap between erasing and writing reduces the influence of the erase pulse and speeds up the switching. An additional compensation pulse, placed before the erase pulse, ensures the DC in the entire waveform is zero.

The Control Window (CW) consists of four time-slots. These are used to obtain either a high amplitude, high rms signal across the pixel, or a low amplitude, low rms voltage during the CW. In the first situation the switching is "held back" and the pixel remains in the erased state since the writing pulse is then too weak to move the liquid crystal molecules sufficiently far towards the opposite state. This movement is dominated by the ferroelectric torque. The switching is concluded by the dielectric torque stemming from the AC-field generated by the cross-talk.

2 Techniques

2.1 Basis for the new approach

The switching processes in rms responding devices and in ferroelectric devices are different. In the rms responding device amplitude of voltage across the pixel is important. The polarity of the voltage however is not important. In a ferroelectric display not only the amplitude of the pulse is important, but also its area and polarity. The polarity dependence, in particular, has made the multiline addressing techniques to appear unsuitable for driving ferroelectric devices.

The dielectric torque, being quadratic with the field, has no polarity dependence and plays a decisive role within the CW of fast addressing schemes. This fact encouraged us to control the strength of the dielectric torque within the CW of the SSFLC addressing scheme by using an approach similar to the multiline technique for rms devices. Two techniques for driving two rows at a time in ferroelectric LCDs are described in this paper.

2.2 The principle

The process of switching a pixel in these new techniques is very similar to that of switching in SW mode. The row waveforms of the new techniques also contain an erase pulse, write pulse and compensation pulse. Only the pulses in the control window are different. The background knowledge in driving rms responding LCDs is useful here. In rms responding LCDs the rms voltage across a pixel is controlled to be low or high using orthogonal functions. Two functions that are orthogonal to each other are necessary to select two rows simultaneously during the control window. There are several orthogonal functions that meet the requirement. One possible set of orthogonal function is:

[{-1,+1,+1,+1}, {+1,-1,+1,+1},
{+1,+1,-1,+1}, {+1,+1,+1,-1}].

Out of these, two orthogonal functions given below are used in the control window:

{+1,+1,-1,+1} and {+1,-1,+1,+1}.

Next, there are four possible combinations of states for two pixels in two selected rows of each column. They are:

[{OFF,OFF}, {OFF,ON}, {ON,OFF}, {ON,ON}].

Therefore a set of four data sequences is necessary corresponding to the four possible states of the pixel in a column. The corresponding data sequences are:

[{+1,-1,-1,+1}, {-1,+1,-1,+1},
{+1,-1,+1,-1}, {-1,+1,+1,-1}].

One could, however, use other orthogonal functions and corresponding data sequences in the Control Window to achieve the same result.

2.3 Addressing waveforms

Figure 3 shows possible pulse sequences for rows and columns within the Control Window that allow addressing two rows at a time. The row (selection) sequences are orthogonal to each other. There are four different data sequences for the column waveforms. They are the four possible combinations of pixel states in the selected rows. Each pixel experiences a voltage which is the difference between the voltages applied to its row and column electrodes. As can be seen in the figure the resulting pulse sequences for ON and OFF pixel differ significantly from each other. ON-sequences have lower rms value and, thus, produce a lower dielectric torque as compared to the OFF-sequences. Moreover, OFF pixels get a strong pulse of negative polarity. This, together with the higher rms voltage, forces the FLC molecules down and counteracts the switching.

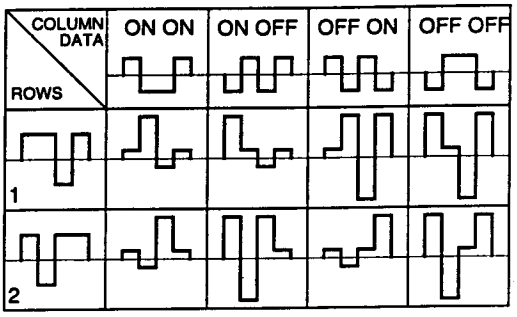


Fig. 3 Pulse sequences within the control window for simultaneous addressing of two rows in a SSFLC display.

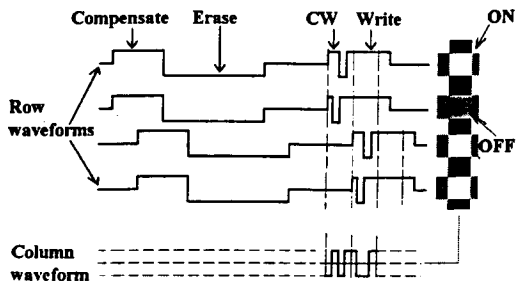
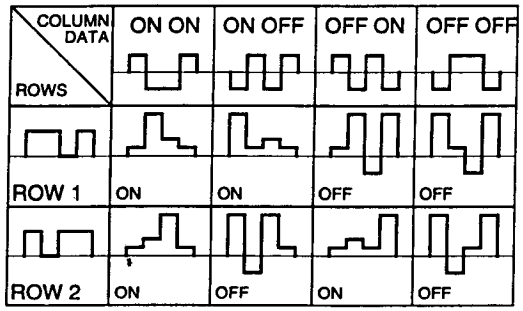


Fig. 4 Addressing waveforms for simultaneous driving of two rows in an SSFLC matrix display. The optical state of the two pixels in a column is defined by the data pulse sequence applied to the column during the control window (CW) and is independent of the column waveform outside the CW. The length of the write and erase pulses is determined by the electro-optic characteristics of the display, while the compensation pulse assures zero net DC in the waveform.



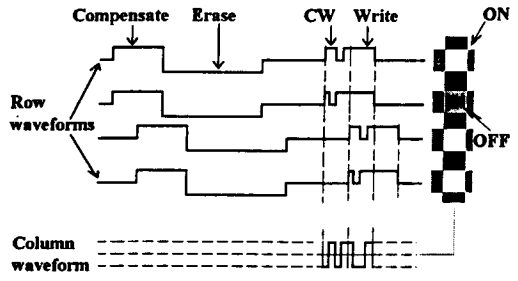


Fig. 5 Pulse sequences (above) and selection waveforms (below) for the 2-line SSFLC addressing technique with lower rms strength within the CW.

Typical addressing waveforms are shown in **Figure 4**. They resemble the waveforms of Split Writing scheme for addressing one row at a time. The control window covers the initial part of the switching process. Erase pulse preceding the CW ensures a well-defined and repeatable starting condition for switching irrespective of the previous state of the pixel. The row waveforms have here a negative pulse in the control window. **Figure 5** illustrates the technique where the negative pulse in the control window is replaced by zero voltage. The addressing waveforms are here same as those in **Figure 4** in all other aspects. Replacing the negative pulse during the CW in the row waveforms with the zero pulse reduces the strength of the rms voltage in the CW and is a tool to achieve a proper balance between the CW and the writing pulse.

3 Results

An example of the electro-optic response of a ferroelectric cell driven with waveforms corresponding to the technique illustrated in **Figure 3** and **Figure 4** is shown in **Figure 6**. Correspondingly, **Figure 7** presents the same cell driven by waveforms from **Figure 5**. The cell had the thickness of 1.9 μm and was filled with Felix 16/000 liquid crystal, that was aligned by buffing the PI-2610 polyimide coating on the inner surfaces of the cell. The cell was driven as thought it is a pixel in a matrix with 768 rows. The amplitude of row waveforms was 14 V and 11.5 V for the data waveforms in **Figure 6**, and 17 V and 12.5 V in **Figure 7**, respectively. The width of the control window was 128 μs. It is important to note that while voltage levels and the pulse widths are comparable to that of the Split Writing scheme (17 V and 10 V, respectively, in the same conditions), the display was scanned at the double rate of 64 μs per line on the average. In order to ensure that the switching is independent of the data outside the control window, the experiments were performed by randomly changing the image data preceding and following the control window.

4 Conclusions

A new approach to driving ferroelectric LCDs is proposed. Two sets of addressing waveforms for simultaneously selecting and driving pixels in two rows in a ferroelectric LCD are presented. This new approach could be used to increase the addressing speed or the matrix size without any change in frame refresh rate. This technique might also be useful to double the width of the control window for the same matrix size. Power consumption in a passive matrix LCD is mainly due to charging and discharging of the pixel capacitors. The width of the pulses in the drive waveform is doubled when two rows are simultaneously driven. Hence, for a given matrix size and panel refresh rate the power consumed to drive the matrix panel may be reduced using the new approach. Low voltages used in

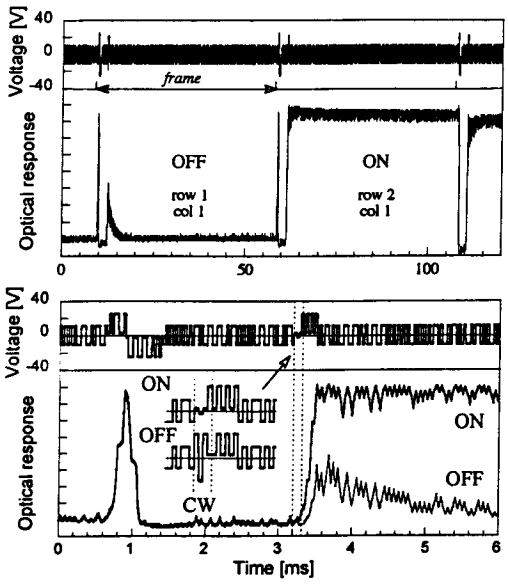


Fig. 6 An example of electro-optic response of one pixel in a 768-row SSFLC display driven 2 lines at a time with the line addressing time of 128 μs and using waveforms shown in **Figure 3** and **Figure 4**. The amplitude of the row waveform is 14 V and of the data pulses is 11.5 V. For the sake of comparison, the upper plot shows the response of the pixel 1 (row 1 and column 1) during one frame and then the response of pixel 2 (row 2 and column 1) during the same frame. In the lower plot the thicker trace shows switching ON pixel 2 (in the case of switching OFF pixel 1) and, correspondingly, the thinner trace shows switching OFF same pixel (in the case of switching ON pixel 1). Dotted vertical lines mark the position of the control window.

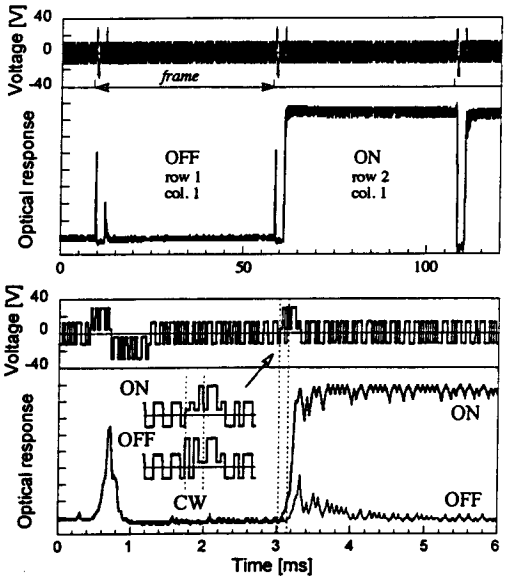


Fig. 7 Plots of a pixel electro-optic response, as described in **Figure 6**, obtained using the waveforms shown in **Figure 5**. The amplitude of selection pulses is 17 V, data 12.5 V and the width of the CW is 128 μs.

the addressing scheme are comparable to that of the fast addressing. The drive waveforms of the new technique are simple and the number of voltage levels (3 for rows and 2 for columns) is compatible with LCD drivers available today. There is scope to increase the addressing speed further by selecting more than two rows simultaneously.

Acknowledgments

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5 References

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