7.2: An Addressing Technique with Reduced Hardware Complexity

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Abstract

An addressing technique, with reduced hardware complexity of column drivers is presented. Choice of various parameters which will lead to a large reduction in hardware complexity will be discussed. A 50% reduction in hardware complexity is possible in some cases.

Introduction

Development of relatively fast responding Super Twisted Nematic Liquid Crystal Displays (STN-LCDs) with average response time of less than 50 ms has opened up many applications for these displays. New addressing techniques like the Improved Hybrid Addressing Technique(IHAT) [1], Sequency Addressing Technique(SAT) [2] and Active Addressing [3] are effective in suppressing frame response phenomenon [4] in fast responding LCDs. Hence the contrast ratio obtained by using these techniques is higher as compared to contrast ratio obtained by using the conventional addressing technique [5,6].

All these new addressing techniques are based on selecting more than one address line (row) simultaneously at a given instant of time. The number of voltage levels in the column (data) waveforms depends on the number of rows (L) that are selected simultaneously. The number of voltage levels is (L+1) when L rows are selected and the information displayed is bilevel (the pixel is driven either to ON state or OFF state). Hence the number of voltage levels increases with L.

There are two types of LCD column drivers available. In analog type drivers, the various voltage levels are stored in sample and hold circuits and have no limitation on number of voltage levels. In digital type drivers a number of voltage levels are multiplexed using analog multiplexers and the number of voltage levels is limited. Digital type of drivers are preferred since they consume less power. Hardware complexity of these drivers increases with the number of voltage levels. Hence it is preferable to reduce the number of voltage levels in the addressing waveforms. IHAT and SAT require less number of voltage levels as compared to active addressing, wherein all the rows are selected simultaneously. However, there is scope for reducing the number of voltage levels further in IHAT as discussed below.

Background

In IHAT the N rows in the matrix are divided in to (N/L) non intersecting subgroups each consisting of L rows. At a given instant of time one of the subgroups is selected with voltages corresponding to L bit row select pattern. This row select pattern corresponds to one of the 2^L binary numbers. The L bit row select pattern is compared with the L bit data to be displayed in the column using EX-OR gates. The column voltage is determined by counting the number of mismatches. The column voltage is proportional to (L-2i), wherein i is the number of mismatches. A cycle is complete when all the subgroups are selected with all the possible row select patterns once. This corresponds to selecting the subgroups with Rademacher functions, which are orthogonal.

Principle

The number of voltage levels(n) in IHAT can be reduced by assigning a common voltage to a group of mismatches instead of a separate voltage level for each mismatch. Except for the determination of column voltage, this technique is similar to IHAT. Restricting the voltage levels to a number less than (L+1) reduces the selection ratio (ratio of rms voltage across ON pixel to that across of OFF pixel). The selection ratio decreases as the number of voltage levels is decreased. The Hybrid Addressing Technique (HAT) [7] is the limiting case with just two voltage levels in the column waveform. The number of column voltages can be limited to any value between 2 and (L+1). A lower value is preferred to reduce the hardware complexity of column drivers. Hence restricting the number of voltage levels to 3 or 4 is of practical interest. Optimum grouping of mismatches with minimum degradation in selection ratio can be arrived at by exhaustive search of all possible groupings for each L as shown in the following analysis.

Analysis

In IHAT the number of mismatches ranges from 0 to L. The number of voltage levels is restricted to 3 by forming three groups covering the range of mismatches from 0 to L, when L is even as given below:

$$(0, 1, ..., m); (m+1, ..., L-m-1); (L-m, ..., L) \quad (1)$$

The column voltages are $-V_m$, 0 and $+V_m$ respectively for the voltage levels corresponding to these groupings of mismatches. This technique will be referred to as IHAT-S3 [8] since the number of voltage levels is restricted to three.

Similarly, the entire range of mismatches can be divided in to four groups when L is odd as shown below:

$$(0, 1, ., m1); (m1+1, ., \frac{L-1}{2}); (\frac{L+1}{2}, ., L-m1-1); (L-m1, ., L) \quad (2)$$

and the corresponding column voltages for these four groups are $-V_{m1}$, $-V_{m2}$, V_{m2} and V_{m1} respectively. This technique is referred to as IHAT-S4 [8], since the number of voltage levels is restricted to four. Only $2^{(L-1)}$ row select patterns will be considered here for the analysis, since rest of the row select patterns are complement of these row select patterns. Let the row select voltage be $-V_r$ for logic 0 and $+V_r$ for logic 1 in the row select patterns. The voltage across a pixel is the difference between the row and column voltages. At a given instant of time if the row and column voltages have the same polarity (sign) then this is favourable for OFF pixel and unfavourable for ON pixel. Similarly if the row and column voltages have opposite polarity then it is favourable for ON pixel and unfavourable for OFF pixel.

A pixel gets a favourable voltage during A_i time intervals and an unfavourable voltage during B_i time intervals, when C_i ($=A_i+B_i$) row select patterns with i mismatches are considered.

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$$A_i = \frac{(L-1)!}{i!(L-i-1)!} \tag{3}$$

and

$$B_i = \frac{i(L-1)!}{i!(L-i)!} \tag{4}$$

A pixel gets just column voltages across it during $(\frac{N}{L}-1)2^{(L-1)}$ time intervals since the row voltage is 0 when the rows are not selected.

IHAT-S3

The expressions for rms voltage across the ON and OFF pixel are given by the following expressions.

$$V_{ON}(rms) = \sqrt{\frac{S_1+S_2+S_3+S_4}{2^{(L-1)}\frac{N}{L}}} \tag{5}$$

and

$$V_{OFF}(rms) = \sqrt{\frac{S_5+S_6+S_3+S_4}{2^{(L-1)}\frac{N}{L}}} \tag{6}$$

where

$$S_1 = \sum_{i=0}^{m} A_i(V_r+V_m)^2 \tag{7}$$

$$S_2 = \sum_{i=0}^{m} B_i(V_r-V_m)^2 \tag{8}$$

$$S_3 = \left[2^{(L-1)} - \sum_{i=0}^{m}(A_i+B_i)\right] V_r^2 \tag{9}$$

$$S_4 = (\frac{N}{L}-1)\sum_{i=0}^{m}(A_i+B_i)V_m^2 \tag{10}$$

$$S_5 = \sum_{i=0}^{m} A_i(V_r-V_m)^2 \text{ and} \tag{11}$$

$$S_6 = \sum_{i=0}^{m} B_i(V_r+V_m)^2 \tag{12}$$

(13)

The selection ratio,the ratio of rms voltage across ON pixel to that across OFF pixel is maximum when the following condition is satisfied

$$\frac{V_r}{V_m} = \sqrt{\frac{C_m^* N}{2^{(L-1)}L}} \tag{14}$$

where

$$C_m^* = \sum_{i=0}^{m}(A_i+B_i) = \sum_{i=0}^{m} C_i \tag{15}$$

and the maximum selection ratio is given by the following expression

$$R = \sqrt{\left[\sqrt{\frac{C_m^* N}{L}} + \sqrt{\frac{A_m^2}{2^{(L-1)}}}\right] / \left[\sqrt{\frac{C_m^* N}{L}} - \sqrt{\frac{A_m^2}{2^{(L-1)}}}\right]} \tag{16}$$

where

$$A_m = \frac{(L-1)!}{m!(L-m-1)!} \tag{17}$$

This equation can also be expressed in the standard form shown below:

$$R = \sqrt{\frac{\sqrt{N_{eq}}+1}{\sqrt{N_{eq}}-1}} \tag{18}$$

Hence,

$$N_{eq} = \frac{2^{(L-1)}C_m^* N}{A_m^2 L} \tag{19}$$

where the Neq gives the number of lines that are to be multiplexed using the conventional technique to get the same selection ratio as given in equation 16.

IHAT-S4

The expressions for rms voltage across ON and OFF pixel are given below when L is an odd number

$$V_{ON}(rms) = \sqrt{\frac{s_1+s_2+s_3}{2^{(L-1)}\frac{N}{L}}} \tag{20}$$

$$V_{OFF}(rms) = \sqrt{\frac{s_4+s_5+s_3}{2^{(L-1)}\frac{N}{L}}} \tag{21}$$

where

$$s_1 = \sum_{i=0}^{m1} A_i(V_r+V_{m1})^2 + \sum_{i=(m1+1)}^{(\frac{L-1}{2})} A_i(V_r+V_{m2})^2 \tag{22}$$

$$s_2 = \sum_{i=0}^{m1} B_i(V_r-V_{m1})^2 + \sum_{i=(m1+1)}^{(\frac{L-1}{2})} B_i(V_r-V_{m2})^2 \tag{23}$$

$$s_3 = (\frac{N}{L}-1)\left[\sum_{i=0}^{m1}(A_i+B_i)V_{m1}^2 + \sum_{i=(m1+1)}^{(\frac{L-1}{2})}(A_i+B_i)V_{m2}^2\right] \tag{24}$$

$$s_4 = \sum_{i=0}^{m1} A_i(V_r-V_{m1})^2 + \sum_{i=(m1+1)}^{(\frac{L-1}{2})} A_i(V_r-V_{m2})^2 \tag{25}$$

and (26)

$$s_5 = \sum_{i=0}^{m1} B_i(V_r+V_{m1})^2 + \sum_{i=(m1+1)}^{(\frac{L-1}{2})} B_i(V_r+V_{m2})^2 \tag{27}$$

The selection ratio is a maximum when the following conditions are satisfied

$$V_{m2} = \frac{DG}{EF}V_{m1} \tag{28}$$

and

$$\frac{V_r}{V_{m1}} = \sqrt{\frac{DN}{2^{(L-1)}FL}} \times \sqrt{\frac{EF^2+DG^2}{EF}} \tag{29}$$

wherein

$$D = \sum_{i=0}^{m1}(A_i+B_i) = \sum_{i=0}^{m1} C_i \tag{30}$$

$$E = \sum_{i=(m1+1)}^{(\frac{L-1}{2})}(A_i+B_i) = \sum_{i=(m1+1)}^{(\frac{L-1}{2})} C_i \tag{31}$$

$$F = \sum_{i=0}^{m1}(A_i-B_i) \tag{32}$$

$$\text{and } G = \sum_{i=m1+1}^{(\frac{L-1}{2})}(A_i-B_i) \tag{33}$$

The maximum selection ratio is given below:

$$R = \sqrt{\left\{\sqrt{\frac{DN}{FL}} + \sqrt{\frac{EF^2 + DG^2}{2^{(L-1)}EF}}\right\} / \left\{\sqrt{\frac{DN}{FL}} - \sqrt{\frac{EF^2 + DG^2}{2^{(L-1)}EF}}\right\}} \quad (34)$$

The selection ratio can also be expressed in the standard form given in equation 18 and the resulting N_{eq} for IHAT-S4 is shown below:

$$N_{eq} = \frac{2^{(L-1)}DEN}{(EF^2 + DG^2)L} \quad (35)$$

Table 1

Various possible groupings of mismatches in IHAT-S3 – A comparison

L	Grouping of mismatches (i) for deciding the column voltages	Parameters A_m	Parameters C_m^*	Row-select voltage normalized to V_m	N_{eq}	Best grouping for each L
4	(0,1) (2) (3,4)	3	5	$\sqrt{\frac{5N}{32}}$	$\frac{10N}{9}$	*
4	(0) (1,2,3) (4)	1	1	$\sqrt{\frac{N}{32}}$	2N	
6	(0,1,2)(3)(4,5,6)	10	22	$\sqrt{\frac{11N}{96}}$	$\frac{88N}{75}$	*
6	(0,1)(2,3,4)(5,6)	5	7	$\sqrt{\frac{7N}{192}}$	$\frac{112N}{75}$	
6	(0)(1,2,3,4,5)(6)	1	1	$\sqrt{\frac{N}{192}}$	$\frac{32N}{6}$	

Table 2

IHAT-S3 (with L=6) vs. IAPT (conventional technique) – A comparison

N	Selection ratio (R) of IHAT-S3	Selection ratio (R) of IAPT	N_{eq} of IHAT-S3
6	1.487	1.543	7.04
12	1.314	1.346	14.08
18	1.247	1.272	21.12
24	1.210	1.230	28.16
30	1.186	1.203	35.20
36	1.168	1.183	42.24
42	1.154	1.168	49.28
48	1.143	1.156	56.32
54	1.135	1.147	63.36
60	1.127	1.139	70.40
90	1.103	1.112	105.60
120	1.088	1.096	140.80
150	1.078	1.085	176.00
300	1.055	1.060	352.00

Results

Table 1 gives the various possible grouping of mismatches for L=4 and 6 in IHAT-S3. The best grouping is indicated by asterisk and this gives a selection ratio close to the value obtained by using conventional technique. Table 2 gives the comparison between IAPT and IHAT-S3 with L=6.

Table 3 gives the possible groupings of mismatches for L=5 and 7. Table 4 gives the comparison of selection ratio of IHAT-S4 for L=7 with that of conventional technique. The selection ratio is very close to the conventional technique and there is no significant change in the contrast ratio of the display.

Table 3

Various possible groupings of mismatches in IHAT-S4 – A comparison

L	Grouping of mismatches (i) for deciding the column voltage	Row-select voltage $\lvert V_r \rvert$	Ratio of column voltages $\lvert V_{m2}/V_{m1} \rvert$	N_{eq}	Best grouping for each L
5	(0,1)(2)(3)(4,5)	$\sqrt{\frac{69N}{800}}$	$\frac{3}{10}$	$\frac{24N}{23}$	*
5	(0)(1,2)(3,4)(5)	$\sqrt{\frac{N}{30}}$	$\frac{1}{3}$	$\frac{6N}{5}$	
7	(0,1,2)(3)(4)(5,6,7)	$\sqrt{\frac{1247N}{17640}}$	$\frac{29}{105}$	$\frac{232N}{215}$	*
7	(0,1)(2,3)(4,5)(6,7)	$\sqrt{\frac{2N}{63}}$	$\frac{1}{3}$	$\frac{8N}{7}$	
7	(0)(1,2,3)(4,5,6)(7)	$\sqrt{\frac{53N}{3528}}$	$\frac{19}{63}$	$\frac{72N}{53}$	

Table 4

IHAT-S4 (with L=7) vs. IAPT (conventional technique) – A comparison

N	Selection ratio (R) of IHAT-S4	Selection ratio (R) of IAPT	N_{eq} of IHAT-S4
7	1.464	1.488	7.553
14	1.3010	1.315	15.107
21	1.238	1.248	22.660
28	1.202	1.211	30.214
35	1.178	1.186	37.767
42	1.161	1.168	45.321
49	1.148	1.155	52.874
56	1.138	1.144	60.428
63	1.130	1.135	67.981
70	1.123	1.128	75.535
140	1.0850	1.0884	151.07
210	1.0688	1.0716	226.60
280	1.0593	1.0617	302.14
350	1.0529	1.0550	377.67
420	1.0481	1.0500	453.21
490	1.0445	1.0462	528.74
560	1.0415	1.0432	604.28
630	1.0391	1.0407	679.81
700	1.0371	1.0385	755.35
1050	1.0302	1.0314	1133.02
1400	1.0261	1.0271	1510.70

L=7 is specially attractive for practical applications. There is a 50% reduction in the number of voltage levels (4 levels as compared to 8 levels in IHAT) and nearly 50% reduction in the hardware complexity of column drivers. Typical column drivers with M outputs consist of M bit shift register(s) to serially shift in the data, M bit latch to load the data in parallel and M(L+1) analog switches to select any one of (L+1) voltages depending on the data loaded into the latch. The IHAT will have 3 bit data to select one of the eight voltage levels when L is 7. Hence, the shift register and latch for each output should store 3 bits. However, only 2 bits of data need to be stored in the shift register and latch when the number of voltage levels is restricted to 4. Hence the number of flip flops in shift registers and latches is reduced by a factor 1/3 as compared to IHAT. This hardware reduction is in addition to the reduction of analog switches to select one of the voltage levels from 8 to 4, for each column output. Hence use of this technique will lead to cost reduction of the column drivers since more devices can be accommodated in a given silicon area and reduced power consumption.

Conclusion

A method for reducing the number of voltage levels in the column waveform is presented. This in turn reduces the hardware complexity of column drivers and also reduces the power consumption in the column drivers. Good brightness uniformity and low supply voltage requirement which are the main advantages of IHAT is retained even after this reduction in the number of voltage levels. IHAT-S4 with L=7 is very useful for displays since the complexity of hardware can be reduced by 50% and L=7 is sufficient to suppress the frame response in fast responding LCDs [2].

References

1. T.N.Ruckmongathan, *A genereralised addressing technique for rms responding matrix LCDs, Proc. IDRC*, pp.80-85, 1988.
2. T.N.Ruckmongathan, T. Kuwata, T.Ohnishi, S.Ihara, H. Koh and Y.Nakagawa, *A new addressing technique for fast responding STN LCDs, Proc. Twelfth International Display Research Conf. - Japan Display'92*, pp. 65-68, 1992.
3. T.J.Scheffer and B.Clifton, *Active addressing method for high contrast video rate STN displays, 1992 SID Digest and Technical Papers*, XXIII,m pp.228-231, 1992.
4. Y.Kaneko, K.Okada, E.Tajima, K.Tsuruma, H.Kurauchi, A.Suzuki, T.Ishida, M.Okamoto, S.Togashi and T.Aoyama, *Full-color STN video LCDs, Proc. Tenth International Display Research Conf. - Eurodisplay'90*, pp.100-103, 1990
5. P.M.Alt and P.Pleshko, *Scanning limitations of liquid crystal display, IEEE Trans. ED*, Vol. ED21, pp. 146-155, 1974.
6. H.Kawakami et. al. *Matrix addressing technology of twisted nematic liquid crystal display, SID-IEEE Record of Biennial Display Conf.*, pp.50-52, 1976
7. T.N.Ruckmongathan and N.V.Madhusudana, *New addressing techniques for multiplexed liquid crystal displays, Proc. of SID*, Vol.24/3, pp.259-262, 1983
8. T.N.Ruckmongathan, . *Some new addressing techniques for rms responding matrix LCDs, A Thesis submitted to Electrical Communication Engineering, Indian Institute of Science, Bangalore*, 1988