NEW ADDRESSING TECHNIQUES FOR MULTIPLEXED LIQUID CRYSTAL DISPLAYS

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Abstract — A binary addressing technique (BAT) for multiplexing liquid crystal displays (LCDs) is described. It requires addressing waveforms with only two voltage levels, and leads to a naturally dc-free operation. The method is suitable only for small matrices ($N<9$). We propose a hybrid addressing technique (HAT) which combines the features of both BAT and the familiar Alt and Pleshko technique (APT). It is shown that HAT can be used for large matrices. The three techniques are compared.

I. INTRODUCTION

The Alt and Pleshko technique (APT)[1] is widely used in multiplexing liquid crystal displays (LCDs). An alternative technique which will be referred to as the binary addressing technique (BAT)[2] was proposed recently (see, also, Ref. 3). In this technique all the N rows to be multiplexed are selected simultaneously with voltage levels $\pm V_r$ corresponding to 1 or 0, so that the voltage pattern applied to the rows corresponds to an N digit binary number. This is compared with the binary pattern to be displayed in a given column and the column voltage is decided as $+ V_c$ or $- V_c$ such that a majority of rows get a favorable voltage. Now, the row address pattern is changed to a new N-digit binary number and the process is continued until all the 2^N possible combinations are exhausted, and the cycle is then repeated. The principal merits of the technique are (a) it requires a single relatively low power supply and (b) a natural dc-free operation. To demonstrate this technique, we constructed a 16-segment alphanumeric display[2] which was treated as a 4 × 4 matrix. Since the binary addressing technique can be used only for an odd number of rows,[2] N was chosen to be 5. The details are given in Ref. 2 along with some photographs of the display, which had an acceptable contrast. However, BAT is not suitable if $N>9$ or 11, since the number of time intervals to complete a cycle takes a very high value.

In this paper, we will briefly review BAT and propose a combination of BAT and APT. It will be called the hybrid addressing technique (HAT) and can be used for relatively large values of N. In this technique the total N rows to be multiplexed are divided into N/n non-intersecting subsets, each consisting of n rows. At a given instant of time one of these subsets is subject to BAT while the rest of the rows are at ground potential. A cycle is complete when all the subsets are subjected to binary addressing. The features of the three techniques are compared in Table I.

II. THE BINARY ADDRESSING TECHNIQUE

In a multiplexed display with n rows, if the information to be displayed is bilevel (i.e., the segment is either ON or OFF), the pattern to be displayed in a column can be represented by $d_1, d_2, \ldots, d_n$; $d_i = 0$ or 1. In this addressing technique, the rows are applied with voltages corresponding to an n bit pattern $a_1, a_2, \ldots, a_n$; $a_i = 0$ or 1. A bit-by-bit comparison is made between the two patterns, and the number of anticoincidences (mismatches) is counted. Mathematically, we have to find s where

$$s = \sum_{i=1}^{n} a_i \oplus d_i$$

where $\oplus$ is an exclusive OR operation. The column voltage is decided by a majority decision, i.e., if $s>n/2$, the column voltage will correspond to 1, otherwise to 0. This reduces the number of errors in that column. Now, $a_1, a_2, \ldots, a_n$ is changed to a new binary pattern and the procedure is repeated. A cycle is complete when all the n-bit binary combinations are exhausted, i.e., after 2^n intervals. Since a majority decision is needed in this technique, n has to be odd.

The voltages across an element with different conditions during an interval are given in Table II.

Now it is required to calculate the number of times an element gets the correct voltage during one cycle. We will consider only 2^{n-1} intervals such that they are com-

TABLE I. Comparison of the features of the three techniques.

	APT	BAT	HAT
V_{ON}/V_{OFF}	High	Low	Intermediate
Address duty factor	$1/N$	$P/2^{n-1}$	$nP/2^{n-1}N$
V_r/V_c	$\sqrt{N}$	1	$\sqrt{N/n}$
Power supply voltage	High	Low	Intermediate
Number of voltage levels across an element	4	3	6
Number of intervals to complete a cycle	N	2^n	$2^n(N/n)$

TABLE II. Voltage across an element with different conditions during an interval.

Column	Row	
Logic level/voltage	logic level/voltage	
	$0/-V_c$	$1/+V_c$
$0/-V_r$	$-(V_r-V_c)$ OFF	$-(V_r+V_c)$ ON
$1/+V_r$	$+(V_r+V_c)$ ON	$+(V_r-V_c)$ OFF

ABLE III. Values of P and V_{ON}/V_{OFF} for various values of n.

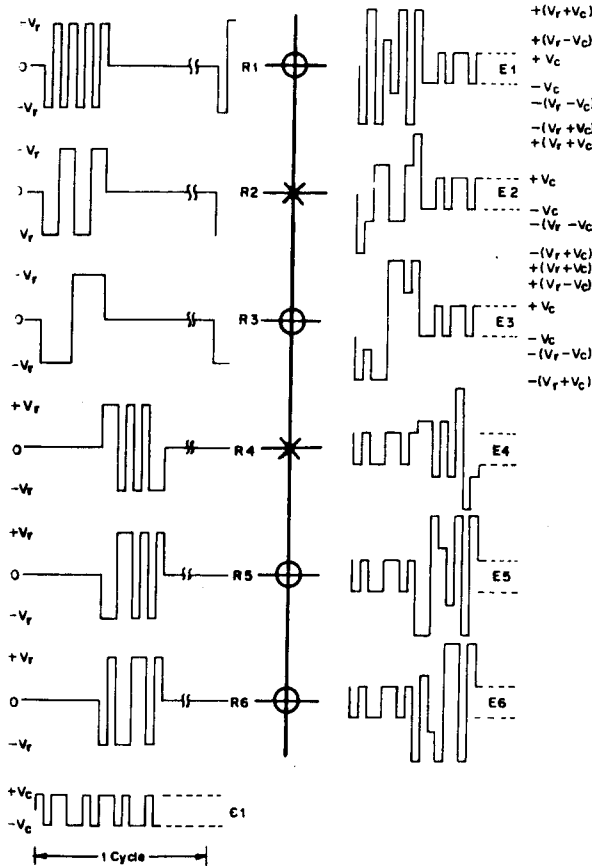| o. of rows ultiplexed	P	V_{ON}/V_{OFF} BAT	V_{ON}/V_{OFF} APT
= 3	3	1.732	1.932
= 5	11	1.483	1.618
= 7	42	1.382	1.488
= 9	163	1.324	1.414

IG. 1. Representative Waveforms for HAT R1–R6 are the waveforms
pplied to rows 1–6, respectively, and C1 is the waveform applied to a
olumn. Note that R3–R1 are applied with the binary pattern sequence
00, 001, 010, 011, 100, 101, 110, and 111, whereas R6–R4 are applied
vith the binary pattern sequence 001, 101, 010, 011, 100, 111, 000, and
10. The sequence in which the 2^n combinations are applied to the rows
Joes not alter the rms voltage across an element, but has an effect on the
'requency spectrum of the waveform across the element.

olementary to the remaining 2^{n-1} intervals. As shown in
Ref. (2), the number of times (say P) an element gets the
orrect voltage is given by

$$P = \sum_{m=0}^{\frac{n-1}{2}} \frac{(n-1)!}{m!(n-1-m)!} .$$

The expressions for V_{ON} and V_{OFF} can be written as

follows:

$$V_{ON} = \left(\frac{2P(V_r + V_c)^2 + 2(2^{r-1} - P)(V_r - V_c)^2}{2^n} \right)^{1/2} ,$$

$$V_{OFF} = \left(\frac{2P(V_r - V_c)^2 + 2(2^{n-1} - P)(V_r + V_c)^2}{2^n} \right)^{1/2} .$$

The V_{ON}/V_{OFF} ratio is optimized for $V_r/V_c = 1$. Table III
shows the values of P, and V_{ON}/V_{OFF} for various values of
n.

III. THE HYBRID ADDRESSING TECHNIQUE

Here we use the binary addressing technique to address a
subset consisting of n rows of the total N rows, while the
rest of the $N-n$ rows are at ground potential. After
completion of 2^n intervals, a different subset with n rows is
scanned with BAT. The rows to be scanned by BAT can be
represented by $ni+1$, $ni+2$, . . . $ni+n$, where i takes the
values 0 to $[(N/n)-1]$.

Representative wave forms for the hybrid addressing
technique are given in Fig. 1.

The rms voltage across the ON and OFF elements are
given by

$$V_{ON} =$$

$$\left(\frac{2P(V_r + V_c)^2 + 2(2^{n-1} - P)(V_r - V_c)^2 + 2^n[(N/n)-1]V_c^2}{2^n(N/n)} \right)^{1/2} \quad (1)$$

and

$$V_{OFF} =$$

$$\left(\frac{2P(V_r - V_c)^2 + 2(2^{n-1} - P)(V_r + V_c)^2 + 2^n[(N/n)-1]V_c^2}{2^n(N/n)} \right)^{1/2} . \quad (2)$$

The V_{ON}/V_{OFF} ratio is optimized for $V_r/V_c = \sqrt{N/n}$.
Substituting this into Eqs. (1) and (2), we get

$$V_{ON} = \left(\frac{2^n(N/n) + (N/n)^{1/2}(4P - 2^n)}{2^{n-1}(N/n)} \right)^{1/2} ,$$

$$V_{OFF} = \left(\frac{2^n(N/n) - (N/n)^{1/2}(4P - 2^n)}{2^{n-1}(N/n)} \right)^{1/2} ,$$

$$\frac{V_{ON}}{V_{OFF}} = \left(\frac{(N/n)^{1/2}2^n + (4P - 2^n)}{(N/n)^{1/2}2^n - (4P - 2^n)} \right)^{1/2} = \sqrt{K}. \quad (3)$$

Figure 2 gives a comparison of the V_{ON}/V_{OFF} ratio ob-
tained for different values of N in both APT and HAT.

The supply voltage needed to address a multiplexed
display using APT has been shown to be $(V_r + V_c)$ by
Kawakami et al.[4] This can be achieved by the synthesis of
suitable waveforms applied to both the rows and columns.

$$V_r + V_c = \frac{\sqrt{N}+1}{\sqrt{2}[1-(1/\sqrt{N})]} V_{th}, \quad (4)$$

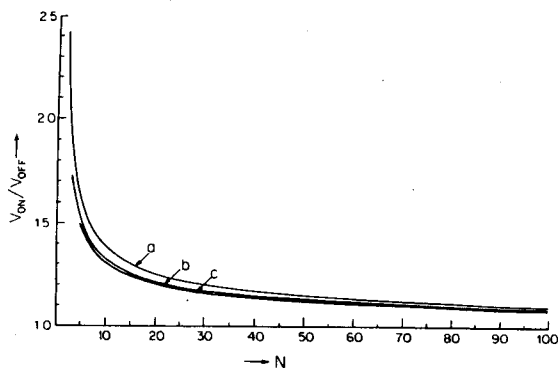where V_{th} is the threshold voltage of the liquid crystal. In

FIG. 2. Plot of V_{ON}/V_{OFF} vs. N for (a) ALT, Pleshko (b) HAT with n = 3, and (c) HAT technique with n = 5.

the case of HAT, it does not appear to be possible to rearrange the row and column address waveforms to reduce the power supply requirement to less than $2V_r$, which is given by the following expression:

$$2V_r = \left(\frac{2(N/n)}{1 - [(4P - 2^n)/2^n (N/n)^{1/2}]} \right)^{1/2} V_{th}. \qquad (5)$$

However, APT gives a higher contrast ratio than HAT. In order to make a proper comparison between the power supply requirements in the two cases, we reduce the V_{ON}/V_{OFF} ratio given by APT to the optimum value given by HAT, i.e.,

$$\left(\frac{V_{ON}}{V_{OFF}} \right)^2 = K = \frac{(x+1)^2 + (N-1)}{(x-1)^2 + (N-1)}, \qquad (6)$$

where K is given by Eq. (3) and $x = V_r/V_c$ of APT which would give the same contrast ratio as HAT. This leads to the following expression for x:

$$x = \frac{(K+1) - [(K+1)^2 - (K-1)^2 N]^{1/2}}{(K-1)}.$$

Using this, we get the power supply voltage required for the degraded APT as

$$(V_r + V_c) = \left(\frac{N}{(x-1)^2 + (N-1)} \right)^{1/2} (x+1)V_{th}. \qquad (7)$$

IV. RESULTS

The salient features of the three techniques are summarized in Table I. We give a comparison of the power supply requirements given by HAT [Eq. (4)] and the degraded APT [Eq. (7)] in Table IV for various values of N and n. If $n = N$, we recover BAT. As can be seen from Table I, the power supply requirement of HAT is lower than that of the degraded APT if n is large. For any n, the advantage decreases as N increases.

We constructed a twisted nematic (TN) cell to make an experimental comparison between the two techniques. The liquid crystal used had a threshold voltage $V_{th} = 1.45$ V and a steepness $\gamma \; [= (V_{50} - V_{10})/V_{10} \times 100] \approx 17\%$. The percentage transmission as a function of the power supply voltage ($= V_r + V_c$) when the cell is addressed as if it is an

TABLE IV. Comparison of the power supply requirements given by HAT and the APT for various values of N and n.

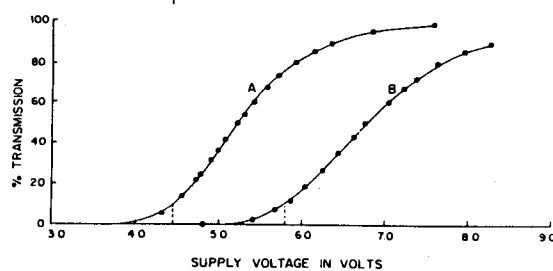| N	n	Supply voltage of HAT $2V_r$ ($\times V_{th}$)	V_r/V_c of APT for same contrast as HAT	APT supply voltage $V_r + V_c$ ($\times V_{th}$)	$\dfrac{V\,supply_{HAT}}{V\,supply_{APT}} \times 100$
3	3	2.0 V	1.0	2.449 V	81.65
6	3	2.487 V	1.415	2.601 V	95.62
5	5	1.789 V	1.214	2.461 V	72.69
10	5	2.333 V	1.718	2.786 V	83.73
15	5	2.767 V	2.105	3.082 V	89.77
20	5	3.138 V	2.432	3.345 V	93.80
25	5	3.466 V	2.714	3.578 V	96.87
30	5	3.764 V	2.981	3.8 V	99.05
7	7	1.706 V	1.400	2.558 V	66.69
14	7	2.266 V	1.977	2.982 V	76.00
21	7	2.706 V	2.422	3.342 V	80.97
28	7	3.079 V	2.794	3.652 V	84.42
35	7	3.409 V	3.132	3.937 V	86.60

FIG. 3. Plot of transmission characteristics of a TN LC cell addressed by APT as modified in Ref. 4 for N = 15. A and B are the selected and nonselected elements, respectively.
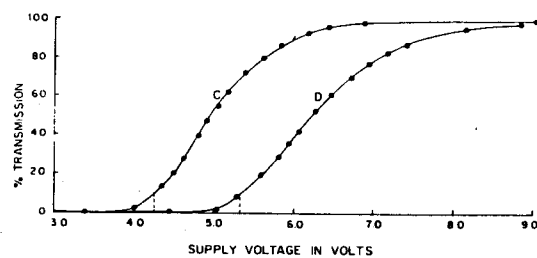

FIG. 4. Plot of transmission characteristics of a TN LC cell addressed by HAT with N = 15 and n = 3. C and D are selected and nonselected elements, respectively.

ON and an OFF element of APT with N = 15 are shown in Fig. 3 as curves A and B, respectively. The same cell was addressed using HAT with n = 3 and N = 15. The corresponding percentage transmission coefficients as functions of the power supply voltage ($= 2V_r$) are shown in Fig. 4.

In Fig. 5, we show the transmission curves for APT which is degraded to give the same V_{ON}/V_{OFF} as HAT with N = 15 and n = 5. These can be compared with the transmission curves for HAT shown in Fig. 6. It is clear that the power supply voltage required by HAT is lower than that for APT as expected from Table IV. The experimental values which are accurate to $\sim 2\%$ agree with the calculated values given in Table IV.
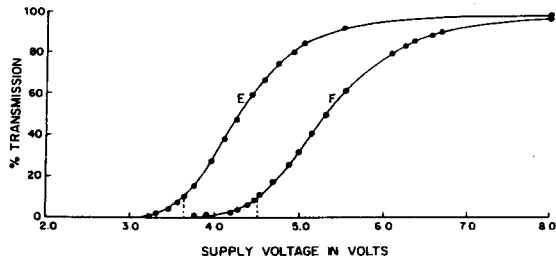
FIG. 5. Plot of transmission characteristics of a TN LC cell addressed by a degraded APT [see Eq. (7)] for $N = 15$ which has the same V_{ON}/V_{OFF} ratio as HAT with $N = 15$ and $n = 5$. E and F are selected and nonselected elements, respectively.
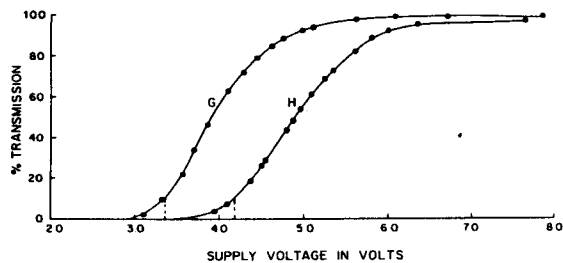

FIG. 6. Plot of transmission characteristics of a TN cell addressed by HAT with $N = 15$ and $n = 5$. G and H are selected and nonselected elements, respectively.

V. CONCLUSIONS

A binary addressing technique, which requires a single supply voltage has been described. It depends on scanning the N-row matrix, with the binary voltages corresponding to the 2^N possible N-digit binary numbers. It is useful for small matrices ($N<9$ or 11). A hybrid technique which combines BAT with APT in which the matrix is addressed line by line has been proposed to overcome this limitation. In many cases, this results in some reduction in the power supply requirement compared to the APT scheme. We have illustrated this point by studying the transmission characteristics of both the ON and OFF elements of a TN cell while being addressed by HAT and APT.

ACKNOWLEDGEMENT

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