Ultra Wide band and High Dynamic range Low Noise Amplifier for Low Frequency applications in Radio Astronomy

A Project Report

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for the degree of
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by
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Abstract

In low frequency astronomy (< 300 MHz), antennas used to collect radiation from the sky, function like short dipoles ($l \ll \lambda/2$) over an appreciable range of wavelengths. Since the short dipoles do not possess appreciable impedance matched bandwidth for 50 Ω systems, coupling of sky radiation to amplifiers connected to the output of antennas will be highly inefficient over a substantial portion of the bandwidth. This in general leads to degradation in the Signal to Noise ratio. This can be compensated by minimizing the noise contribution by the receiver system and ensuring that the sky noise dominates the system temperature despite the inefficiency of coupling. This necessitates the development of a low noise amplifiers at low frequencies. Since the low frequency environment is highly dominated by the strong manmade interference signals, the amplifier should also have a very high dynamic range.

In this project an improved design of LNA to achieve low noise, broadband and high dynamic range operation is examined to develop an effective front–end for a new low frequency telescope being designed by Raman Research Institute (RRI), operating in the frequency range of 30–300 MHz. Microwave Integrated Circuit (MIC) approach has been followed in the design of LNA instead of Monolithic Microwave Integrated circuit (MMIC) technique, since the latter is impractical for implementation in the laboratory and is economically viable for small number of units required as a part of this activity.

As a part of this development program we have designed and tested a low noise

HEMT amplifier (Noise Temperature = 50 K) with wide bandwidth (30–300 MHz) using thermal noise canceling technique. In the second phase we are attempting to increase the dynamic range performance using Post-distortion technique. In the third phase we will develop a differential amplifier with the same characteristics which can be directly connected to the balanced line from a short dipole.

Acknowledgements

I would like to thank my internal adviser, Dr. K J Vinoy for the patient guidance and insight he provided as I learned from each of many rewarding challenges I encountered during my graduate career at IISc. Researching under his expert supervision has taught me many invaluable lessons about the pursuit of academic research. I also thank him for giving me an opportunity to work in Raman Research Institute (RRI).

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Lastly, and most importantly, I wish to thank my family for providing a loving environment for me. My parents have been an inspiration throughout my life, I dedicate this thesis to them.

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Chapter 1

Introduction

A radio telescope forms a major tool for the investigation of several astrophysical phenomena in radio astronomy. The investigation is normally carried out over a range of frequencies starting from few tens of MHz till several hundred GHz. The frequency of observation is mainly determined by the phenomenon being investigated.

The Low noise amplifier plays an important role in any front end receiver of radio telescope [1]. The main purpose of having an amplifier is to increase the signal level collected by the antenna, without seriously affecting the SNR.

1.1 Requirement of LNA for low frequency radio astronomy

Nowadays in Low Frequency Astronomy ($<$ 300 MHz) short dipoles are used as feeds to collect radiation from the sky. Short dipoles have the property that they couple lesser and lesser sky radiation (T_{sky}) into the front end Receiver. (T_{sky}) forms one of the components of system temperature, (T_{sys}), which represents the total noise power available at the low noise amplifier input.Other components of the system temperature come from ground, and receiver etc. Hence (T_{sys}) can be

represented as

$$T_{sys} = T_{sky} + T_{gnd} + T_{LNA} \tag{1.1}$$

In order to ensure sky noise dominates the SNR, the noise contribution from the amplifier following the antenna must be minimized as much as possible. This requires the development of an amplifier at low frequencies with a low noise figure.

For studying the astrophysical phenomena occurring at different frequencies, the sky observation is normally carried out at multiple wavelengths. So, the receiver (mainly LNA) is normally built to have as broadband character as possible.

1.2 LNA specifications

Raman Research Institute (RRI) has taken up the project of building a low frequency radio telescope operating at a frequency range of 30-300 MHz. The LNA being developed will be used in the front end receiver of the radio telescope.

In general the Low noise amplifier is designed to have sufficient gain ($\sim$ 20–25 dB) in order to minimize the noise contribution from the subsequent stages in the RF chain. Good input return loss of -10 to -15 dB is always preferable in order to maximize the input power transfer.

The sky contribution at 50 MHz has been estimated to be about 5000 K. Assuming a coupling efficiency of 10 % for the antenna, an amplifier having 50 K as its noise temperature is desired to maintain a minimum SNR ($\sim T_{sky}/T_{LNA}$) of about 10.

The radio interfering signal levels in the frequency range of our interest is of the order of 0 dBm. So, the amplifier working in this environment is expected to be be capable of working linearly for as large input as possible preferably 0 dBm.

The required specifications of the LNA to be designed is as shown in the Table 1.1.

Parameter	Target value
Frequency range	30-300 MHz
Noise Figure	50 K
Gain	$\geq$ 25 dB
Maximum input power	0 dBm
Input Return loss	$\leq$ -10 dB

Table 1.1: specifications of the LNA

1.3 Organization of the report

The report is organized as follows. Chapter 2 describes the literature survey undertaken before beginning the design. It gives a brief comparison of different type of microwave transistors, talks about the different broad band techniques followed by low noise techniques and different methods to improve linearity of the amplifier and gives the advantages and disadvantages of each of them. Chapter 3 deals with the circuit topology chosen for the project and shows the design calculations along with the simulation results. Chapter 4 elaborates on the constructional details of the LNA along with the comparison of the simulated and measured results. Chapter 5 concludes the report with a summary and also points out possible future developments.

Chapter 2

Literature Survey

Survey was done to begin with on various devices available in the market for building a low noise amplifier. Their electrical characteristics like mobility, thermal conductivity, thermal coefficient etc were looked into, to find out their suitability to our application. Then, various techniques available for broad band operation of a low noise amplifier were studied along with the limitation that each one of them had with regard to either noise contribution or broad band nature or complexity in the circuit. Finally, different linearizing techniques currently being adopted for achieving high dynamic range were also looked into in greater detail.

In the sections following, a brief description of various aspects mentioned above is presented.

2.1 Semiconductor materials and their characteristics

For high-speed applications(few GHz), higher mobility is required. So GaAs devices are selected in general, because of their large mobility (9200 $cm^2/V-sec$) when compared to silicon whose mobility is 1450 $cm^2/V-sec$. This primary benefit comes from its lower effective mass. Along with this major advantage, it also has certain

disadvantages like non-availability, lower thermal conductivity and high thermal coefficient of expansion etc. Since the low field mobility determines basically the RF noise characteristics, GaAs is generally preferred than Silicon in low noise applications. On the other hand, silicon is better in high field mobility characteristics. So, for high frequency applications where larger electric field is involved, Silicon is preferred over GaAs.

2.2 Microwave transistors and their characteristics

Several microwave devices are available in the market and some of the most commonly used are silicon Bipolar junction transistors (BJT), GaAs Metal-semiconductor field effect transistors (MESFET), Hetero junction bipolar transistors (HBT) and High electron mobility transistors (HEMT). Various figures-of-merits are used to evaluate and compare transistor characteristics including maximum available gain, Gain-Bandwidth product (f_T), maximum frequency of oscillations (f_{max}), minimum noise figure (F_{min}). The following section gives an overview of various device technologies described above and compare them for their advantages and disadvantages.

2.2.1 Bipolar junction transistor (BJT)

Silicon bipolar transistor is a current driven device in which the base current modulates the collector current of the transistor. The high frequency equivalent circuit of a BJT is shown in the figure 2.1.

The figure of merits for the BJT can be shown as [2]-[4]:

Gain–Bandwidth product,

$$f_T = \frac{1}{2\pi\tau_{ec}}, \tag{2.1}$$

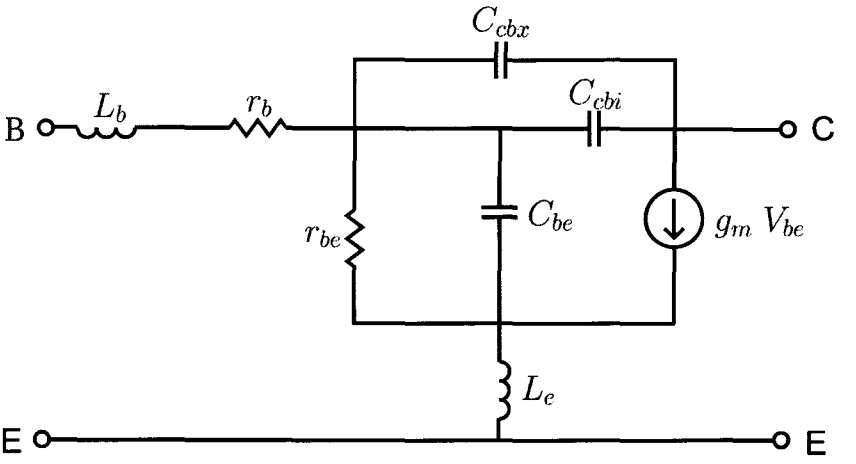


Figure 2.1: Hybrid π high frequency equivalent circuit of a BJT.

Maximum frequency of oscillation,

$$f_{max}^2 = \frac{f_T}{8\pi r_b C_c} \tag{2.2}$$

Minimum Noise figure,

$$F_{min} = 1 + bf^2\left(1 + \sqrt{1 + \frac{2}{bf^2}}\right), \qquad where\ b = \frac{40 I_c r_b}{f_T^2} \tag{2.3}$$

here r_b is the parasitic base resistance, I_c is the collector current, C_c is the collector base capacitance, f_T is the frequency at which the common emitter current gain becomes unity and τ_{ec} is delay time from emitter to collector. For a BJT, τ_{ec} can be as small as 10 Ps.

From the above equations, it is clear that BJT can work satisfactorily in the required frequency range of 30-300 MHz. But its noise figure is too high (typically of the order of 1 dB). This high noise figure is due to its large value of base resistance. Moreover, the noise figure of the BJT increases quadratically with frequency, which has adverse effect in our application where there is a large bandwidth requirement. Hence BJT is not considered in the present design.

2.2.2 Metal-Semiconductor Field Effect Transistor (MESFET)

MESFET is the most commonly used and important active device in MMIC. It is very similar to the silicon FET, but the only difference is that, the channel is formed out of GaAs substrate. The cross sectional view of a MESFET is shown the figure 2.2. The base material on which the transistor is fabricated is semi insulating GaAs substrate. A buffer layer is epitaxially grown over the semi-insulating GaAs substrate to isolate defects in the substrate from the transistor. The channel layer is epitaxially grown over the buffer layer. Since the electron mobility is 20 times the hole mobility in GaAs, the conducting channel is always made of n-type material in microwave transistors.

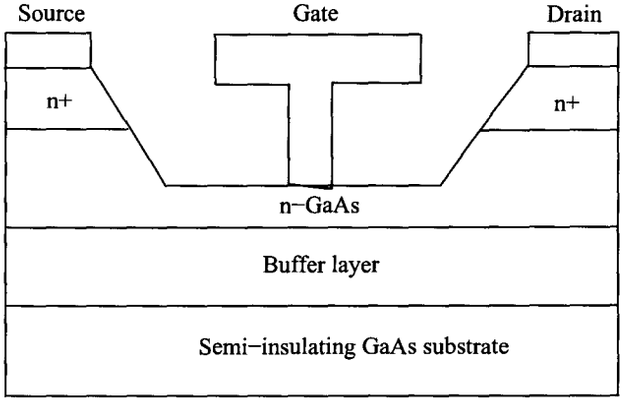


Figure 2.2: Cross sectional view of MESFET.

The figure of merits for the MESFET can be shown as [2, 4]

Gain–Bandwidth product,

$$f_T = \frac{g_m}{2\pi C_{gs}} \tag{2.4}$$

Maximum frequency of oscillation,

$$f_{max} = f_T \left[\frac{4R}{R_{ds}} + 4\pi f_T C_{gd}(R + R_g + \pi f_T L_S) \right]^{-1/2} \tag{2.5}$$

Minimum Noise figure,

$$F_{min} = 1 + 2\pi f \frac{C_{gs}}{g_m} k_1 \sqrt{g_m(R_s + R_g)} \tag{2.6}$$

where g_m is transconductance, C_{gs} is gate-to-source capacitance, L_s is source parasitic inductance, C_{ds} is drain capacitance, R_d is drain-to-channel resistance including contact resistance, R_s is source-to-channel resistance including contact resistance, R_g is gate-metal resistance, R_{ds} is drain source resistance, C_{gd} is gate drain feedback capacitance, R_i input channel resistance, R_g is gate metal resistance, R_s is source to channel resistance, L_S is parasitic source inductance

MESFET achieves lower noise figure than the BJT because its source to drain channel resistance, R_s, is small compared to base resistance, r_b, of BJT. Also the noise figure of the MESFET increases linearly with frequency. All these facts make MESFET a potential candidate for the present design.

2.2.3 High Electron Mobility transistor (HEMT)

HEMT is a field effect transistor. Cross sectional view of HEMT is shown in the figure 2.3. HEMT is based on a modulation-doped GaAs–AlGaAs single hetero junction structure. The density of doping species is modulated, so as to confine and control a two dimensional electron gas (2DEG).

In the absence of the 3-degree freedom, electrons and donors travel in two different media. This minimizes the chances of collision between the donors and electrons and hence increases the mobility of electron. This higher mobility of electrons in HEMT results in lower parasitic drain and source resistances.

HEMTs and MESFETs are modeled by the same equations as shown in the equation ??.

As a result, f_T and F_{max} are increased from the other active devices like MESFET and BJT, for a given gate length and also leads to a lower noise figure and higher

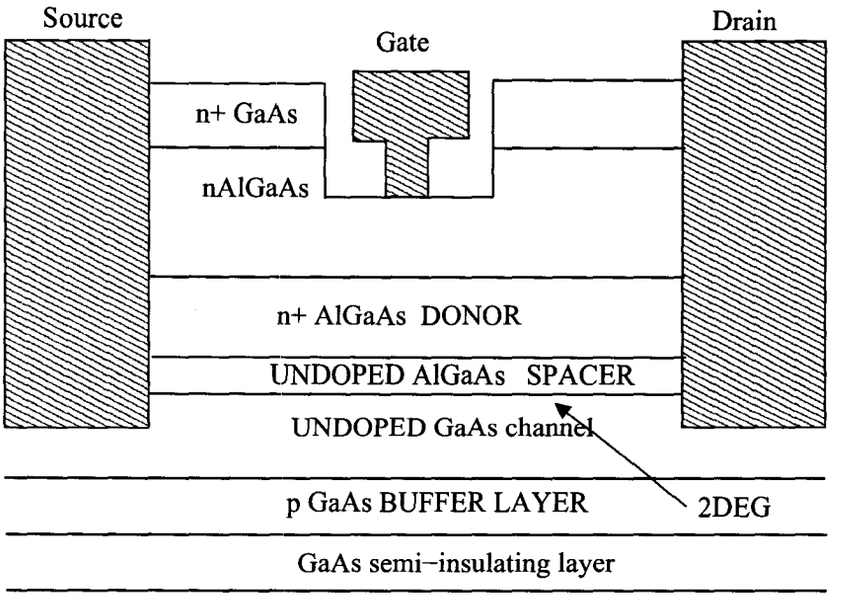


Figure 2.3: Cross sectional view of HEMT.

gain. Due to all these factors, HEMT was considered as the best candidate for our design. Before starting the design using the HEMT, its high frequency noise behavior should be understood. This can be done by analyzing its high frequency noise analysis.

2.3 A review of Broad band amplifiers

Discussed below are various types of broad band amplifiers operating under different principles.

2.3.1 Balanced amplifiers

The working principle of the balanced amplifiers [5] can be explained using the figure 2.4. It employs two amplifiers in parallel with two quadrature hybrids one each at the input and output respectively. The amplifiers in this configuration are matched for minimum noise figure. This gives rise to impedance mismatch at the

inputs resulting in the reflections. The quadrature hybrids make the reflected signals appear 180^0 out of the phase at the source end and hence nullify their effects. This configuration provides broad band flat gain. But due to the lossy input Hybrids, noise figure will be higher.

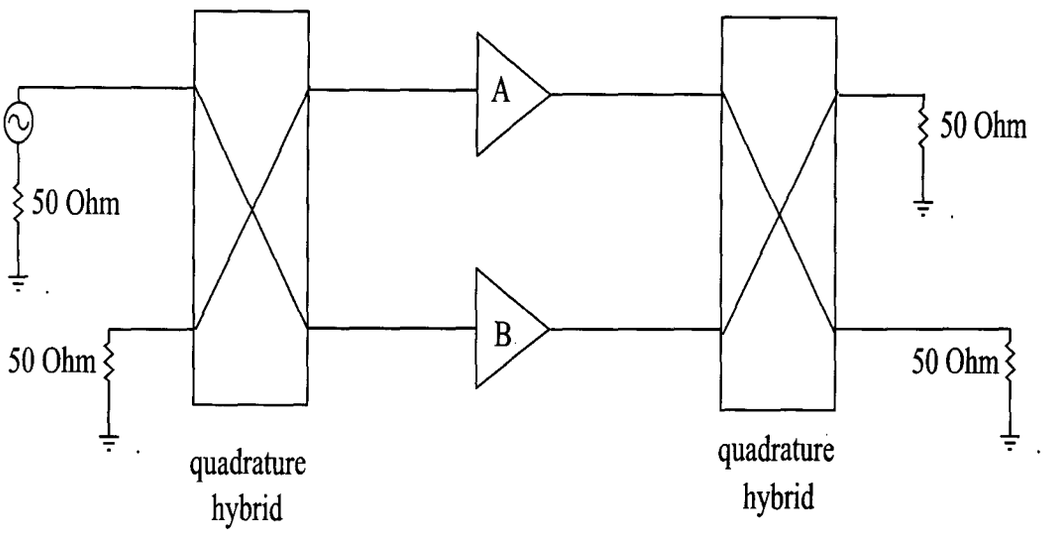


Figure 2.4: Block diagram of a balanced amplifier.

2.3.2 Distributed amplifier (DA)

The circuit diagram of the distributed amplifier is shown in the figure 2.5. A voltage step applied to the input of the figure propagates down the input line causing a step to appear at each transistor in succession. Each transistor generates a current equal to its g_m multiplied by its input. Currents of all transistors ultimately sum in time coherence, if delays of inputs and output lines are matched.

The gain of each device is g_m and the output impedance seen by each transistor is half the characteristic impedance of the transmission line. So the overall voltage gain of the DA is given by

$$A_v = n * g_m * \frac{Z_O}{2} \qquad where\ n\ is\ the\ number\ of\ stages. \tag{2.7}$$

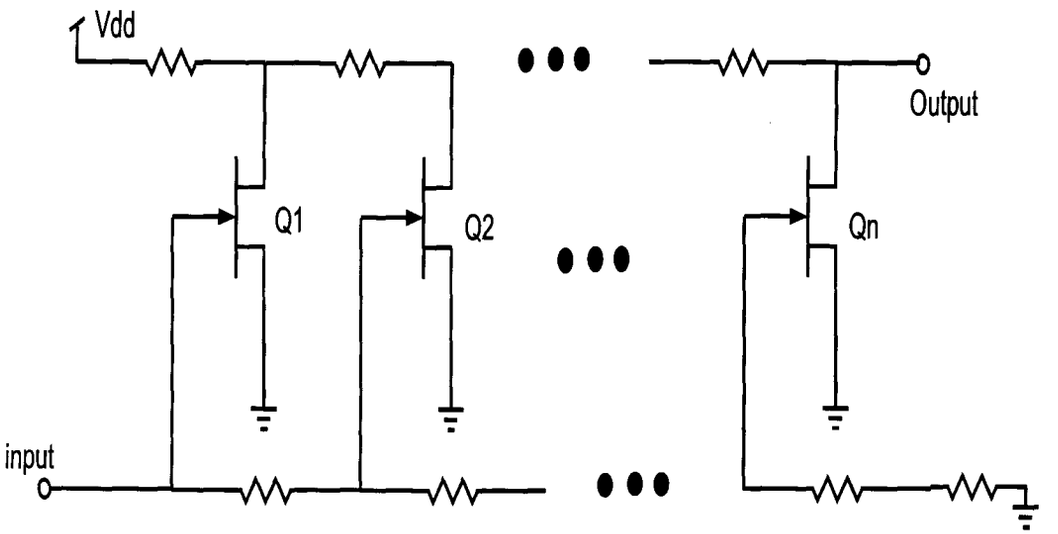


Figure 2.5: Block diagram of a distributed amplifier.

Neglecting losses, the gain demonstrates a linear dependence on the number of devices (stages). Unlike the multiplicative nature of a cascade of conventional amplifiers, the DA demonstrates an additive quality. It is this property of the DA architecture that makes it possible for it to provide gain at frequencies beyond that of the unity-gain frequency of the individual stages. In practice, the number of stages is limited by the diminishing input signal resulting from attenuation on the input line. Bandwidth is typically limited by impedance mismatches brought about by frequency dependent device parasitics.

2.3.3 RL feedback from drain to gate

Normally amplifiers will have higher gain at lower frequencies. In this configuration as shown in the figure 2.6, the series RL feedback between drain and gate of transistor lowers the gain at lower frequencies and hence levels the gain over the entire frequency range. Using this configuration many octave bandwidths could be achieved. Also good I/O return loss, stability can be improved. But noise figure is worse because of the resistive feedback.

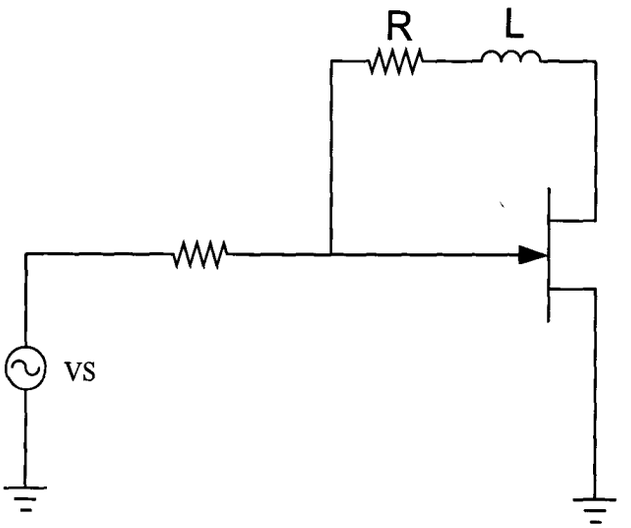


Figure 2.6: Amplifier with RL feedback.

Next section discuss the different types of the low noise techniques and the effect of different input matching sections on the noise performance of amplifier.

2.4 Low noise techniques

Even though low noise amplifiers are critical in the design of RF receivers, their design has not been based on a sound analytical foundation until the paper by Shaeffer and Lee [6]. Their paper not only provides a systematic approach for analyzing and optimizing the design of an inductively degenerated common source CMOS LNA, but also points out the importance of induced gate noise in CMOS technologies.

Many researchers have investigated the design and fabrication of different LNA architectures [7]-[10] using CMOS technology.

The noise performance of the LNA is mainly decided by the type of the input matching network. The following section discusses the effects of different types of the input matching section on the noise figure and gain of the amplifier [11]-[12].

2.4.1 Inductive Source Degeneration

This is the most popular technique in LNA design. Figure 2.7 shows the inductively degenerated common source amplifier. Equation 2.8 gives the relation for input impedance of the amplifier derived from its small signal equivalent circuit. The important advantage in this method is that one has control over the value of the real part of the impedance by a proper choice of inductance in the source leg of the transistor as is clear from equation 2.8

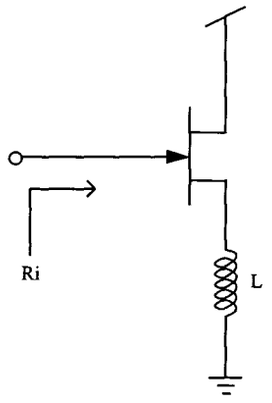


Figure 2.7: Inductively degenerated common source amplifier.

$$R_i \simeq \frac{V_i}{I_i} = \frac{1}{sC_{gs}} + sL + \frac{g_m L}{C_{gs}} \tag{2.8}$$

where c_{gs} is gate to source capacitance, r_o is the output impedance of the transistor.

Also it is observed in the equation that inductor acts as a noise less resistor, i.e. increases the real part of input impedance without adding any additional thermal noise. Hence, we can choose emitter degeneration inductance to produce an input impedance whose real part is equal to the optimum source resistance to achieve minimum noise figure.

But this method can only provide narrow band impedance matching. The overall gain of the amplifier gets reduced.

2.4.2 Active matching amplifier

Inductors occupy large area in MMIC designs. In order to save area on chip, inductors can be replaced with active elements. This property is used in active matching amplifiers, where the lumped inductors are replaced with transistors as shown in the figure 2.8. Bandwidth of this circuit is better compared to the inductive source degeneration. But the matching transistor needs biasing current resulting in higher power consumption. Also, the matching transistor gives rise to thermal channel noise and worsens the noise performance of this amplifier, making it unsuitable for our design. Hence, this method is only suitable for MMIC designs, where saving die area is the primary concern.

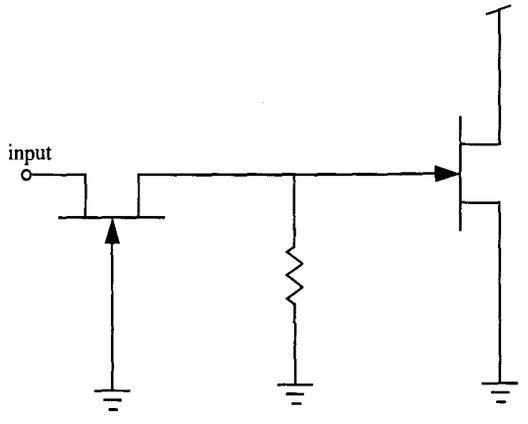


Figure 2.8: Active matching amplifier.

2.4.3 Common source stage with RC shunt feedback

This circuit (shown in the figure 2.9) achieves good bandwidth, but its noise performance is poor. This poor noise performance is due to the resistor coming in the feedback loop. Also it needs large bias current to improve gain and hence results in higher power consumption.

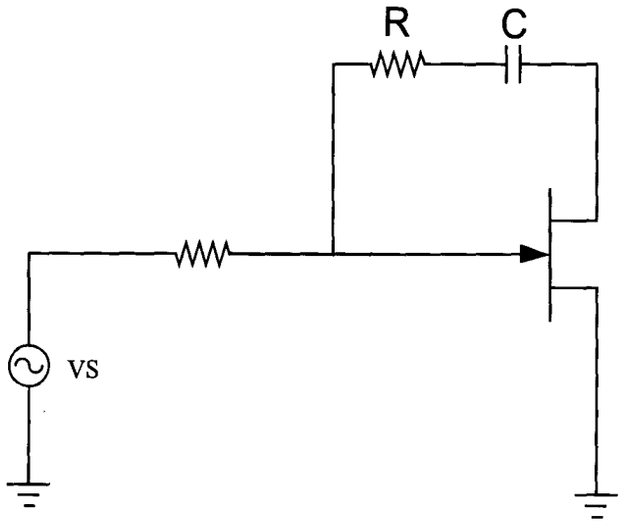


Figure 2.9: Amplifier with RC feedback.

2.5 Linearization Techniques

The LNA linearity is typically measured by the 3^{rd}-order intercept point (IP3), which can be referred to input (IIP3) or output (OIP3). Achieving a high IP3 in combination with a low NF and high gain is a challenging design, which can be achieved by using linearization techniques. Linearization techniques can be broadly classified under closed loop and open loop.

2.5.1 Closed loop techniques

Linear feedback, Harmonic feedback and series feedback techniques are the most popular techniques that are classified under the closed loop. Brief description of each one of them is given below.

Series feedback

In a transistor, the nonlinearity arises due to many factors like transconductance (g_m), output impedance (r_o), nonlinear parasitic capacitances etc. Of all these, the transconductance is the dominating factor. Series feedback is a technique which

linearises the transconductance. Series feedback can be achieved by the source degeneration inductance as shown in the figure 2.10. With source degeneration, the effective transconductance ((g_{meff})) will be decided by the impedance of the source inductance ($g_{meff} = 1/sL$). Hence effective transconductance is made almost independent of device properties. This technique makes the amplifier very narrow banded.

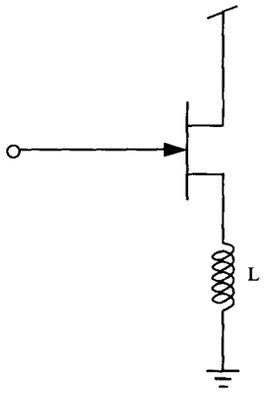


Figure 2.10: Amplifier using series feedback.

Linear feedback

Feedback is the most widely known linearization technique. It is based on feeding back a linearly scaled version of the output signal and subtracting it from the input. The methodology adopted is shown in the block diagram 2.11

Here the non linearities are suppressed by a factor equal to a magnitude of the loop transmission, at the cost of an equal reduction in closed loop gain. One therefore needs an ample supply of excess gain to enable large improvements in linearity.

This technique has some disadvantages like gain reduction and narrow bandwidth. Nishikawa et al. [13] have used active negative feedback to improve third order inter-modulation distortion ratio at high input power levels.

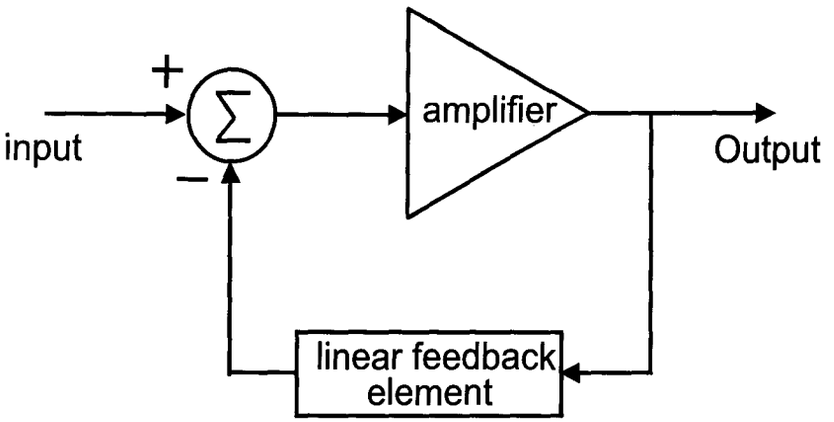


Figure 2.11: Linear feedback method.

Second Harmonic Feed back

Recently Moazzam et. al have used a novel technique [14] of second harmonic feedback and achieved quite good results on par with analog pre-distortion. This novel technique is based on using the non-linearity property of the amplifier to cancel out the 3^{rd} order IM product.

This technique can be explained from the figure 2.12. The second harmonics of the source signals which are produced at the amplifier output are fedback to the input of the amplifier through a series of band pass filter (BPF), variable attenuator and variable phase shifter. Non-linearity of the amplifier causes interaction between the source signals and their fed back second harmonics resulting in additional signals at the output of the amplifier at the 3^{rd} order inter-modulation frequencies. By proper selection of phase and amplitude of the fedback second harmonics, it is possible to make the 3^{rd} order inter-modulation product produced by the second harmonics to have same amplitude as the original 3^{rd} order product, but with 180^0 out of phase. As a consequence the 3^{rd} order inter-modulation distortion gets totally cancelled.

This technique requires a wide band feedback loop which includes a band-pass filter, a variable phase shifter, a variable attenuator and a power combiner. Also the

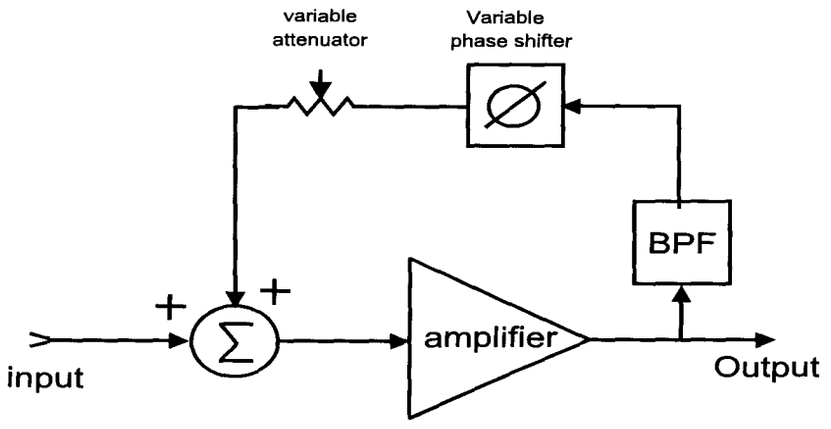


Figure 2.12: Harmonic feedback method.

frequency performance is poor because of the narrow band nature of the feedback elements.

2.5.2 Open loop techniques

Feed-forward

The technique adopted in the feed forward amplifier to reduce the harmonic level is as shown in the figure 2.13 [15]. The amplifier1 produces at its output, an amplified input signal and higher order components (A_{vi}, ϵ), when it operates in the saturation mode. This output is subtracted from the input after suitably attenuating, to separate out the harmonic component (ϵ/A). This component is further amplified by a factor 'A' before subtracting from the delayed version of the input to produce mainly the spurious free amplified input. This is under the assumption that, the higher order modes generated by the amplifier2, is much weaker than the signal itself.

As there is no feedback involved, this technique avoids the stability problems. Under theoretical assumptions this will give infinite bandwidth. But practically, the bandwidth over which this technique woks depends upon the bandwidth over which the group delay of the individual amplifier may be tracked by the realizable

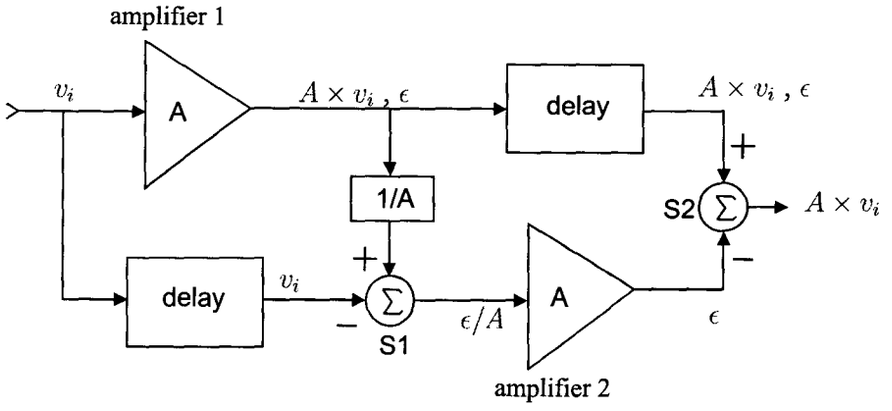


Figure 2.13: Feed forward amplifier.

time delay elements. The amount of linearity improvement at the output depends on the matching of the two paths. Noise performance is also poor for this technique, since the two paths directly load the RF input. Difficulty in matching the two paths makes it operate over a narrow band.

Even though this technique offers higher bandwidth, low power efficiency, higher noise figure and difficulty in matching the two paths make it unsuitable for our project.

Pre-distortion

The principle of the pre-distortion can be explained by the figure 2.14. It exploits the fact that, by cascading a nonlinear element (amplifier in saturation) with its mathematical inverse results in an overall transfer characteristic that is linear. The compensating element is called pre-distorter since it precedes the non linear amplifier. In practice, it is impossible to cancel all orders of nonlinearity simultaneously. Therefore, the linearizer is usually designed to cancel the nonlinearity due to 3^{rd}-order component.

If the amplifier exhibits a gain compression, the pre-distorter is designed to have a gain expansion characteristic, and vice versa. The linearizer can be built out of either shunt or series, active or passive elements [16]-[22].

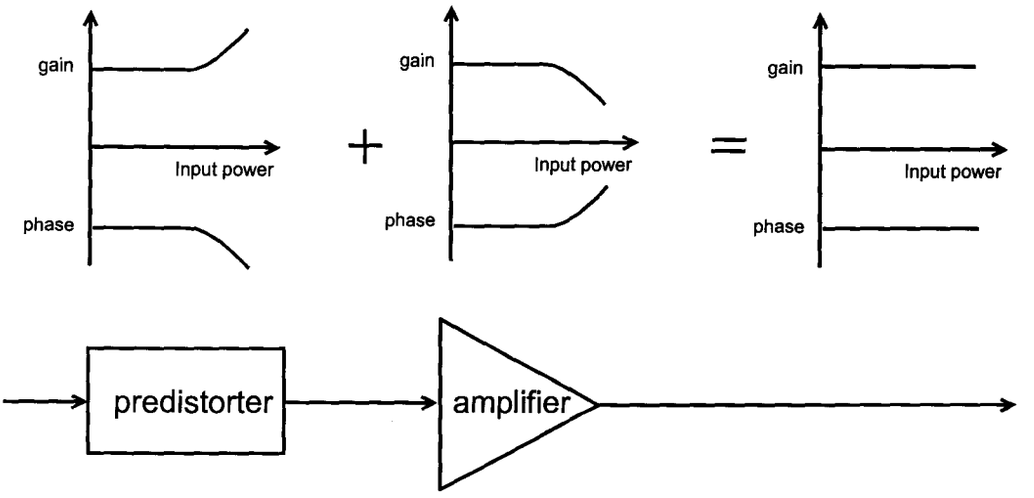


Figure 2.14: Principle of Pre-distortion linearizer.

Pre-distorters can be broadly divided into analog and digital pre-distorters. Analog pre-distorters are small, inexpensive, and simple in configuration and use non linear devices like diodes and transistors. However, because of the accuracy to which the transfer functions may be realized, analog pre-distorters are generally used to reduce the third-order inter modulation components [23]-[24]. In order to compensate for higher-order inter modulation distortions in multi-carrier systems, more complex circuits may be employed. Moreover, an adaptive control circuitry is often needed to ensure linear operation of the amplifier over a wide range of input power, ambient temperature, frequencies etc. Digital base band pre distortion methods have been popular in recent years due to their higher accuracy, as compared to analog systems. However, these techniques makes the circuit more complex than analog. The computational speed of the digital circuits limits the bandwidth of operation.

In general, the noise performance of the amplifier gets degraded by the use of pre-distorters.

Post-distortion

Post-distorter functions similar to pre-distorter, but uses a linearizer after the amplifier. Since the linearizer is coming after the amplifier, Post distortion circuit resolves the noise figure issue of the pre-distorter [25, 26].

Since power amplifiers in general have very large signal swing output, it would be difficult to correct for distortion. Moreover, the power added efficiency gets reduced by the post distorter. Hence pre distorter is normally preferred over the latter. However, in LNAs, the output signal swing is relatively small, and PAE is not vital. Therefore, the post-distortion method deserves a wider attention.

None of the techniques mentioned above satisfies the requirements of meeting sufficient gain, low noise figure and good impedance match simultaneously over a wide range of frequencies because of the inherent limitation that each one of them possesses. So, to meet our requirements, we have tried to adopt Thermal noise cancellation technique to achieve low noise over as wide range of frequencies as possible. To improve the dynamic range, post-distortion technique has been applied.

Chapter 3

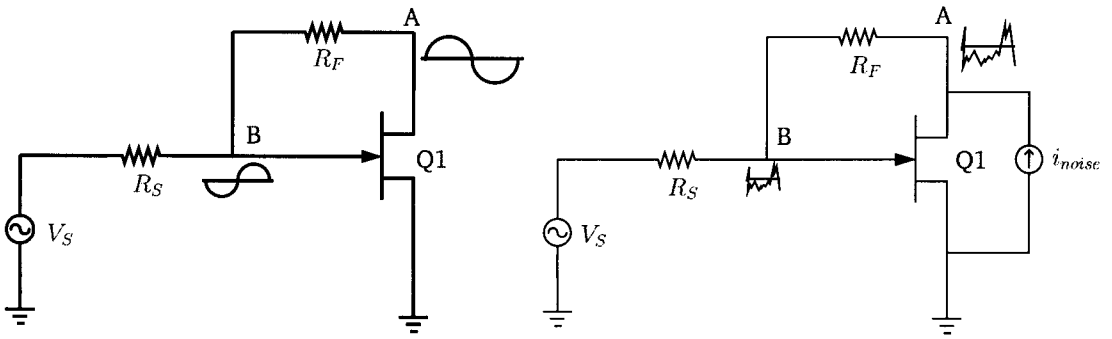
Design of the LNA using the Thermal Noise Canceling technique

3.1 Principle of thermal noise cancellation (TNC)

The salient feature of thermal noise cancellation technique is that, the interdependence of the low noise behavior and impedance match for the maximum power transfer is completely eliminated [27]. Each of them is achieved independently in different parts of the circuit to achieve the required amplifier performance.

The principle of operation of the noise cancellation technique is explained below. Consider a simple voltage shunt feedback amplifier circuit as shown in the figure 3.1. If r_o represents the output impedance of the transistor and g_m the transconductance then, the input signal V_B at the node B appears amplified by a factor $|1 - g_m r_o|$ at the node A, with a phase shift of 180^0

Let V_n be the drain to source channel noise generated at the output of the transistor (node A). This noise voltage appears at the node B in same phase but with an amplitude reduced by a factor $1 + R_F/R_S$. The voltage at the node B is suitably amplified and phase inverted before adding on with the voltage at node A. This results in



(a) (b)

Figure 3.1: (a) signal & (b) Source-drain noise voltages of the shunt feedback amplifier

1. Cancellation of the major portion of the drain generated noise of the transistor Q1 and

2. Amplification of the input signal

Addition of the two node voltages V_A and V_B is accomplished by introducing an adder circuit (noise cancellation circuit) at the output of the 1st stage of the amplifier as shown in the figure 3.2

By designing the input stage for the maximum power transfer and output stage for noise cancellation, both low noise performance and good input VSWR could simultaneously be achieved. However, complete noise cancellation takes place for only the source drain generated thermal noise at the output of the transistor Q1, but not for

1. Noise arising out the resistor R_{Fm}, which is miller equivalent of the feedback resistor, RF, at the input of the matching stage as shown in the figure 3.3.

2. Gate induced and gate resistive noises.

3. Noise contributed by the transistors Q2 & Q3 shown in the figure 3.2.

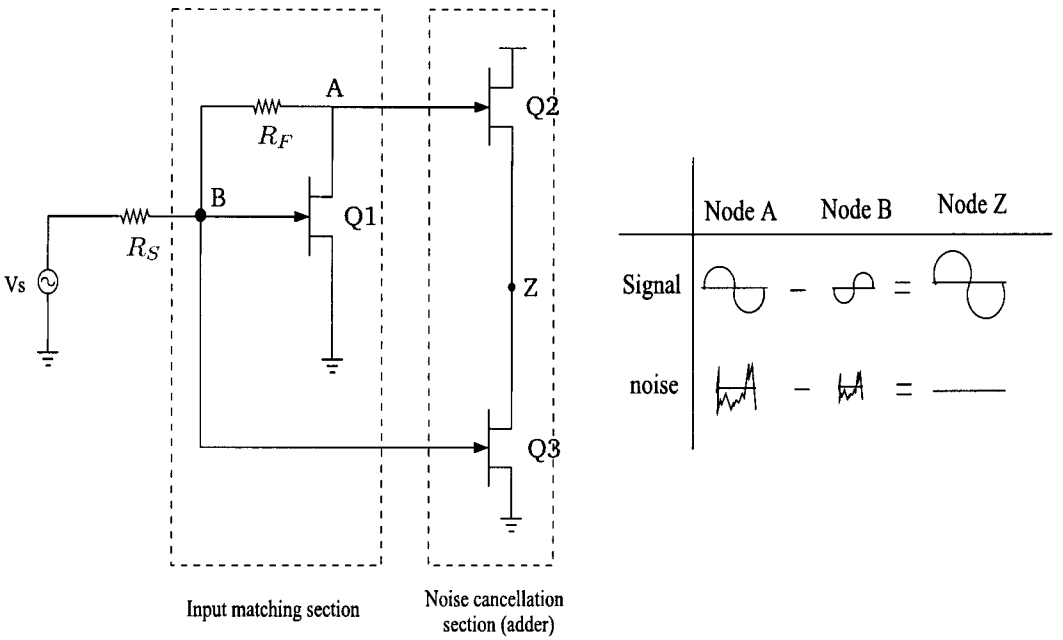


Figure 3.2: Schematic of LNA adopting thermal noise cancellation technique.

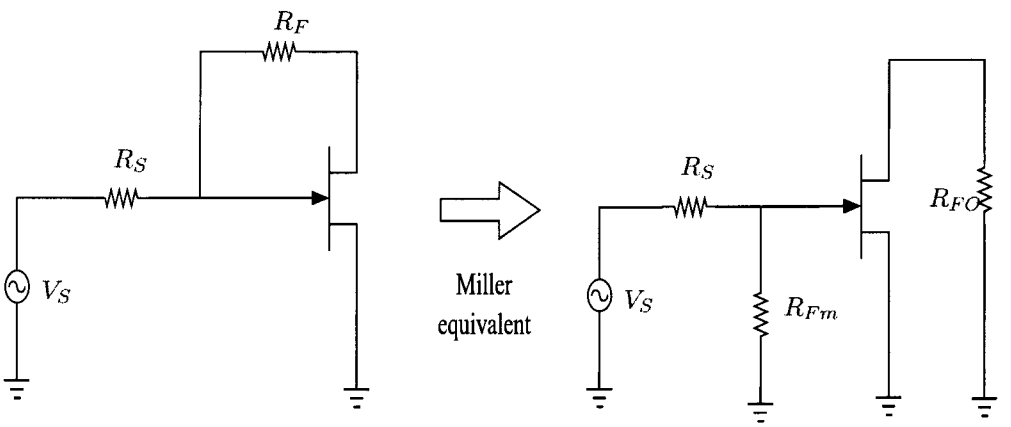


Figure 3.3: Miller equivalent of the input matching section of the amplifier shown in figure 3.2.

since these noise components do not appear with required amplitude and phase at the noise cancellation section input. These noise components continue to be present at the input as residual noise preventing us from achieving zero noise condition. The noise factors due to the input matching section, feedback resistor (R_F)

and the noise cancellation stage (NC) are determined from the following relationships:

$$EF_{input\ matching\ stage} = 0 \tag{3.1}$$

$$EF_{Feedback\ resistor} = \frac{R_s}{R_F} \tag{3.2}$$

$$EF_{NC} = \frac{NEF}{g_{m2}}\left(\frac{1}{R_S} + \frac{3}{R_F} + \frac{2R_S}{R_F^2}\right) \tag{3.3}$$

where NEF is Noise excess factor [27]

3.2 Design of the LNA

3.2.1 Design of the 1st stage

The parameters to be found out in the design of the first stage as shown in the figure 3.4 are Feedback resistor (R_F) and transconductance (g_m) of the transistor Q1. A decoupling capacitor C_C is introduced in the fedback path in order to isolate the bias from the feedback resistor. The value of it is chosen in such a way that its reactance is made much smaller than (R_F) (10 nF in our case). In general, the gain of the LNA is chosen such that the stages following it contribute very less noise effectively at the input [28]. So a gain (A_v) of at least 10 has been chosen in our design.

The small signal equivalent circuit of the figure 3.4 is as shown in the figure 3.5. The input impedance from it can be derived as[1]

$$R_i = \frac{r_o \| R_L + R_F}{1 + g_m(r_o \| R_L)} \tag{3.4}$$

where, g_m is the transconductance of the transistor, r_o is the output impedance of the transistor and R_L is the load at the output of the first stage. For the maximum

[1]See Appendix A for the derivation.

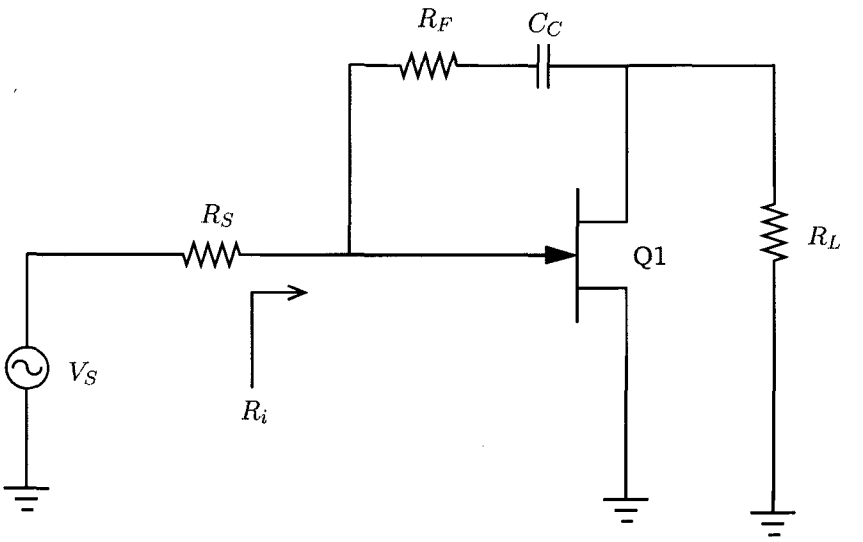


Figure 3.4: 1st stage of LNA.

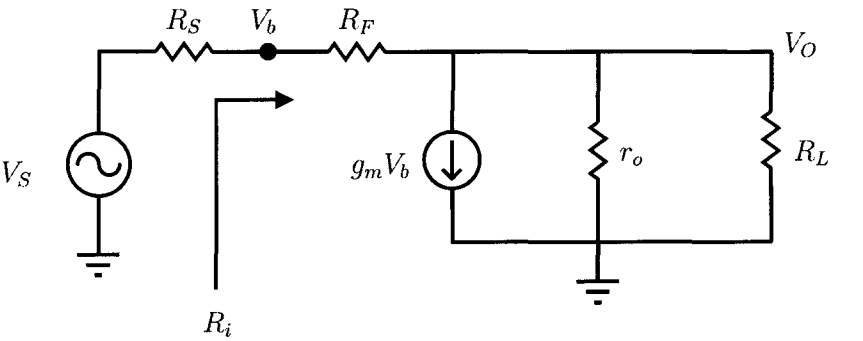


Figure 3.5: Small signal equivalent circuit of the figure 3.4.

input power transfer, the input impedance of the amplifier, R_i, must be equal to the source impedance (R_S), which is normally 50 Ω.

The small signal gain, A_v, of the amplifier can be written as

$$A_v = \frac{V_O}{V_b} = -\frac{(g_m R_F - 1)}{1 + \frac{R_F}{r_o \| R_L}} \tag{3.5}$$

With a prior knowledge of r_o (which in our case is $\approx$ 450 Ω at a bias point of V_{ds} = 3 V $\& I_{ds}$ = 40 mA.), R_F and g_m are determined using the equations 3.4 & 3.5

The approximate values determined were R_F = 500 Ω, g_m = 0.3 A/V, for $R_L \gg$

r_o

3.2.2 Design of the 2nd stage

The circuit diagram of the 2nd stage is shown in the figure 3.6. The main parameters to be determined in the second stage are the individual gains of the transistors Q2 & Q3.

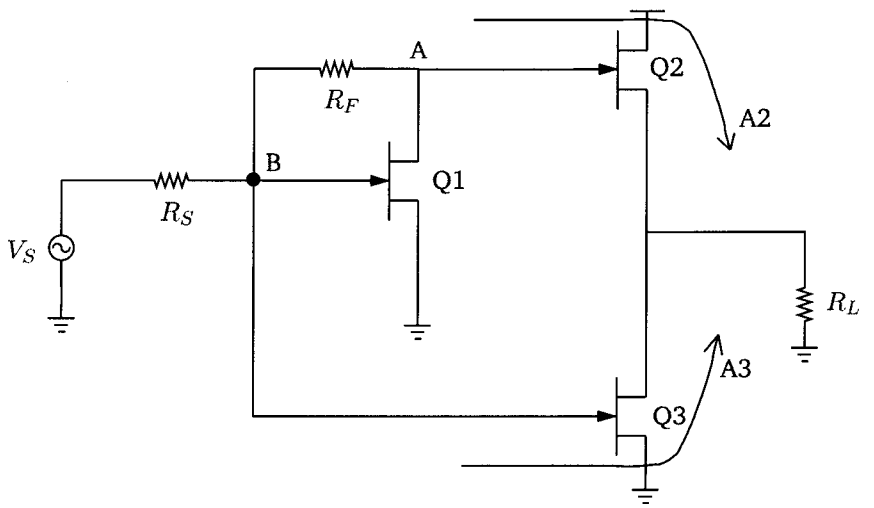


Figure 3.6: Schematic of the two stage LNA.

Since the noise voltage at node B appears $(1 + R_F/R_S)$ times weaker when compared to that at the node A, Q3 should have a gain (A3) equal to $(1 + R_F/R_S)$ in order to ensure equal amplitudes of the noise voltages at the input of the noise cancellation stage. This assumes a unity gain for the transistor Q2, i.e. $A_2 = 1$.

Expressing the gain A_3 in terms of the transconductance[2], we get

$$A_3 = -g_{m3} \times \left(r_{O3} \| R_{i2} \| R_L \| r_{o2} \right) = -g_{m3} \times \left(r_{O3} \| \left(\frac{1}{g_{m2}} \right) \| R_L \| r_{o2} \right) \tag{3.6}$$

[2]See Appendix B for the derivation.

where R_{i2} is the impedance looking into the source of Q2, which is approximately equal to $1/g_{m2}$.

Assuming $(r_{o3}\|r_{o2}\|R_L) \gg 1/g_{m2}$, we can approximate equation 3.6 as

$$A_3 \simeq -\left(\frac{g_{m3}}{g_{m2}}\right) \tag{3.7}$$

Hence the transconductance ratio required for the design can be calculated from the equation 3.7 as

$$\frac{g_{m3}}{g_{m2}} \approx (1 + R_F/R_S) = 11 \tag{3.8}$$

Since the transistor conductance g_m is proportional to $\sqrt{I_{ds}}$, where I_{ds} represents the drain current, the above equation can be written as

$$\frac{g_{m3}}{g_{m2}} \approx \sqrt{\frac{I_{ds3}}{I_{ds2}}} = 11 \tag{3.9}$$

$$\frac{I_{ds3}}{I_{ds2}} \approx 121 \tag{3.10}$$

For the device chosen (ATF-54143), the range of drain current recommended for achieving minimum noise figure is 1–90 mA. This can be observed from the figure 3.7 as obtained from the transistor datasheet.

With these constraints, the ratio of transconductances can have a maximum value of 9.5 instead of 11. This limitation results in an incomplete cancellation of the thermal noise. Accordingly I_{ds2} was set at 1 mA & I_{ds3} was set at 90 mA.

The distribution of drain currents for Q2 & Q3 has been achieved using the configuration as shown in the figure 3.8. The inductance used prevents the leakage of the RF signal into the bias section.

Figure 3.9 shows the complete schematic diagram of the Low Noise Amplifier with designed values.

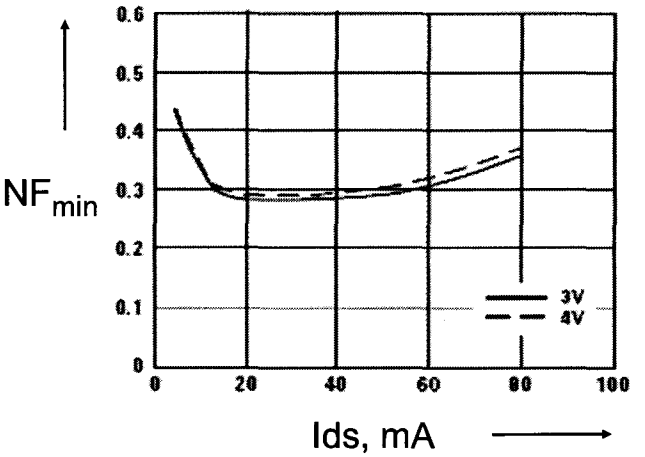


Figure 3.7: Noise Figure minimum as a function of Ids at Vds = 3 V & 4 V as obtained from data sheet.

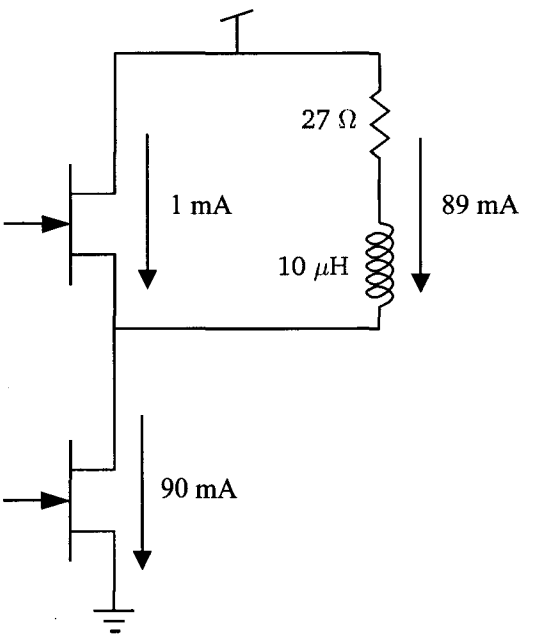


Figure 3.8: Method of biasing the noise cancellation stage.

3.3 Simulation of the LNA performance

The response of the amplifier was simulated using ADS – a CAD package for RF and Microwave circuits, in order to optimize the performance characteristics of it. The simulation process was carried out in three discrete phases. In phase 1, the input

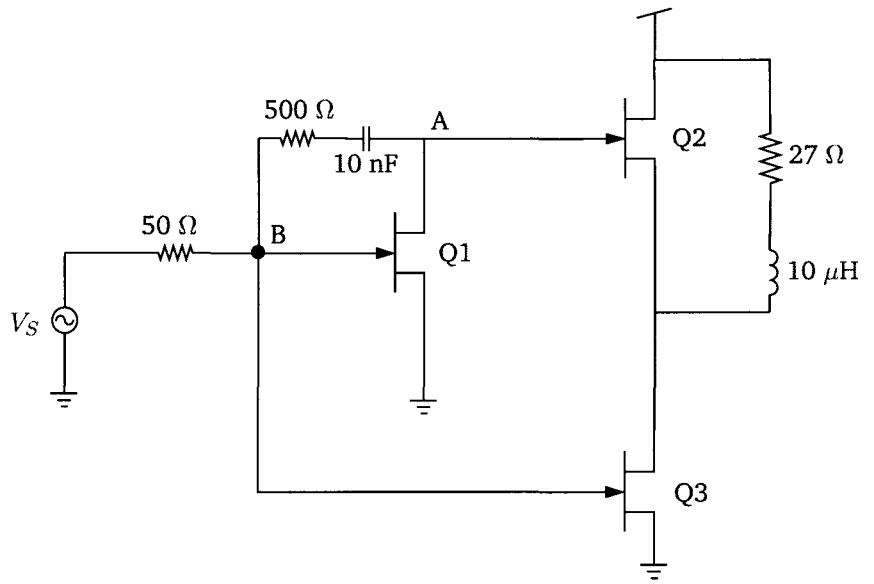


Figure 3.9: Complete circuit diagram of the Low Noise Amplifier with designed values.

matching section was simulated. In phase 2, the principle of TNC was validated using ideal 2nd stage and in phase 3, the entire circuit was optimized.

3.3.1 Input matching section

In phase 1, the input matching section optimization was carried out for a good input return loss and desired power gain of ~20dB. The optimized circuit and the obtained plots of the gain, noise figure, input & output return losses are shown in Figure 3.10 & figure 3.11 respectively.

3.3.2 Validation of the noise cancellation principle

In order to validate the principle of TNC, the second stage of the amplifier was introduced having ideal behavior for all the components in it (shown in the figure 3.12). The noise performance as shown in the figure 3.13 clearly indicates that, the cancelling property of the circuit has brought down the overall noise figure from 0.659 dB to 0.332 dB .

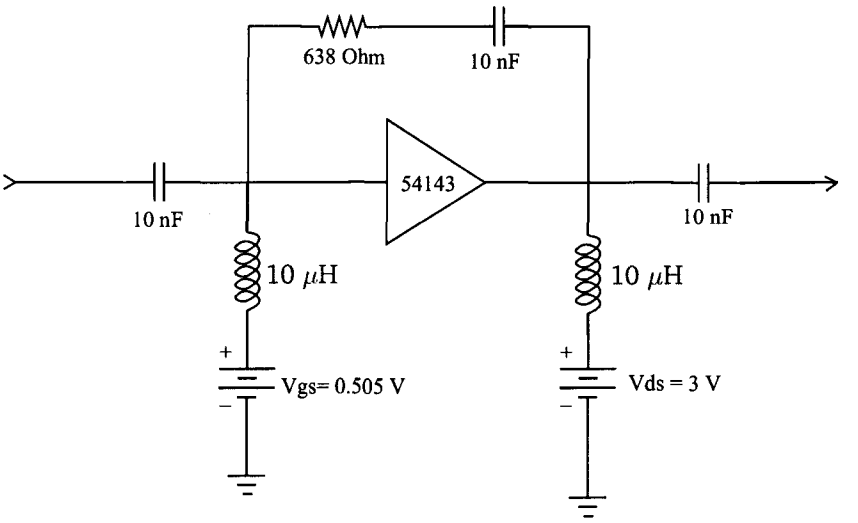


Figure 3.10: 1st stage of LNA (optimized in ADS).

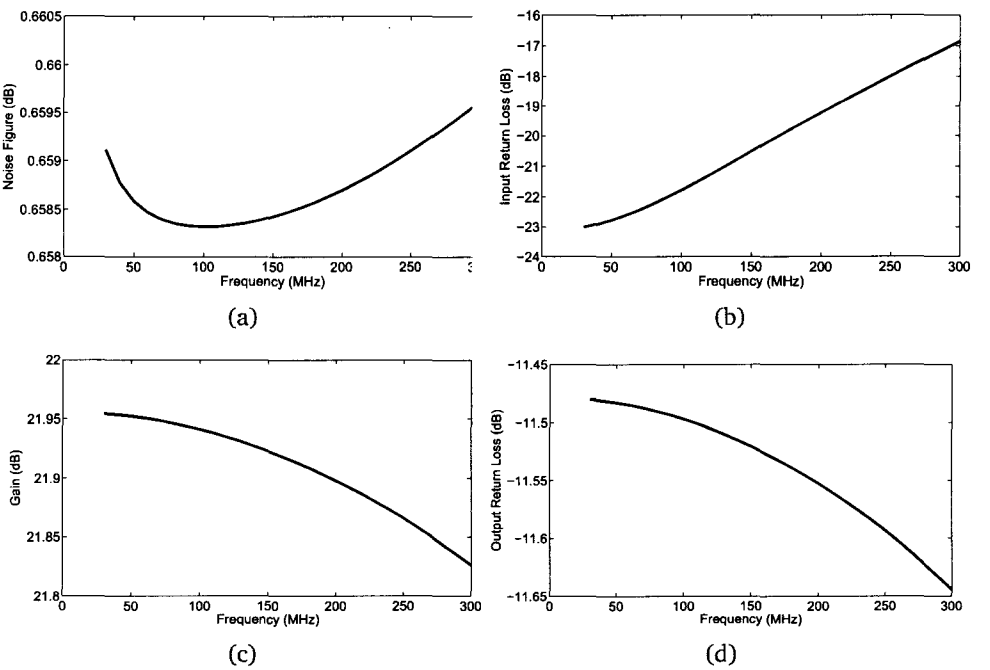


Figure 3.11: Simulated (a) Noise figure, (b) input return loss (c) gain & (d) Output return loss of the LNA as a function of frequency.

From the plot 3.13 it can be seen that, a minimum noise figure that can be achieved is 0.332 dB. The expected residual noise according to equation 3.2 is 1 +

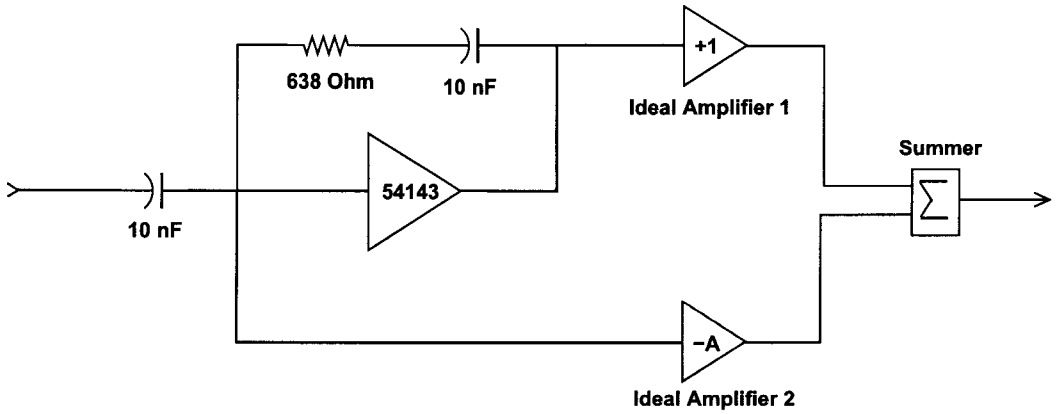


Figure 3.12: Block diagram of 1st stage along with ideal 2nd stage.

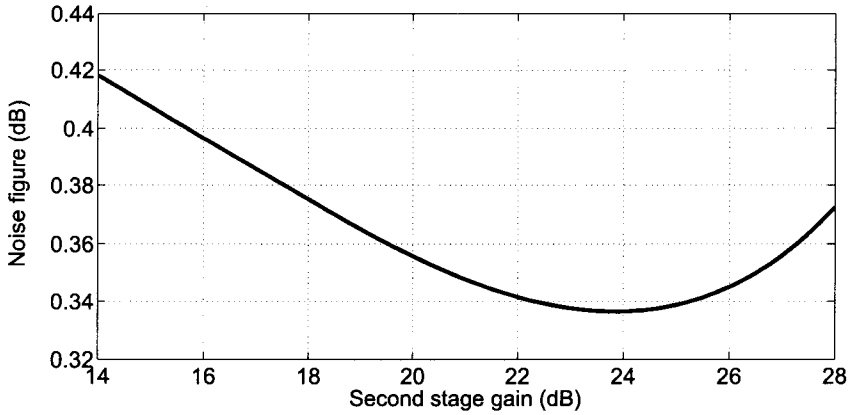


Figure 3.13: Noise figure vs 2nd stage gain (A) of the figure shown in 3.12.

R_S/R_F= 1.07836=0.328 dB. This small deviation of simulated NF_{min} from the expected NF_{min} is due to the Gate resistive and Gate induced noises, which are not cancelled by the TNC technique.

Figure 3.13 also shows that the minimum noise performance occurs for a second stage gain of 23.2 dB. This is in accordance with the predicted gain of the second stage, which is equal to $1 + R_F/R_S$= 13.76 = 22.772 dB.

3.3.3 Second stage simulation

Phase 3 was carried out (with the ideal 2nd stage replaced by the elements having non ideal behavior) taking into account the non ideal behavior of the various elements of the circuit. The circuit shown in the figure 3.14 was optimized under this condition to get optimum response in terms of overall noise figure, input return loss and gain. The plots of these parameters as a function of frequency are shown in the figure 3.15.

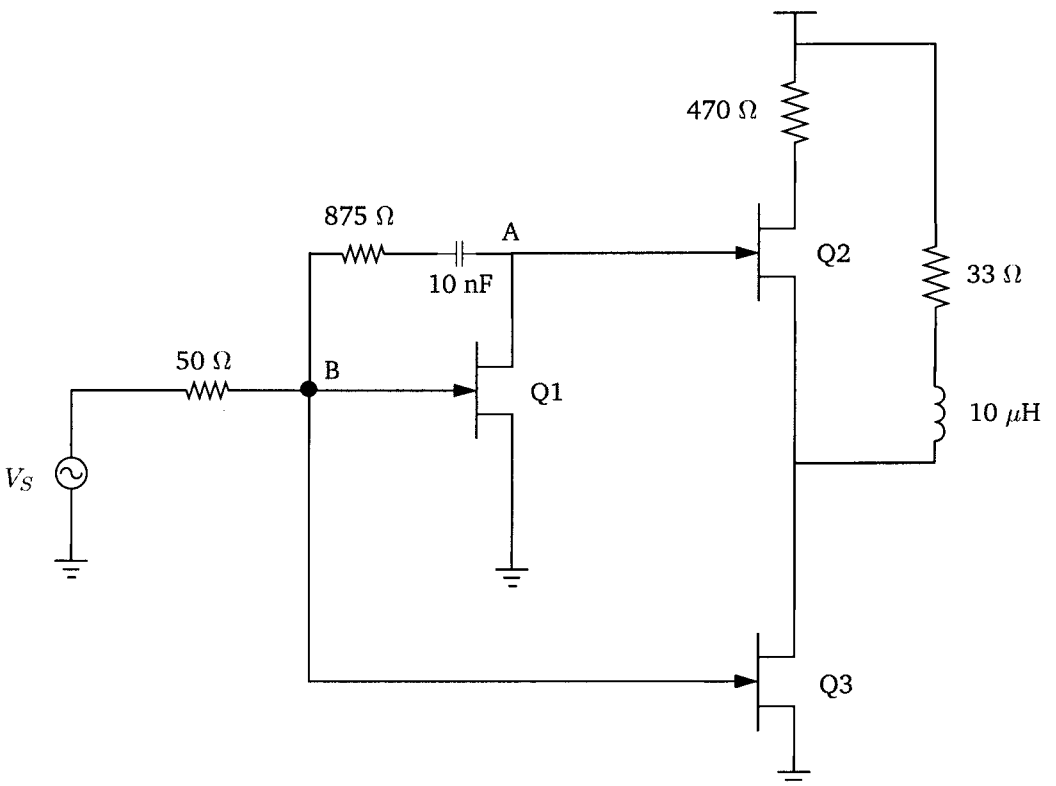


Figure 3.14: LNA circuit optimized in ADS.

Figure 3.15 shows that, the amplifier has got an overall gain of ~24–25 dB with a noise temperature of 32 K. The return loss of the amplifier is better than −11 dB over the entire frequency range.

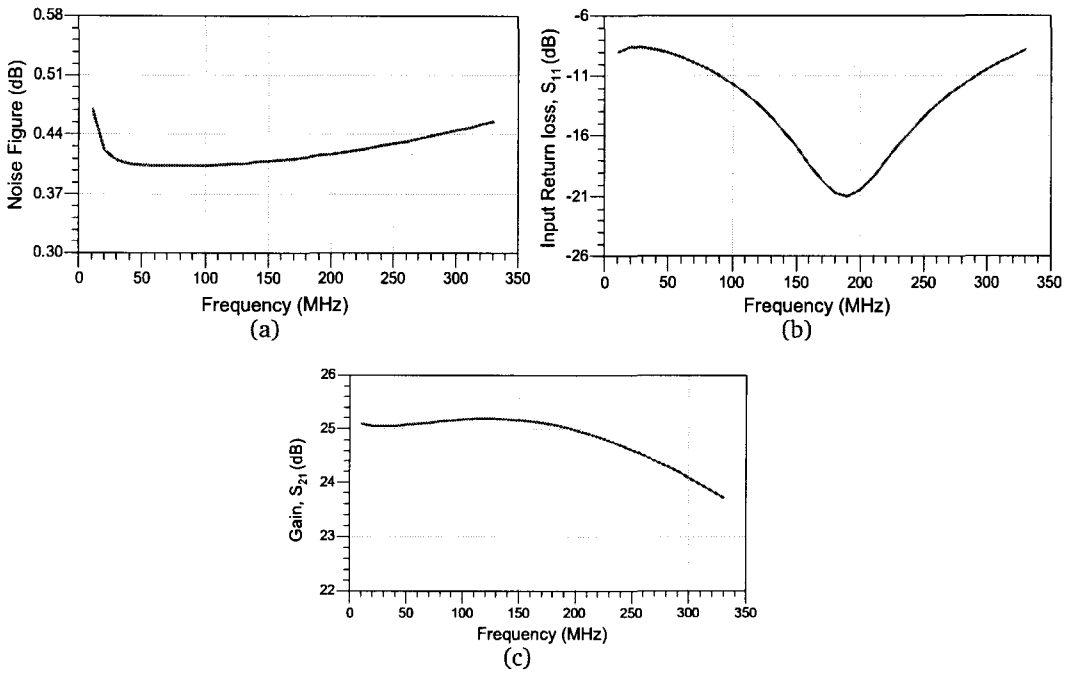


Figure 3.15: Simulated plots of (a) Noise figure, (b) input return loss & (c) gain of the LNA as a function of frequency .

The stability of any amplifier can be determined using the Rollett's stability factor (K) and $|\Delta|$ which are as defined in the equation 3.11 [29]. The stability characteristics of the present amplifier was obtained & is as shown in the figure 3.16. It clearly shows that, the amplifier is unconditionally stable over entire frequency range.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2\,|S_{12}S_{21}|} > 1 \qquad where, |\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \quad (3.11)$$

Simulation was also carried out to obtain its 1dB compression point and output 3rd order intercept point (OIP3). 1dB compression point was obtained by feeding signals of various power levels ranging from -50 dBm to $+10$ dBm. It was carried out at 180 MHz, which is very close to the band center ($f_{center} = 165\ MHz$). The

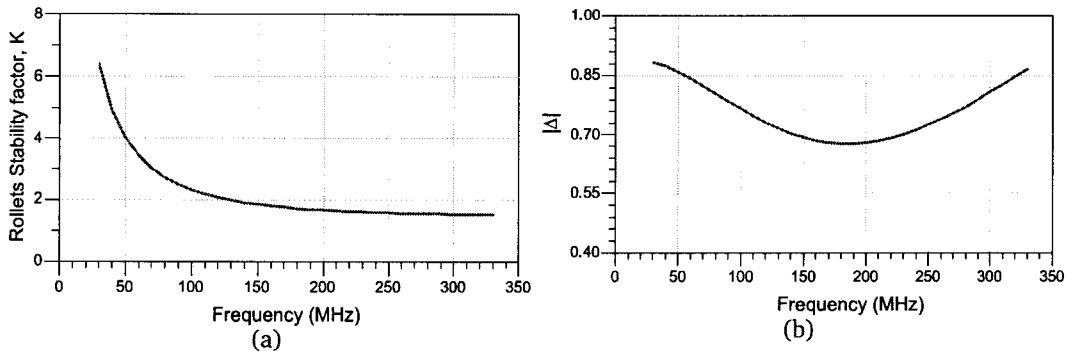


Figure 3.16: Simulated plots of (a) Rollett's stability factor, K & (b) $|\Delta|$ of the LNA.

response obtained is as shown in the figure 3.17. The response shows that, the output 1dB compression point is around +5 dBm.

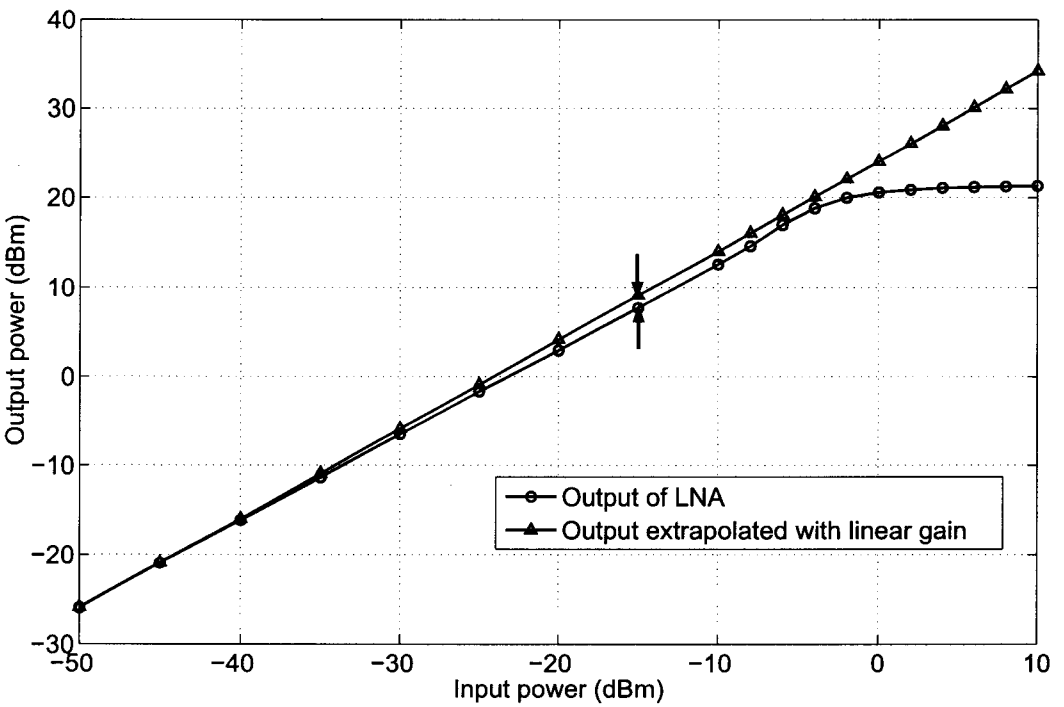


Figure 3.17: Simulated 1dB compression point obtained by sweeping input power.

Similarly, 3rd order intercept point was also obtained in simulation by feeding two tones of same amplitude centered at 181 MHz and with a frequency spacing of

2 MHz. The power level of these two tones was varied from −50 dBm to 0 dBm and at each power level, both the fundamental and 3rd order inter modulation component levels were monitored. Tangents were drawn for both the fundamental and 3rd order components as shown in the figure 3.18. The point of intersection of these two tangents occurs at +14 dBm. This point represents the OIP3 of the entire amplifier [30].

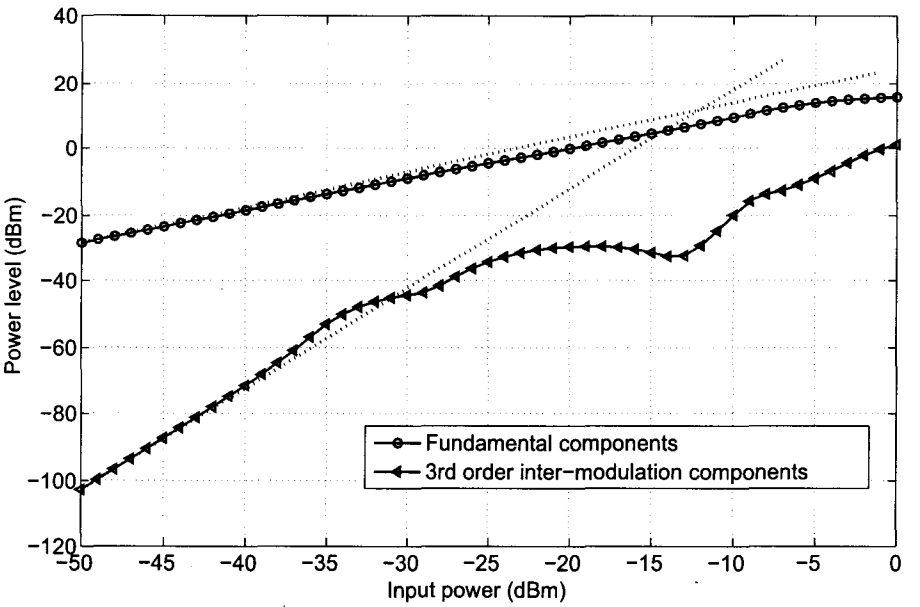


Figure 3.18: Simulated OIP3 obtained from extrapolating fundamental and third harmonics.

The variation of gain and phase as function of input power was also obtained to get the transfer characteristics of the amplifer. Simulated response as shown in the figure 3.19 shows that, the amplifer starts behaving non linearly for the input power level ≥ -30 dBm.

As a result of non linearity, gain starts drooping and the phase starts increasing as a function of input power level. In order to enhance the dynamic range performance of the LNA, a transistor based non-linear element was introduced at the output for correcting the distortion caused in the amplifier circuit due to higher

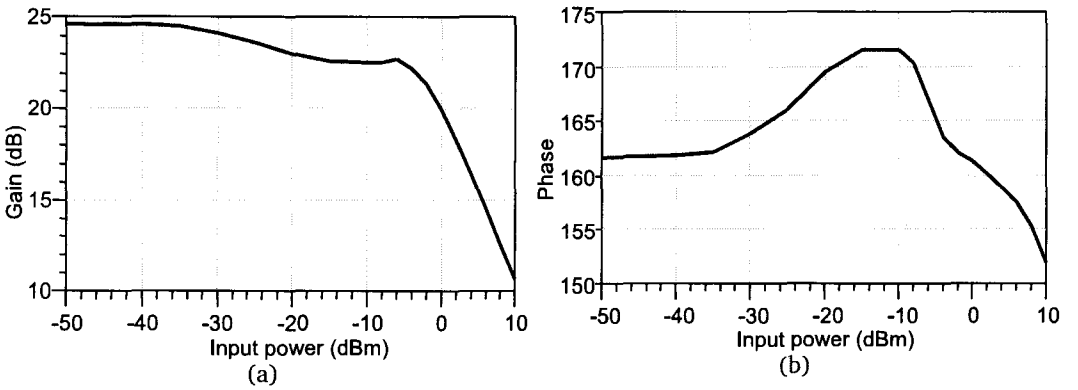


Figure 3.19: Simulated (a) gain & (b) phase characteristics of the LNA with respect to input power at 180 MHz.

input power.

The schematic diagram of the transistor based non linear element is shown in the figure 3.20.

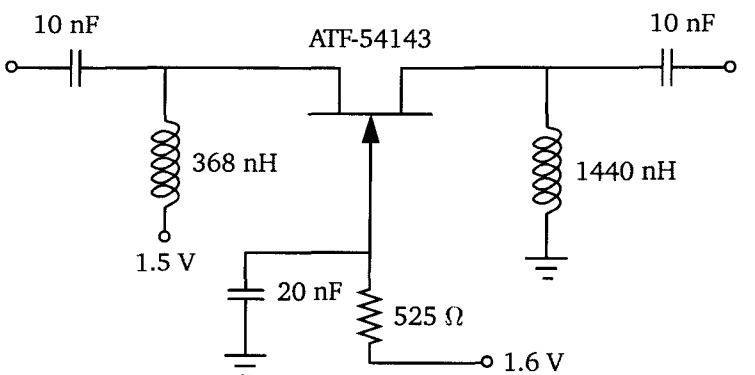


Figure 3.20: Schematic diagram of the transistor post distorter.

The transistor (ATF-54143) is biased near the pinch off, so that any variation in the input power level effectively reduces the net V_{ds} supplied to it and hence decreasing the resistance (as shown in the figure 3.21). Decrease in the resistance results in an increase in the gain of the transistor. This property of gain variation as a function of input power level can be utilized to correct the amplitude distortions of the amplifier circuit. The reactive elements used at the input and output can be

used to get the required phase characteristics of the non linear element.

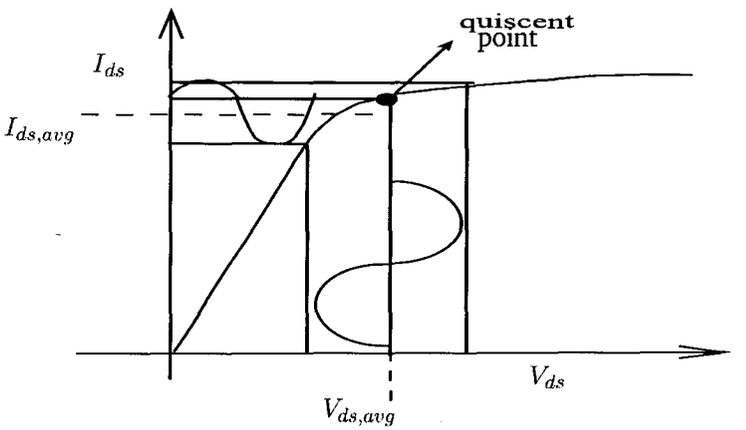


Figure 3.21: Movement of the bias point at higher input power level for a post-distorter circuit.

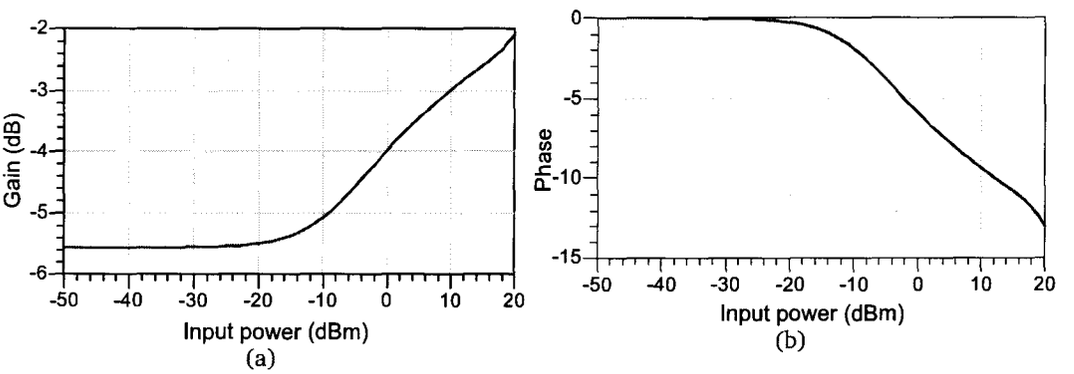
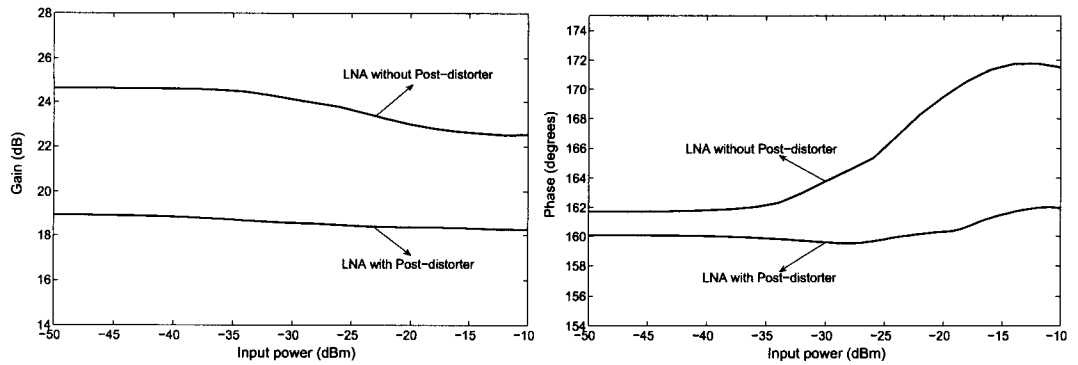


Figure 3.22: Simulated (a) gain & (b) phase characteristics of the post-distorter with respect to input power at 180 MHz.

The post-distorter was included at the amplifer output and its component values were optimized to get the desired response of having constant gain and phase over the entire range of frequency for input power levels as large as -10 dBm (shown in the figure 3.22).The optimized response of the gain and phase of LNA with Post-distorter is as shown in the figure 3.23 along with the response of LNA without Post-distorter.



(a) (b)

Figure 3.23: Comparison of (a) gain & (b) phase characteristics of the LNA with and without post-distorter with respect to input power at 180 MHz.

Also shown in the figure 3.24 is the improvement obtained in the relative third order inter modulation components. It is clear from the response that, an improvement of at least 5 dB is seen between input power level of -21 dBm to -9 dBm.

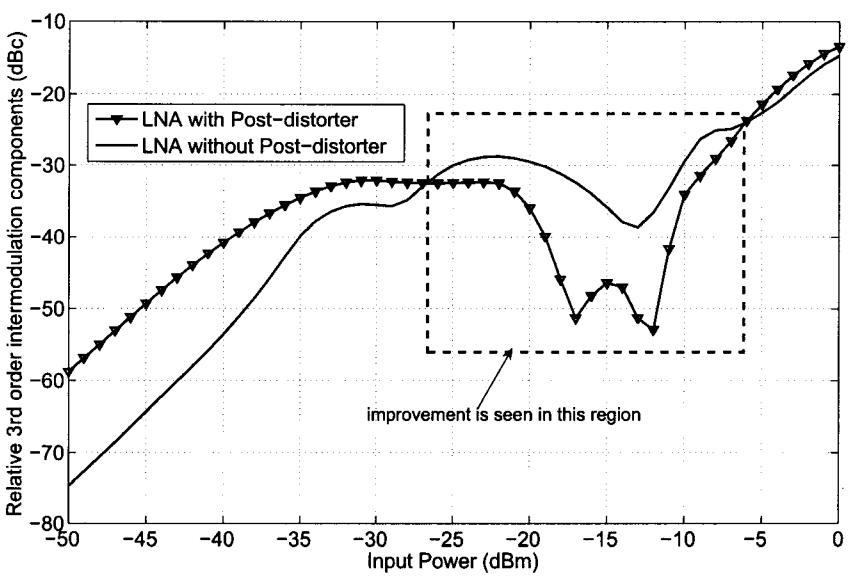


Figure 3.24: Comparison of the 3rd order inter-modulation components relative to the fundamental of the LNA with and without Post-distorter at 180 MHz.

The performance of the post-distorter was also simulated with respect to frequency from 30-300 MHz. The performance is monitored at an input power level

of -12 dBm where the improvement in the 3rd order inter modulation components is maximum. The response obtained is as shown in the figure 3.25. From the plot it is observed that improvement is seen only from 90 MHz.

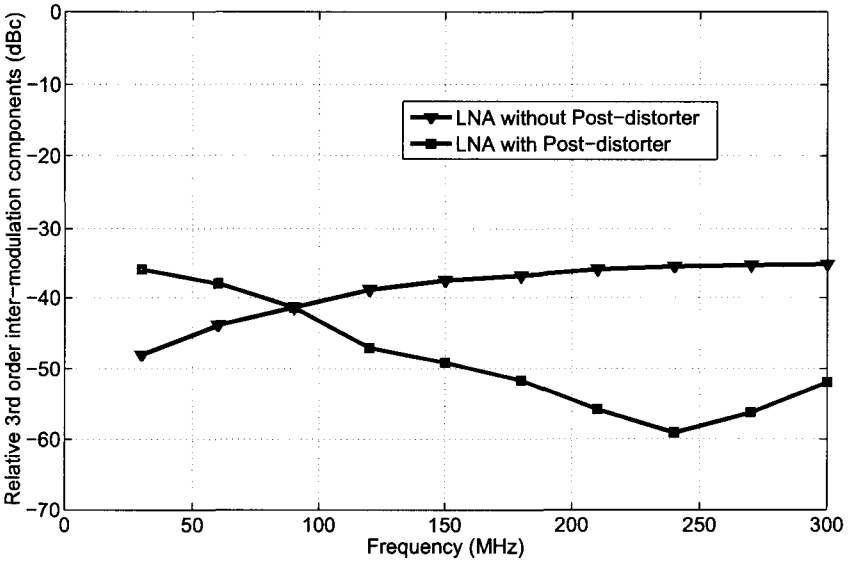


Figure 3.25: Comparison of the 3rd order inter-modulation components relative to the fundamental of the LNA with and without Post-distorter with respect to frequency at an input power level of -12 dBm.

Chapter 4

Measurement and Results

This chapter discusses the constructional details of the LNA along with the experimental set ups used for the measurement of the various parameters of the amplifier.

4.1 Construction details of the LNA

4.1.1 Amplifier card

The amplifier was realized on an ULTRALAM 2000 PCB laminate. It is a woven glass reinforced Polytetrafluoroethylene (PTFE) microwave laminate. This is designed for high reliability strip line and micro strip circuit applications. The dielectric constant of it is typically 2.4. It has a low dissipation factor, Tan (δ), of 0.0022. It can be used at frequencies as high as 10 GHz. The layout of the amplifier made using the Genesys CAD package, is shown in the figure 4.1.

4.1.2 Amplifier chassis

The passive components were selected in such a way that, their self resonance frequencies (SRF) were much higher than the frequencies at which the LNA has been designed to work. Chip resistors of RS make were used for biasing the circuit,

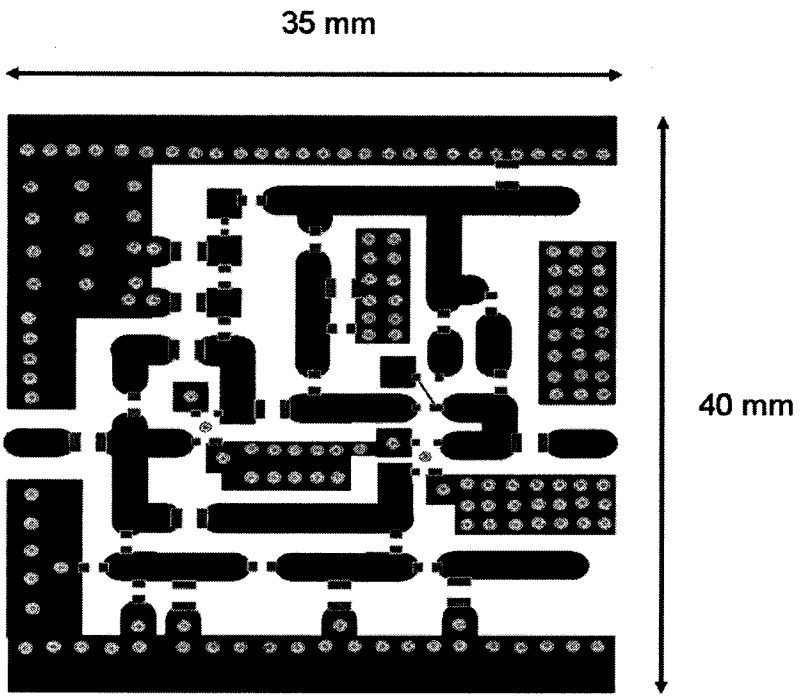


Figure 4.1: Layout of the LNA built on Ultralam card.

whereas ATC Chip capacitors were used both for coupling and bypassing RF signals. Coil craft inductors were used in the bias path for minimizing the RF leakage into DC. The entire assembled card was mounted inside a milled chassis made of aluminum. The card was gold plated in order to prevent it from getting corroded. Similarly the aluminum box was chromated to protect it from getting oxidized. The chassis fabrication drawing view of LNA is shown in the figure 4.2. The photograph of the LNA is shown in the figure 4.3

4.2 Characterization of the LNA

The amplifier was characterized for its gain, input return loss, Noise figure, 1dB compression point & OIP3. The experimental procedure for determining each one of them is discussed below.

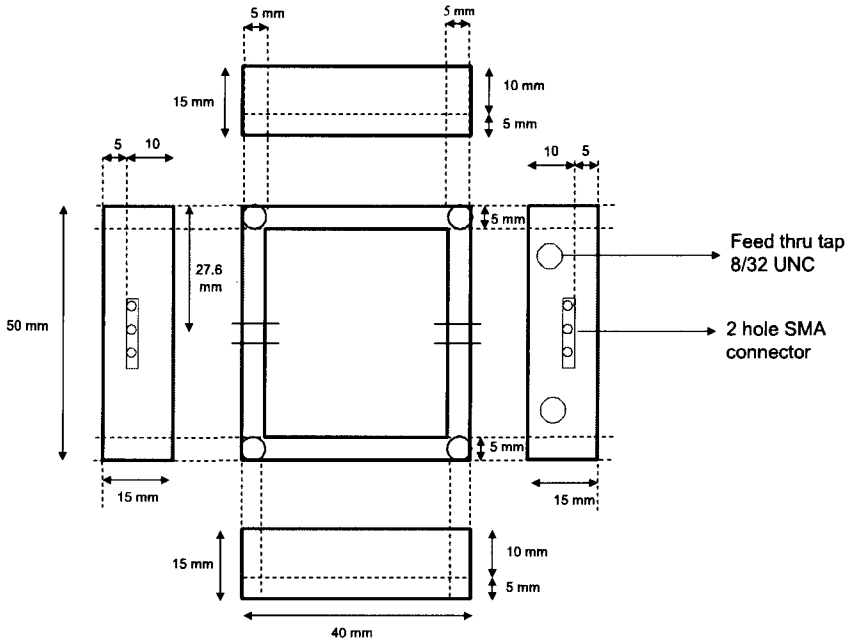


Figure 4.2: Chassis fabrication drawing of the amplifier box.

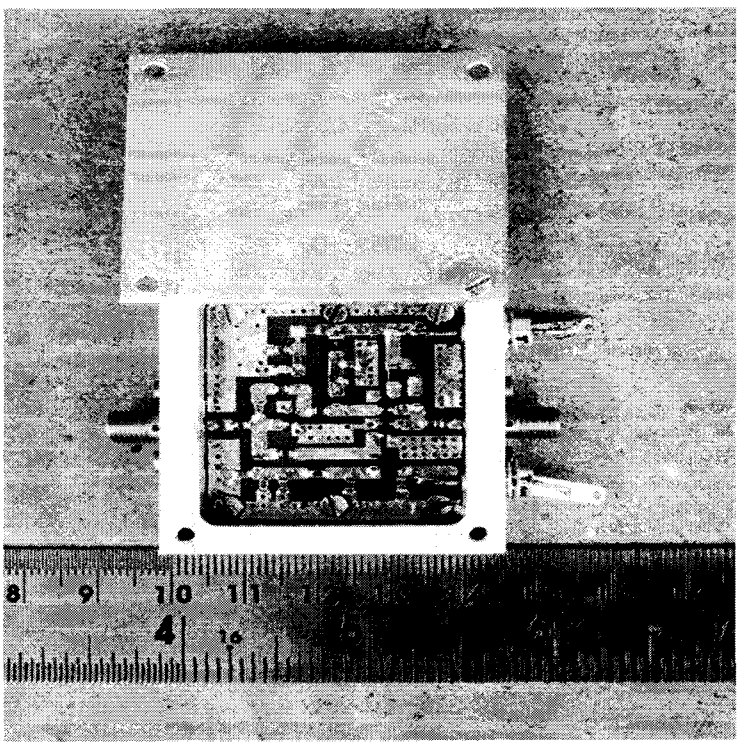


Figure 4.3: Photograph of the LNA built in lab.

4.2.1 Measurement of Gain and Input return loss of the LNA

The schematic and the photograph of the experimental set up for the measurement of gain and input return loss of the LNA are shown in the figures 4.4 & 4.5 respectively. It consists of a scalar network analyzer (HP 8757D), a synthesized sweeper (HP 83752A).

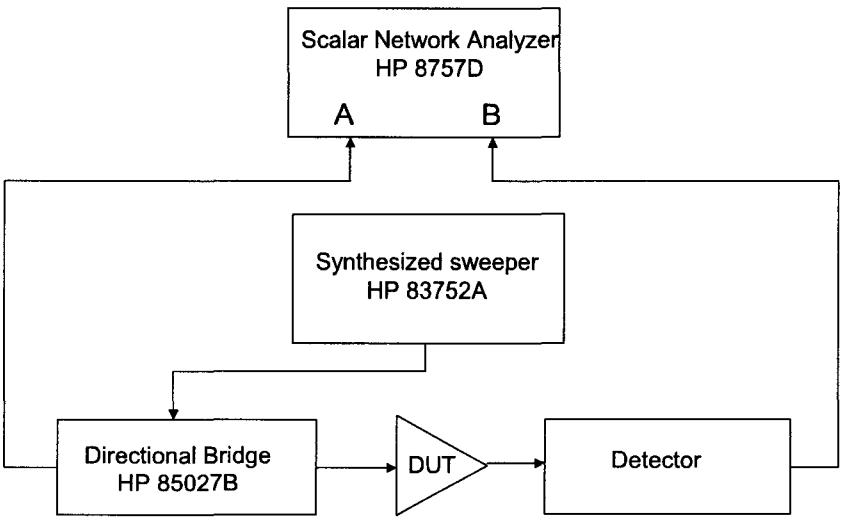


Figure 4.4: Schematic of the experimental setup used for the determination of the Gain & Input return loss.

The instrumental calibration was carried out before making the real measurement on the Device under test (DUT). After carrying out the calibration, the amplifier was connected and its gain and input return loss were measured as a function of frequency (30-300 MHz). The response obtained is shown in the figures 4.6 & 4.7 along with the simulated results.

4.2.2 Measurement of Noise figure of the LNA

Experimental setup for the measurement of Noise Figure of the LNA is shown in the figure 4.8. It mainly consists of a Noise Figure Meter (HP 8970B) and a calibrated Noise source (HP 346A). Calibration was carried out in order to remove the noise

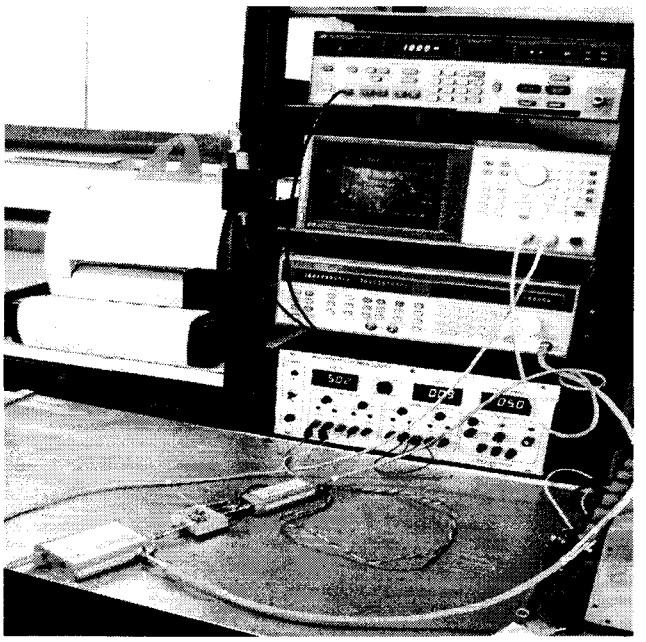


Figure 4.5: Photograph of experimental setup used for the determination of the Gain & Input return loss

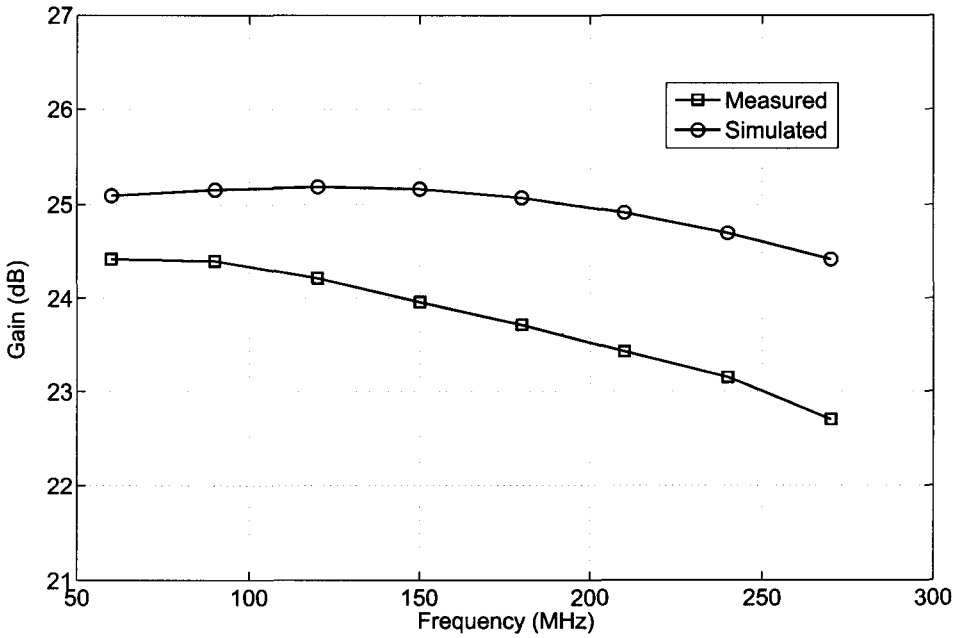


Figure 4.6: Comparison of the simulated and measured Gain of the LNA.

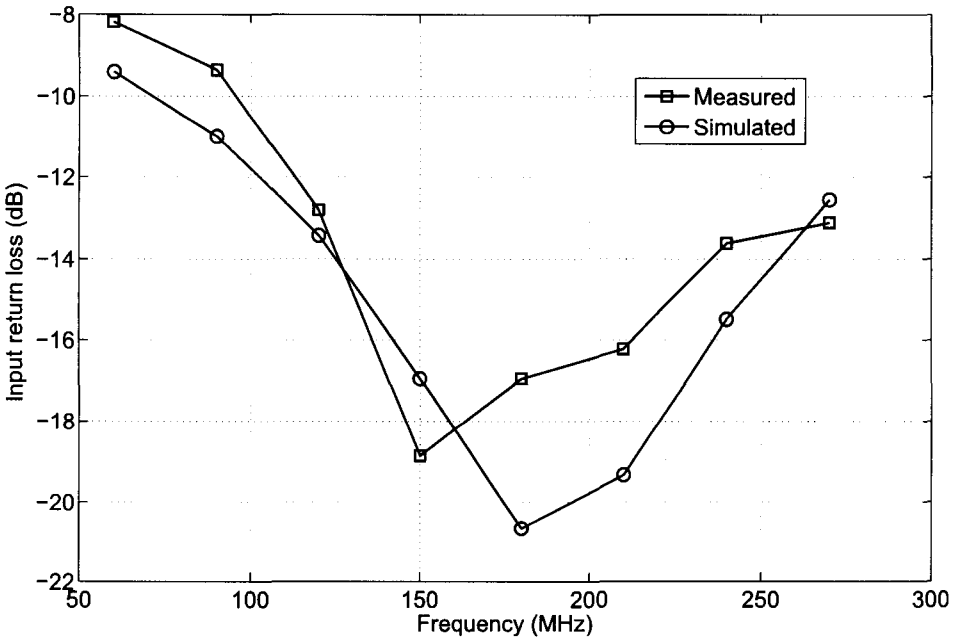


Figure 4.7: Comparison of the simulated and measured Input return loss of the LNA.

contribution from the measuring system. After calibrating, the LNA was characterized for the noise figure along the frequency region of interest. Figure 4.9 shows both the measured and simulated noise figure of the LNA.

Noise figure lower than what has been achieved using the TNC technique would have been obtained using a conventional LNA based on source degeneration technique. But as mentioned earlier this technique has narrow bandwidth and poor input impedance match for the maximum power transfer.

The simulated values appear to be lower than the measured values. This may be because of not considering the noise contribution from the input RF connector and assuming that, all the passive components used in the circuits are ideal during the process of simulation.

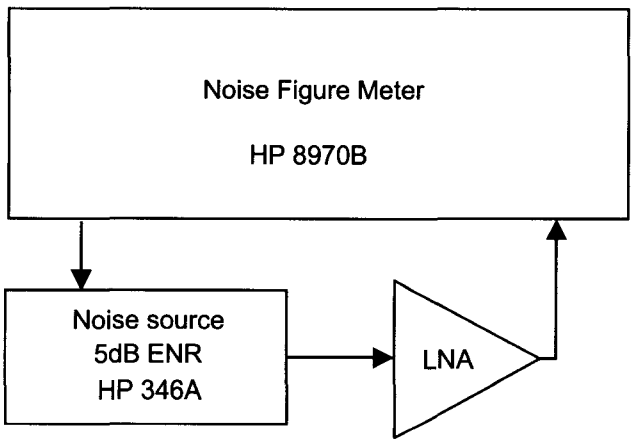


Figure 4.8: Experimental setup for the Noise figure measurement.

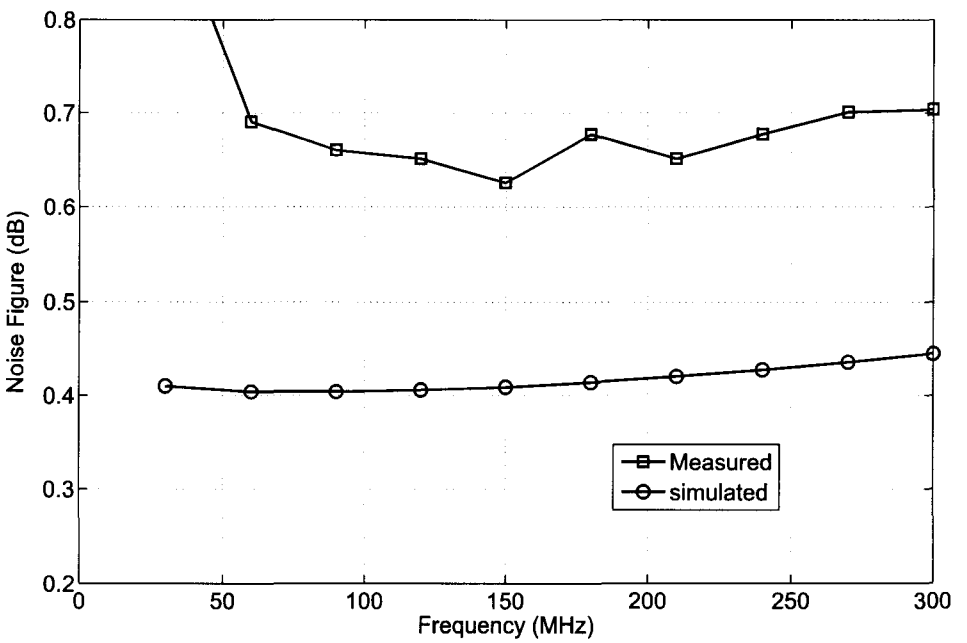


Figure 4.9: Comparison of the simulated and measured Noise figure.

4.2.3 Measurement of 1dB compression point

This experiment was done with the scalar network analyzer. The set up was the same as that used for the Gain and input return loss measurement as shown in the figure 4.4. The input power level was swept from -45 dBm to +10 dBm and the output was recorded at each power level. Output 1dB compression point was

measured to be +16 dBm.

4.2.4 Measurement of Output Third Order Intercept point (OIP3)

The experimental set up for OIP3 measurement is shown in the figure 4.10. It mainly consists two signal generators, a power combiner and a spectrum analyzer. The input power of both the two tones were increased in steps from -40 dBm to -25 dBm. At each input power level, the power levels of both fundamental and 3^{rd} order products were measured with the spectrum analyzer. The data obtained were plotted (shown in the figure 4.11) and the 3^{rd} order intercept point was obtained using the procedure as explained earlier. OIP3 was measured to be +28 dBm.

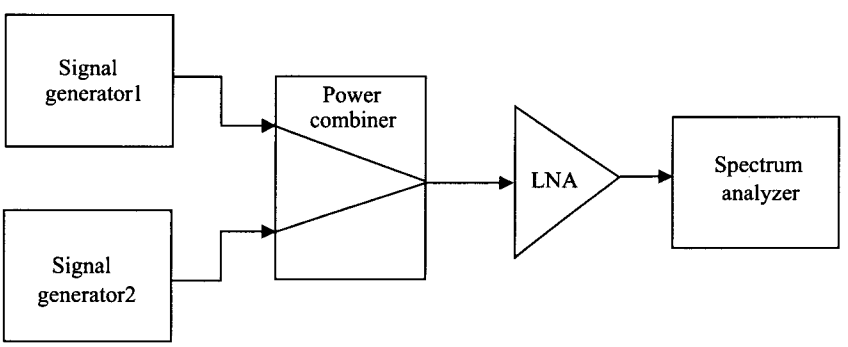


Figure 4.10: Experimental setup for the OIP3 measurement.

4.3 Measurement of LNA with post distorter

Second amplifier was built with the post distorter circuit at its output.The characterization of the amplifier for all its parameters is yet to be carried out.

The results obtained of the LNA without Post-distorter are tabulated in the table 4.1 along with targeted values

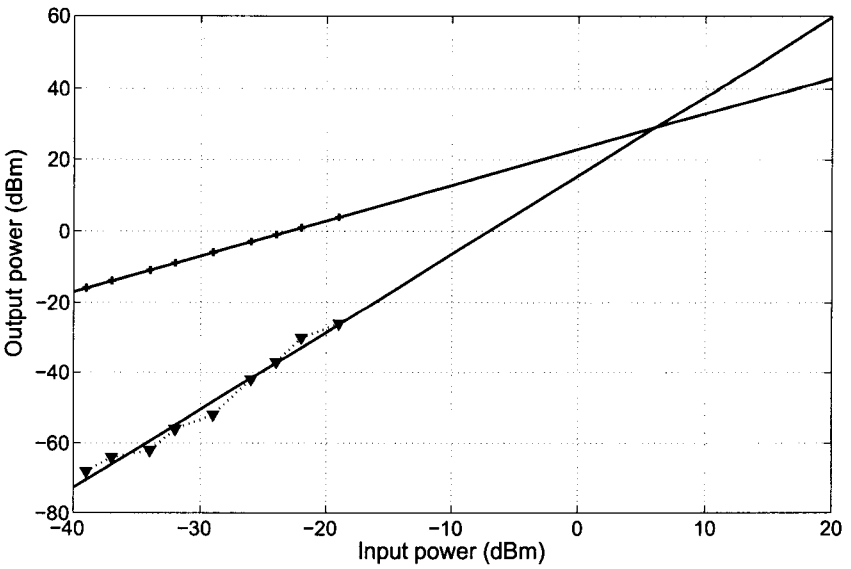


Figure 4.11: OIP3 obtained from extrapolating fundamental and 3^{rd} harmonic components.

Parameter	Targeted value	Measured value
Frequency of Operation	30-300 MHz	30-300 MHz
Noise Temperature	50 K	50 K
Gain	25 dB	24 dB
Input Return loss	$\leq$ -10 dB	$\leq$ -10 dB
OIP3	+ 20 dBm	+ 28 dBm

Table 4.1: Comparison of the Simulated and Measured performance of the LNA

Chapter 5

Conclusion

5.1 Summary

In this project, we have explored different architectures commonly used for the design of the LNA and linearizer. We have successfully adopted thermal noise cancellation technique to design a very wide band (30 – 300 MHz) amplifier having a very low noise contribution of 50 K. We have also attempted to use a post distorter to improve the dynamic range of the amplifier.

LNA without post-distorter was fabricated using ATF-54143 HEMT on Ultralam card and was characterized. The measured and simulated results matched to good extent. LNA is unconditionally stable over the entire frequency region of 30–300 MHz with an input return loss ≤ -10 dB and achieved very good Noise figure of 50 K along with very good OIP3 of +28 dBm and a gain of 24 dB.

5.2 Future Work

The Post-distorter circuit which increases the dynamic range of the LNA was designed but not characterized due to lack of time. So, the future work will project on the characterization of the LNA with post distorter circuit.

Amplifiers based on thermal noise cancellation technique can be designed with differential input, so that they can be directly connected to the balanced line from a short dipole without using any balun.

Appendix A

Input impedance of the 1st stage of the LNA

The input matching section of the amplifier is shown in the figure A.1 and its small signal equivalent is shown in the figure A.2.

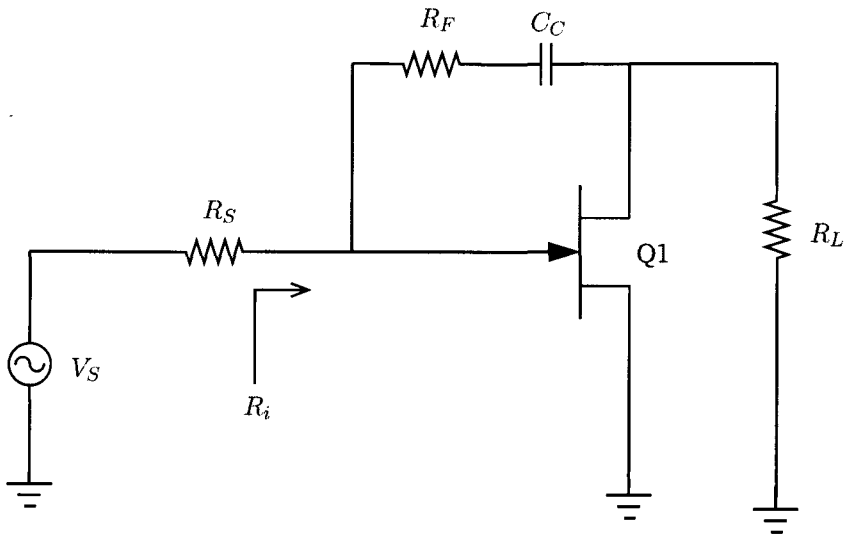


Figure A.1: input matching section of the LNA.

The input impedance of the figure A.2 can be obtained by applying a voltage,V_i, at the input, calculating the input current,I_i, and then finding the ratio of the V_i & I_i.

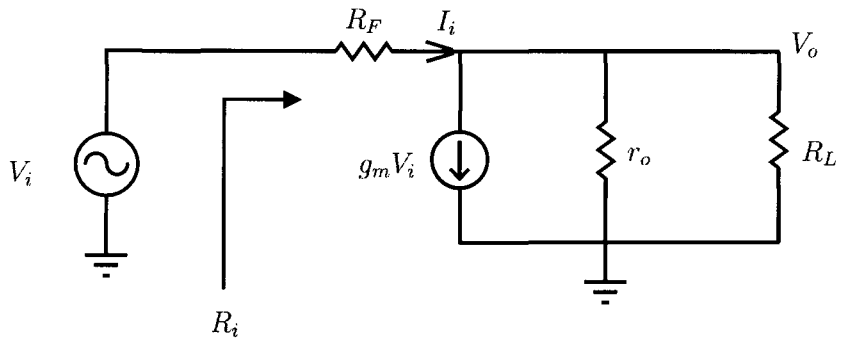


Figure A.2: Small signal equivalent circuit of the figure A.1.

Appying kirchoff's law of voltage, the relation between the V_i and V_o can be written as follows :

$$v_i = I_i R_F + v_o \tag{A.1}$$

Appying kirchoff's law of current at the node V_o we get :

$$\frac{v_o - v_i}{R_F} + g_m v_i + \frac{v_o}{r_o||R_L} = 0 \tag{A.2}$$

$$\Rightarrow v_o\Big[\frac{1}{R_F} + \frac{1}{r_o||R_L}\Big] = v_i\Big[\frac{1}{R_F} - g_m\Big] \tag{A.3}$$

$$\Rightarrow v_o = \frac{v_i[1 - g_m R_F](r_o||R_L)}{R_F + (r_o||R_L)} \tag{A.4}$$

From A.1 and A.4

$$\frac{v_i[1 - g_m R_F](r_o||R_L)}{R_F + (r_o||R_L)} = I_i R_F \tag{A.5}$$

$$\Rightarrow \frac{v_i[R_F + g_m R_F(r_o||R_L)]}{R_F + (r_o||R_L)} = I_i R_F \tag{A.6}$$

$$\Rightarrow \frac{v_i}{I_i} = \frac{R_F + (r_o||R_L)}{1 + g_m(r_o||R_L)} \tag{A.7}$$

Hence, the input impedance is

$$\boxed{\Rightarrow R_i = \frac{R_F + (r_o||R_L)}{1 + g_m(r_o||R_L)}} \tag{A.8}$$

Appendix B

Derivation of the gain, A3

The circuit diagram of the 2nd stage is shown in the figure B.1. The main parameters to be determined in the second stage are the individual gains of the transistors Q2 & Q3.

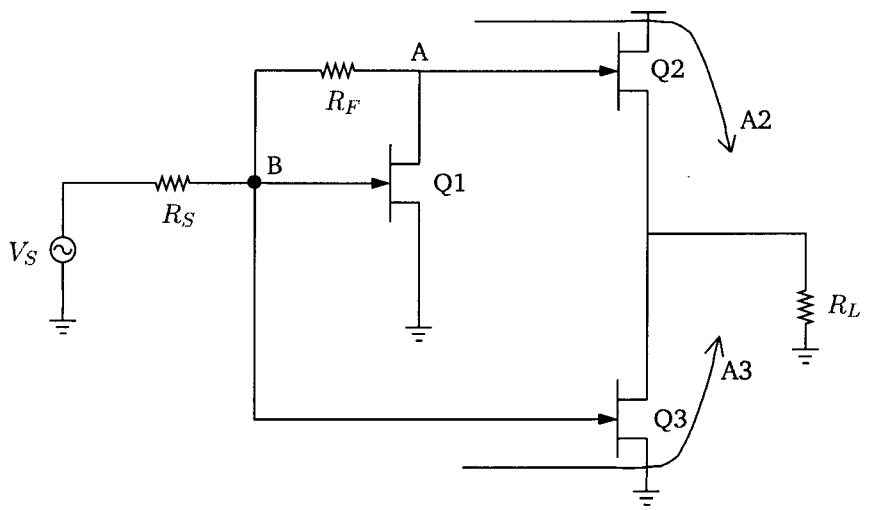


Figure B.1: schematic of the two stage LNA.

The small signal equivalent circuit diagram of the figure B.1 is shown in the figure B.2.

But, any current source which gives current in proportional to the voltage across its nodes can be replaced by a resistor, whose value is equal to the proprtionality

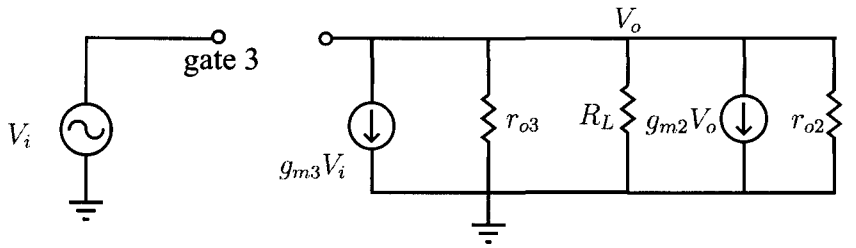


Figure B.2: schematic of the two stage LNA.

constant. Hence, the current source $g_{m2}\,V_o$ can be replaced with a resistor of '$1/g_{m2}$' Ω. The simplified circuit is shown in the figure B.3.

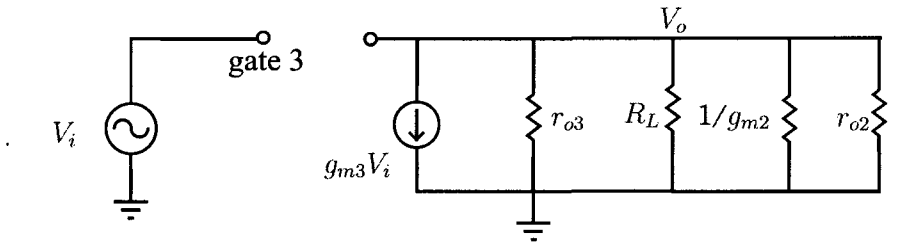


Figure B.3: schematic of the two stage LNA.

From the figure B.3, we can derive that

$$v_o = -g_{m3}v_i\left(r_{o3}||R_L||\frac{1}{g_m2}||r_{o2}\right) \tag{B.1}$$

Hence the voltage gain of transistor Q3, A3 is:

$$\boxed{A3 = \frac{v_o}{v_i} = -g_{m3}\left(r_{o3}||R_L||\frac{1}{g_{m2}}||r_{o2}\right)} \tag{B.2}$$

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