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ADFB board : Functionalities of Version 1.0 firmware

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Abstract

MWA plans to use an ADC board which is developed based on a design provided by CSIRO-ICT center for the 32 tile system. This board is referred to as Analog to Digital converter Filter Bank (ADFB) board. This report summarizes the functionalities that will be implemented in version 1.0 FPGA firmware in the ADFB board.

1 Introduction

The Analog-to-digital converter (ADFB) board, which is based on a design provided by the CSIRO-ICT center, Sydney, consists of four ADC channels. Each channel has a dual 8 bit ADC (AT84AD001B) followed by a field programmable gate array (FPGA; V4SX35). We plan to use the dual ADC to digitize two polarizations from a Tile. The four channels of an ADFB board will be connected to 4 Tiles. There will be two ADFB boards at each Receiver Node to digitize signals from 8 Tiles. In version 1.0, we will operate the ADCs at 660 MHz rate to Nyquist sample 330 MHz bandwidth. Note that the MWA operates over a frequency range of 80 to 330 MHz; the frequencies below 80 MHz are rejected using filters. The FPGA in the ADC board is programmed through an USB 1.1 interface. The local Monitor and Control (LM&C) computer reads the hardware flag and status registers in the ADFB broad through the same interface in version 1.0. The design of the firmware presented here is based on the receiver node requirements previously work out by Briggs (2006, 2007).

2 Functional blocks in the FPGA

Fig. 1 shows the functional blocks needed for version 1.0 of the MWA operations. The signal from the ADC is first "Walsh demodulated" and then fed to a 256 channel polyphase filter bank (PFB). For version 1.0, we plan to use the PFB code developed by Grant Hampson, ATNF, Australia. The output number of bits of the PFB is re-quantized to 5 bits real and 5 bits imaginary, due to the limitation in the data transport through the fiber. The number of sub-bands that needs to be selected from the output of the PFB for observations with the MWA is 24, which amounts to a total processing bandwidth of about 31 MHz. In addition, 8 more bands are selected for monitoring strong known narrow band RFI. Data from 24 selected bands from two polarizations are passed

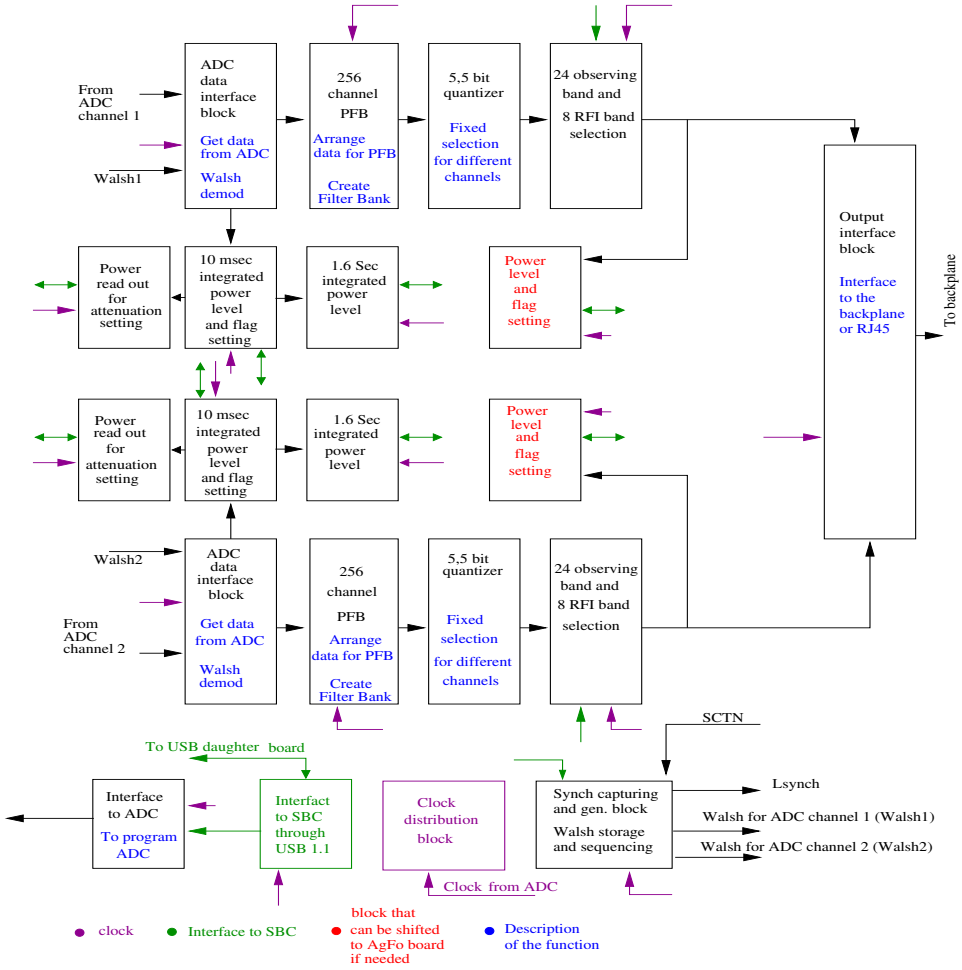

Figure 1: Functional Blocks in the V4SX35 FPGA in the ADFB board

to the back-plane or serialized and sent through RJ45 connectors to the Data Aggregation and Formatting (AgFo) board.

The receiver gain has to be adjusted to an optimum level as required by observations. For this adjustment the total power over the full bandwidth is measured using digitized samples. Integrated power for one Walsh period ($\sim$ 10 msec) will be continuously updated on a register. The LM&C can read this power estimates whenever needed and adjust gains in the SigCB (Signal Conditioning Board).

The power estimate integrated for $\sim$ 1.6 sec will be available in a register, which can be read by the LM&C. The integration time selected is ten Walsh cycles ($\sim$ 160 msec), based on considerations for system synchronization (Roshi 2007). A threshold detector will check whether the power estimated in each Walsh state (ie $\sim$ 10 msec) within the 1.6 sec has exceeded a user programmable threshold value. A flag is set if the value exceeds the threshold. The flag will be updated for each Walsh state within the 1.6 sec and cleared at the end of 1.6 sec.

The output power of each of the 32 selected sub-bands will be measured to check whether the signals are affected by RFI. A threshold detection and an associated flag will register the presence of any RFI. The flag registers can be read by the LM&C and are cleared every 1.6 sec.

The data from the 24 observing bands of the 2 polarizations are multiplexed and sent to the AgFo board. The data will be sent either through the back-plane or serially through a RJ45 connector.

The Walsh sequence for the Tile connected to an ADC is downloaded to a register from the LM&C. Since the Walsh sequence is generated using a clock locked to the sampling clock and synchronized to SCTN (see Roshi 2007), the sequence can be regenerated in the FPGA from the Walsh states stored in the register. We plan to generate the Lsynch signal (see Roshi 2007) within the FPGA, which determines the boundary of the Walsh cycle. The Lsynch generated in the ADFB board will be synchronized to the SCTN signal, which is provided to the ADFB board from the clock and synchronization signal. The Walsh states in the FPGA are generated and synchronized with the Lsynch. In version 1.0, we use this method to generate Walsh signal for demodulation in the FPGA.

The ADC has several programmable modes. The mode of the ADC required for the MWA observations will be programed from the FPGA. In version 1.0 the mode selection will be fixed and cannot be controlled from the LM&C.

3 Output Data Rate from the ADFB board

The data from the 24 frequency channels selected for observations will be sent to the AgFo (Aggregation and Formating) board. With 10 bits for each frequency channel, total data rate from a FPGA in the ADFB board is about 620 Mb/sec. This data rate includes the transmission of data from both polarizations connected to one ADC.

4 Reset command and FPGA configuration

A reset command (see Fig. 2) from LM&C will initialize all the receiver node electronics. On the reception of the reset command, the LM&C will download the FPGA codes in the ADFB and AgFo boards. After downloading, the FPGA will program the ADC and reset the ADC so that the data starts flowing from the ADC. A state machine, described in Section 5, then takes over the control of the operations in the FPGA.

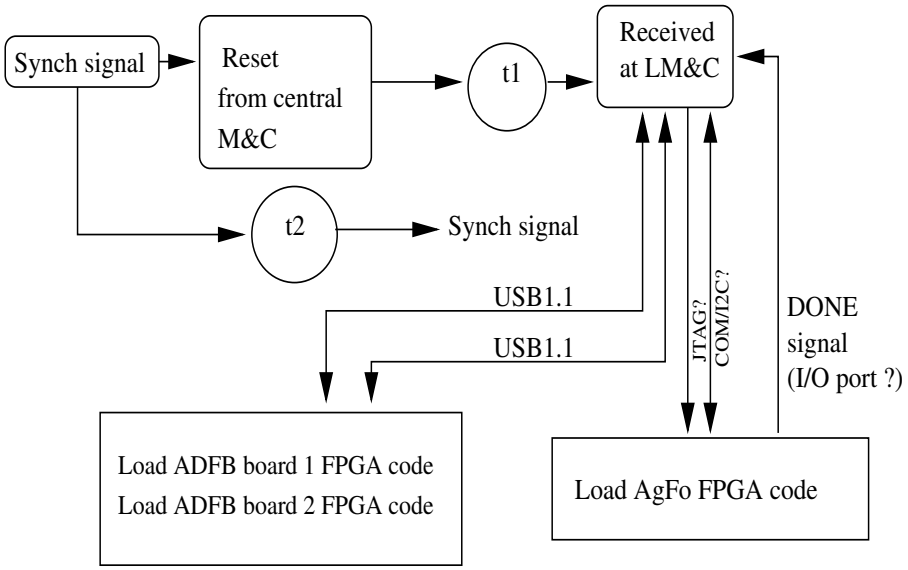

Figure 2: Functions of the Reset command

5 ADFB state machine

The state machine in the ADFB is designed such that the data starts flowing continuously after the FPGA code is loaded. The state machine is resynchronized every $\sim$ 8 sec with the SCTN signal provided by the clock and synchronization circuit (see Roshi 2007). The actions for different states are given in Fig. 3.

After loading the FPGA code from the LM&C the state machine enters the state I0. In this state, the ADCs are programmed as required for MWA observations. After programming the ADC, the machine makes a transition to state S0 where it waits for the next SCTN signal. The power registers, flag registers and PFB output filter banks are either reset or preset. At the rising edge of SCTN, the machine makes a transition to state S1. The operations that will be done at this state are (a) to get the Walsh state; (b) set the multiplication factor for Walsh demodulation corresponding to the present Walsh state and (c) check whether the machine has reached state S1 by skipping some of the states and, if so, set a flag indicating the loss of synchronization. The state transition to S2 takes place at the rising edge of next Lsynch, where the machine waits for a predefined delay before the start of the power estimate. After the delay, a square law detector will estimate the power with an integration of $\sim$ 10 msec.

The transition from S3 to S4 happens if the Walsh cycle is not complete. At S4, the 10 msec integrate power is passed to another accumulator for 1.6 sec integration. A threshold detection for RFI at the outputs of ADC and the selected 32 bands of the PFB are made. Flags are set if RFI is present. At the end of Walsh cycle, state S3 changes to S5. In addition to the actions done at S4, the Walsh pattern stored in a register by the LM&C is used to reset the Walsh state generation. If there is any slip in the generated Walsh state, then a flag is set.

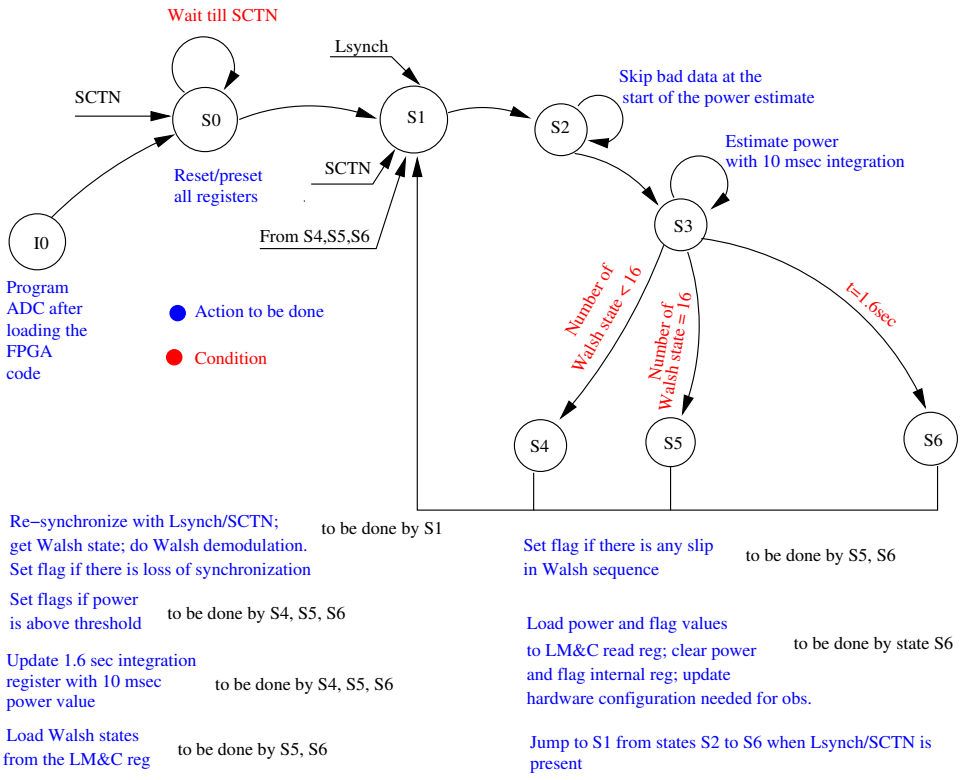

Figure 3: State machine in the ADFB board FPGAs

As discussed in Roshi (2007), a 1.6 sec cycle is needed for the LM&C-hardware interaction. At the boundary of this cycle, which is indicated by state S6, the content of power and flag registers are transferred to another register from which the LM&C can read the values. After transferring, the internal registers are cleared for the next 1.6 sec cycle operations. The 1.6 sec cycle is synchronized with the SCTN signal.

6 Updating hardware configuration for observations

The MWA users need to select the 24 frequency bands for observations and 8 RFI bands for monitoring. In version 1.0, the selection of these bands will take place without interrupting the data flow. Fig. 4 shows a block diagram for filter bank selection. Every 1.6 sec the state machine checks for configuration updates and, if requested, new sub-bands will be selected.

7 Hardware registers accessible to LM&C

The registers that are accessible to LM&C are shown in Fig. 5. Note that in Fig. 5 registers for one polarizations are shown. A similar set of registers for the second polarizations is required. There are three configuration registers that need to be updated by the LM&C for observations. They are the Walsh storage register, addresses of the PFB output banks and the thresholds for RFI flag setting. The flag registers needed for version 1.0 are shown in Fig. 5. A 10 msec integrated power estimate is available in an output register for gain adjustment. For monitoring the health of the analog system a 1.6 sec integrated power estimate is also available in an output register. In addition, a

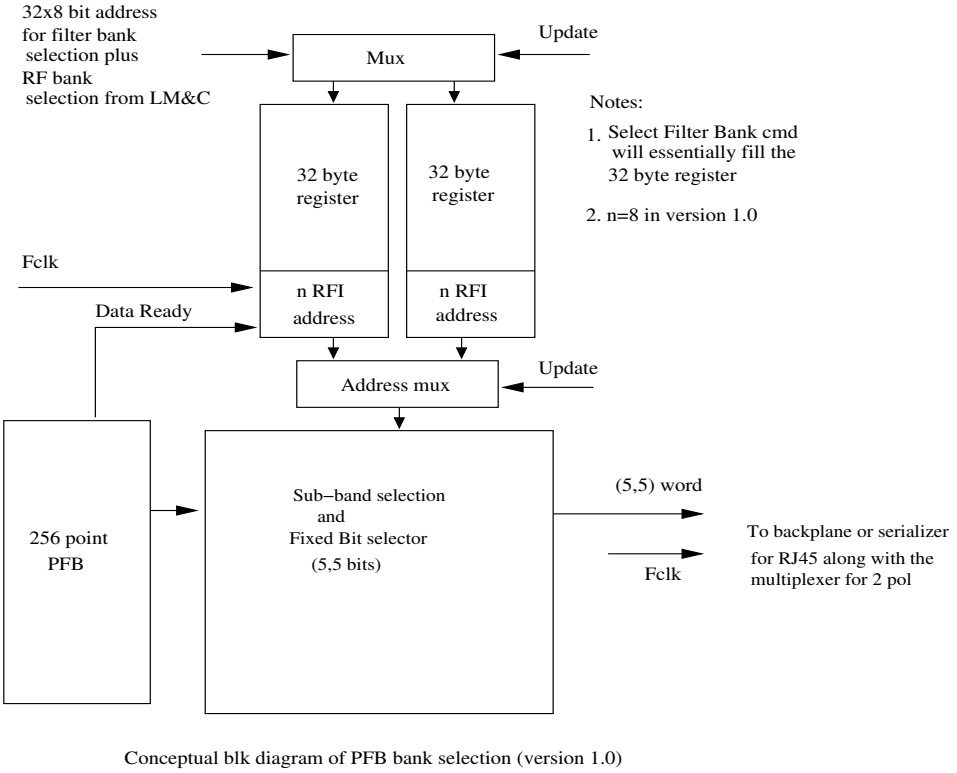

Figure 4: Filter bank selection block in the ADFB board FPGA

register holding either the temperature and voltage values or flags to show excess/low values will be available. The total number of bytes that has to be written to the FPGA for configuration of ADFB is 133. For gain adjustment a 3 byte power value for each polarization has to be read from the FPGA. Every 1.6 sec, 11 bytes per polarization corresponding to the power estimate and flags has to read by the LM&C.

Acknowledgment

We thank the CSIRO-ICT center, Sydney, for providing us with a 4 channel ADC design, which formed the basis for the ADFB board design. We plan to use this design for the 32 T system of the MWA. We thank Grant Hampson for providing his PFB code, which will be used in version 1.0 of the ADFB board.

Reference

Briggs, H. F, August 2006, MWA Knowledge Tree
Briggs, H. F, 14 January 2007, MWA Knowledge Tree
Roshi, D. A, June 2007, MWA Knowledge Tree (to be submitted; draft available)

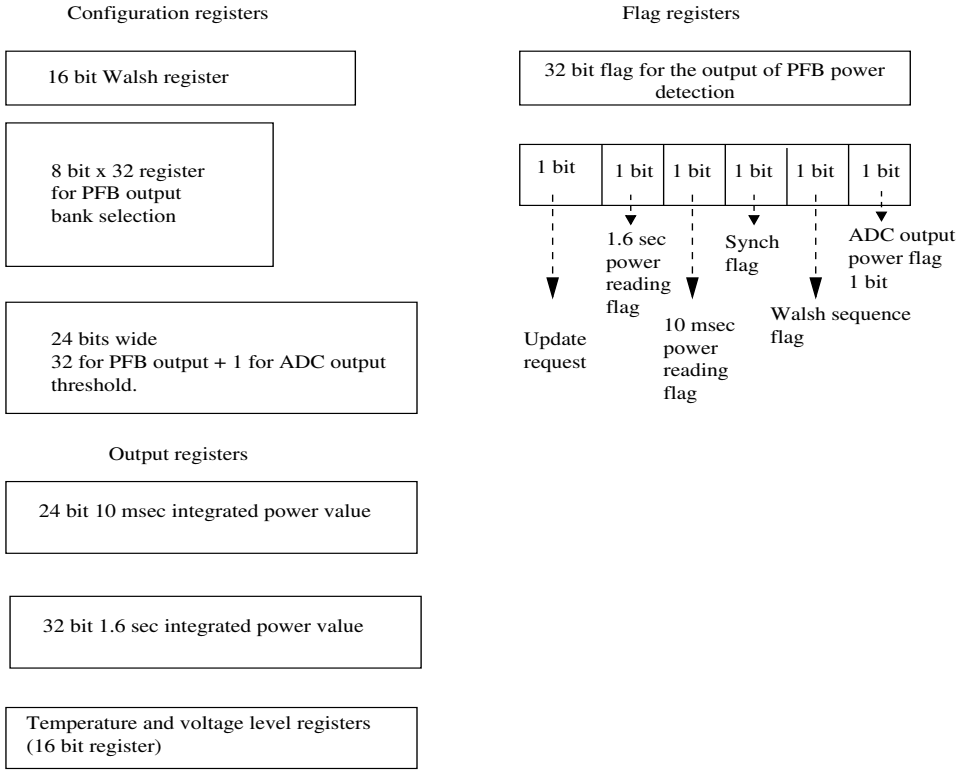

Figure 5: Diagram shows the registers in the FPGA for one polarization accessible for LM&C

Revision History

V1.0 – June 11, 2007
V1.01 – Decided to use the SCTN, instead of Lsynch, as the basic synchronization signal for the ADFB board. This is because the power measurement has to be synchronized with the SCTN signal. Lsynch will be generated inside the FPGAs in the ADFB board using the SCTN signal. This Lsynch along with the Walsh pattern stored in a register in the FPGA will be used to generate the Walsh sequence for the demodulation.