P-177: Multi-line Addressing of LCDs with Simple Diagonal Matrices

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Abstract
A multi-line addressing technique that is based on diagonal matrices is demonstrated. Number of time intervals to complete a cycle is independent of the number of address lines that are selected simultaneously. Good brightness uniformity is achieved among pixels that are driven to the same state.

1. Introduction
Multi-line addressing techniques are extensively used to drive passive matrix liquid crystal displays (LCDs) in portable products like cell phones and other portable gadgets. Selecting an orthogonal matrix is the first and most important step in multi-line addressing. Cross talk free multiplexing of data to pixels is possible when the matrix display is scanned with waveforms derived from orthogonal functions or matrices. Let us consider a matrix display with N rows and M columns. The N rows are grouped into (N/s) sets with s rows in each set. During a particular interval of time called as select time, rows in a set are selected by applying voltages that are proportional to the elements of a select vector i.e., column of the orthogonal matrix. Rows in the other sets are connected to the non-select voltage (zero). Data vector represents the state of the pixels in the selected rows of a column. Voltages that are proportional to the dot product of the select vector and the data vectors are applied to the columns of the matrix display simultaneously during the application of the select voltages. The manner in which the subgroups are selected with all the select vectors differs and is called scanning sequence. A cycle or frame is completed when all the subgroups are selected once with all the select vectors. Time to address a single frame is called the frame time and it is much smaller than the response time of pixels in RMS responding displays like twisted nematic and super twisted nematic displays. The frame time should be short enough to avoid flicker in the display. Good brightness uniformity among pixels that are driven to the same state, high address duty cycle, and low supply voltage are some of the advantages of multi-line addressing (MLA) techniques.

2. Objective and Background
Walsh function [1], Hadamard matrices [2], wavelet [3] are used in multi-line addressing. Number of time intervals to complete a cycle is greater than N if the number of address lines that are selected simultaneously i.e., s is not of the form 2^i or $4 \cdot i$ where in i is an integer, because both Walsh functions and Hadamard matrices do not exist if this condition is not met by s. Hence, one is forced to use higher order matrices that result in increase in number of time intervals. For example, the number of time intervals to complete a cycle is $((8N)/5)$ i.e. 60% higher if five rows are selected simultaneously when Walsh functions or Hadamard matrix of order 8 is used for selecting the rows. Simple orthogonal matrices were proposed for multi-line addressing [4] and it is demonstrated in the present work.

3. Addressing the Matrix LCD
The multi-line addressing technique that uses the diagonal matrices is described in this section. Elements of the diagonal type orthogonal matrices of order s to select s number of rows simultaneously satisfy the following condition:

$$\frac{d}{r} = -\frac{(s-2)}{2} \tag{1}$$

Wherein d is the diagonal element and r is the non-diagonal element in a matrix of order s as proposed in [4].

3.1 Technique
The technique is demonstrated by selecting six address lines (rows) simultaneously with waveforms derived from the orthogonal matrix shown in (2).

$$\begin{bmatrix} -2 & 1 & 1 & 1 & 1 & 1 \\ 1 & -2 & 1 & 1 & 1 & 1 \\ 1 & 1 & -2 & 1 & 1 & 1 \\ 1 & 1 & 1 & -2 & 1 & 1 \\ 1 & 1 & 1 & 1 & -2 & 1 \\ 1 & 1 & 1 & 1 & 1 & -2 \end{bmatrix} \tag{2}$$

Number of time intervals to complete a cycle is reduced by 25% as compared to selecting 6 address lines with either Walsh functions or Hadamard matrix of order eight. The technique for displaying bi-level images using the diagonal matrix is similar to the multi-line addressing technique described first. Let us consider a matrix display with 32 scanning electrodes (rows) and 32 data electrodes (columns). Six scanning electrodes are grouped together to form a set, the two rows that are left out at the end of forming 5 sets of rows can be combined with 4 dummy rows that are not physically connected to the display because 32 is not an exact multiple of 6. Performance of the display will not be affected if zero is assigned as the data to the pixels in the dummy rows. The display is scanned by selecting one set of rows at a time with voltages that correspond to the elements of a select vector. The rows in the non-selected sets are grounded. Data voltages that are proportional to the dot product of select and data vectors are also applied simultaneously to the column (data) electrodes. A set of rows is selected with all the select vectors before moving onto the next set of rows. A scan is complete when all the sets of rows are selected with all the select vectors. The display is scanned continuously by repeating the cycle at about 50 Hz to display images without flicker. Polarities of the addressing waveforms i.e. sign of the select and data voltages are reversed periodically to achieve dc free waveforms across the pixels in the display. Addressing waveforms that are applied to the matrix display during a frame are shown in Figure 1. The waveforms across the pixels are also shown in the figure. Mathematical analysis of the addressing technique is presented in the next section.

3.2 Analysis

Liquid crystal displays respond to root-mean-square (RMS) voltage and the RMS voltage across the pixels in the display is arrived at in the following analysis. Let the unit amplitude of the select voltages be V_r so that five rows in a set of rows are selected with $\pm V_r$ and one of the rows in the set is selected with a voltage $\mp 2 \cdot V_r$. Similarly, let the unit voltage for data voltage be V_c, and any one of eight voltages i.e. $\pm V_c, \pm 3 \cdot V_c, \pm 5 \cdot V_c, \pm 7 \cdot V_c$ in the set is applied to the columns. For example, the data voltage is $\pm 3V_c$ during the six time intervals when all the pixels in the selected rows are either OFF or ON. The data voltage will have the same sign as that of the select voltage when all the six pixels in the selected rows are OFF and it will have opposite sign of the select voltage when all the pixels are ON. The RMS voltages across the ON and OFF pixels are shown in the following equations:

$$V_{ON} = \sqrt{\frac{5\left(V_r + 3V_c\right)^2 + \left(2V_r - 3V_c\right)^2 + \left(\frac{N}{6} - 1\right) \cdot 54V_c^2}{N}} \tag{3}$$

$$V_{ON} = \sqrt{\frac{9V_r^2 + 18V_rV_c + 9NV_c^2}{N}} \tag{4}$$

Similarly, the RMS voltage across OFF pixel is given in the following equation.

$$V_{OFF} = \sqrt{\frac{5\left(V_r - 3V_c\right)^2 + \left(2V_r + 3V_c\right)^2 + \left(\frac{N}{6} - 1\right) \cdot 54V_c^2}{N}} \tag{5}$$

$$V_{OFF} = \sqrt{\frac{9V_r^2 - 18V_rV_c + 9NV_c^2}{N}} \tag{6}$$

In mathematical terms, selection ratio is defined as the ratio of RMS voltage across ON pixels to that across OFF pixels. It is a maximum when the amplitude of select and data voltages satisfies the following condition.

$$\frac{V_r}{V_c} = \sqrt{N}\ . \tag{7}$$

The maximum selection ratio of this technique is as follows:

$$\frac{V_{ON}}{V_{OFF}} = \sqrt{\frac{\sqrt{N}+1}{\sqrt{N}-1}} \tag{8}$$

It is also the maximum attainable by any addressing technique for driving passive matrix LCDs. Supply voltage is determined by the maximum swing in the addressing waveforms. To ensure a good contrast in the display, OFF pixels are biased near the threshold voltage of the LCD and supply voltage of the driver circuit is obtained by equating the expression of RMS voltage across OFF pixels to the threshold voltage of electro-optic response of LCD as shown in (9).

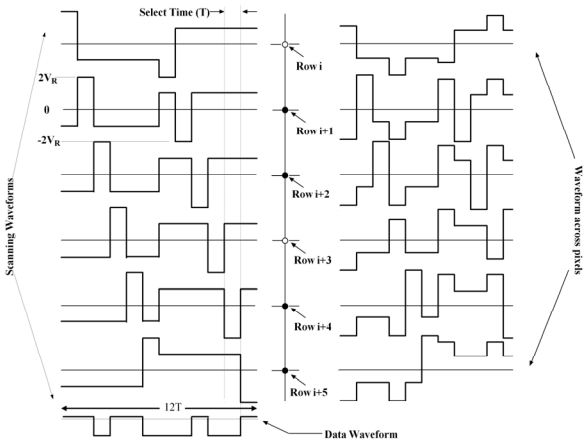

Figure 1. Typical addressing waveforms with polarity inversion for DC free operation when six rows are selected simultaneously.

$$V_{OFF} = \sqrt{\frac{9V_r^2 - 18V_rV_c + 9NV_c^2}{N}} = V_{threshold} \tag{9}$$

Hence, $V_C = \dfrac{V_{threshold}\sqrt{N}}{3 \cdot \sqrt{2(N - \sqrt{N})}}$ (10)

Once V_C is known, supply voltage can be determined. Supply voltage is $14 \cdot V_c$ when N is less than or equal to 12 and it is $4 \cdot \sqrt{N} \cdot V_c$ for N greater than 12. Supply voltage is reduced by shifting the row and column waveforms during one of the two polarities (either negative or positive) of addressing waveforms. It is similar to that for the line-by-line addressing in reference [5]. The expression for the reduced supply voltage is given in equation (11). Supply voltage, which is the maximum swing in the addressing waveforms, is defined for 3 ranges of N because maximum swing in the scanning waveforms is small as compared to data voltages when N is small and it is higher than data waveforms when N is large.

$$V_S = \begin{cases} 14V_C & \text{for } 2 \le N \le 12 \\ 7V_C + 2\sqrt{N} \cdot V_C & \text{when } 13 \le N \le 50 \\ 3\sqrt{N} \cdot V_C & \text{for } \quad N > 50 \end{cases} \tag{11}$$

Supply voltage of the level shifted waveforms is just 75% as compared to the original waveforms when the number of rows that is multiplexed (N) is greater than 50. Typical level shifted waveforms when six rows are addressed using diagonal matrix are shown in Figure 2. Select and non-select waveforms in multiplexed displays with more rows are shown in Figure 3.

4 Implementation

The block diagram of the prototype is shown in Figure 4. An EPROM is used to store the images. Brief description of the blocks is given in the following text.

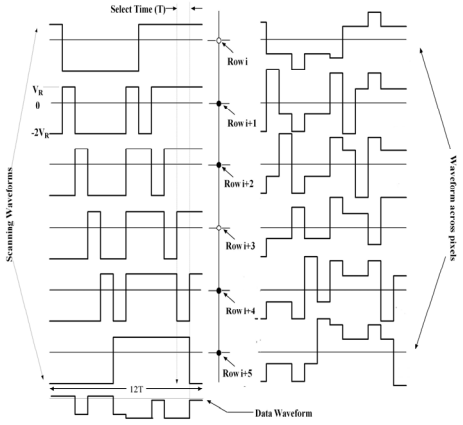

Figure 2. Level shifted waveforms to reduce supply voltage and yet achieve DC free operation (six rows are selected simultaneously.

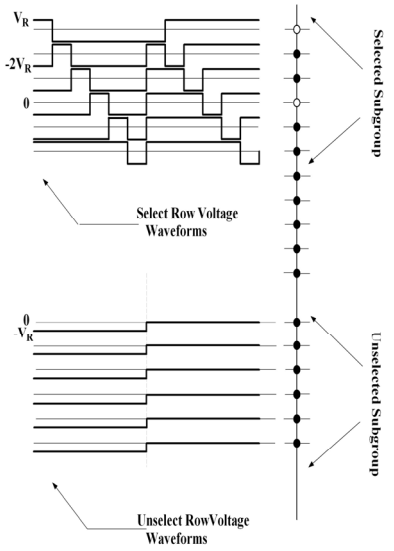

Figure 3. Select and non-select waveforms that are applied to set of rows in a multiplexed display when the voltages are shifted to reduce supply voltage.

4.1 Row Driver

Row waveforms have four voltages but only three of them are applied simultaneously because just one non-select voltage is sufficient at any given instant of time. The non-select voltage itself is selected using a 2:1 multiplexer that is common to all the stages of row drivers as shown in Figure 5.

4.2 Column Driver

Total of 16 different voltages are needed to drive the columns of the matrix display. Of these 8 voltages are used depending on the polarity of the select pulses in the addressing waveforms. A standard column driver with 3-bit shift registers, 3-bit latches, and 8:1 multiplexers that is capable of applying any 1-of-8 voltages is used. Eight 2:1 multiplexers that are common to all stages of column driver select the eight voltages to be applied to the drivers

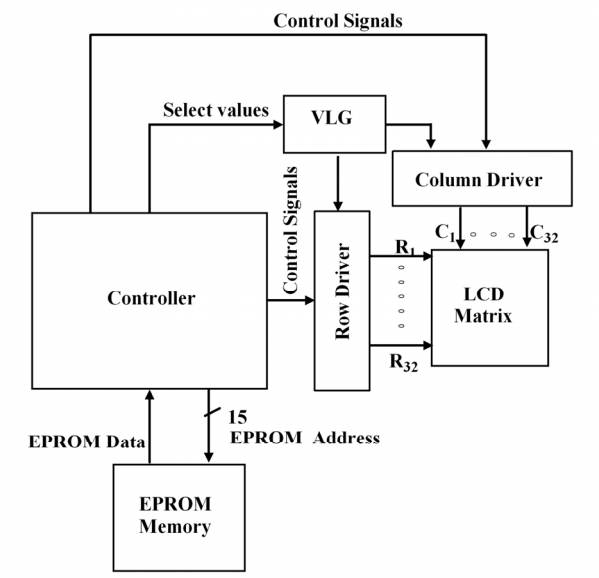

Figure 4. Block diagram of the prototype.

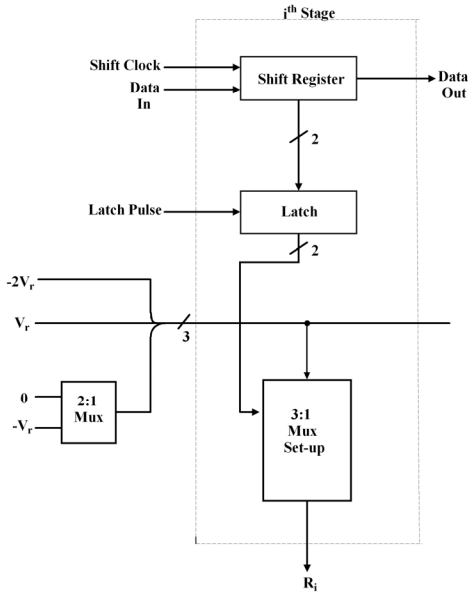

Figure 5. Schematic of row driver that is capable applying four voltages using 3:1 analog multiplexers at each stage and a 2:1 analog multiplexer that is common to all the stages of row driver circuit.

depending on the polarity of the driver waveforms as shown in Figure 6 instead of using drivers that can select 1-of-16 voltages.

4.3 Voltage Level Generator

The voltage level generator is a potential divider circuit wherein all the twenty voltages of the addressing waveforms are generated with appropriate choice of resistors. It contains eight 2:1 multiplexers to select from 16 different voltages and provides only 8 voltages to the column driver. It also contains a 2:1 multiplexer and provides 3 different voltages to the row driver.

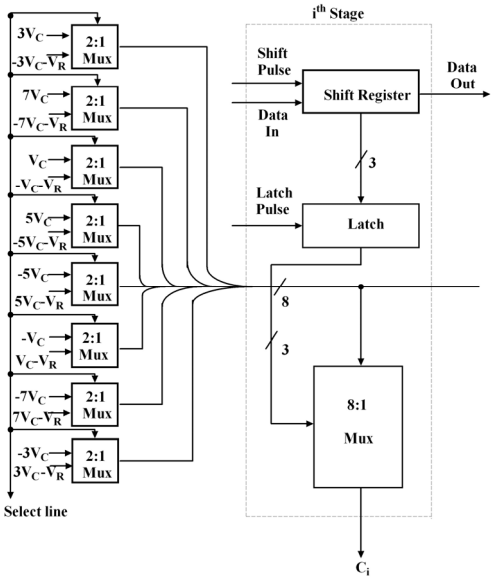

Figure 6. Schematic diagram showing one stage of column driver circuit along with common multiplexers that are used to reduce the hardware complexity of the column driver circuit.

4.4 Controller

The controller accesses the image data in the memory and generates the control signals that are necessary to apply row and column waveforms to continuously scan and refresh the display. The controller is logically divided into 3 parts; viz., column signal generator, row signal generator and the control circuit. The column signal generator provides the data to be shifted into the column driver and it is obtained with the select and data vectors. The data that is shifted in to the column driver is a 3-bit code that represents the voltage that is to be applied to a column in the matrix display. The row signal generator sends a 2-bit code that represents the select and non-select voltages that are applied to the rows of the matrix display. The control section consists of counters and logic circuit to generate all the control signals that are necessary to scan the display. It has been implemented on a CPLD with 256 logic cells. Photographs of the prototype are shown in Figure 7 and typical waveforms captured using an oscilloscope are shown in Figure 8.

5. Acknowledgements

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6. References

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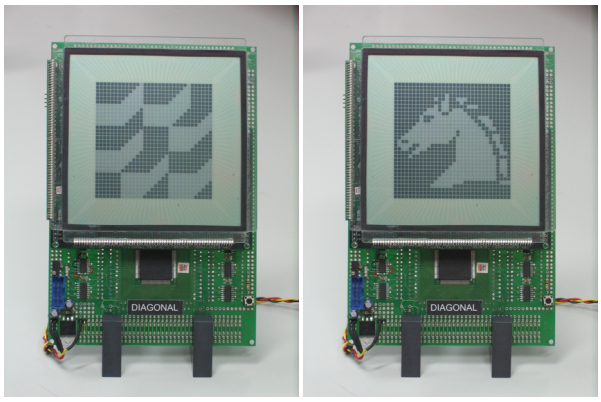

Figure 7. Photographs of the display that demonstrates the multi-line addressing technique that is based on the diagonal matrix.

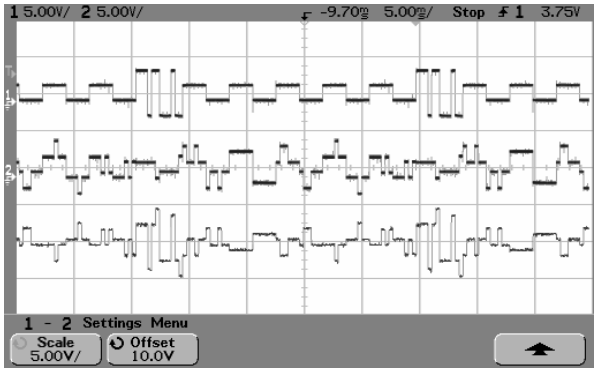

Figure 8. Typical addressing waveforms: row waveform, column waveform and waveform across a pixel respectively from the top. The waveforms have been level shifted to reduce the supply voltage of the driver circuit.

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