

# Power Dissipation in Multi-Line Addressed Liquid-Crystal Displays

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**Abstract**—Power dissipation in the driver circuit of liquid-crystal display is analyzed when the display is scanned with a multi-line addressing (MLA) technique that is based on Rademacher functions. We have considered the binary addressing technique (BAT), hybrid addressing technique (HAT), and improved HAT (IHAT) to obtain, the extreme as well as the average, power dissipation in the driver circuit. Closed-form expression for power dissipation is also obtained for these techniques; when the number of transitions in the addressing waveforms is forced to be independent of the state of the pixels by introducing duty cycle in select and data pulses. An improvement in the brightness uniformity can be achieved among pixels that are driven to the same state without increasing the average power dissipation by introducing duty cycle in the addressing waveforms.

**Index Terms**—Addressing, displays, duty cycle, liquid-crystal displays (LCDs), matrix addressing, multiplexing.

## I. INTRODUCTION

MULTI-LINE addressing (MLA) techniques for driving liquid-crystal display (LCD) have lower supply voltage, better brightness uniformity of pixels and higher contrast ratio (due to suppression of frame response) as compared to the conventional line-by-line addressing technique [1]. Binary addressing technique (BAT) [2] is the first multi-line technique that selects all the address lines with waveforms that are derived from the Rademacher functions. Both the hybrid addressing technique (HAT) [3] and improved hybrid addressing technique (IHAT) [4] are extensions of the binary addressing to drive displays with a large number of address lines. LCD is extensively used in portable products because it consumes less power as compared to many other flat panel displays. Power consumption of multiplexed LCD that is scanned with the conventional line-by-line addressing was analyzed by Marks [5]. Our objective is to analyze the power dissipation in the driver circuit of displays that are addressed with BAT, HAT, and IHAT. Brightness nonuniformity, due to distortions in the addressing waveforms, can be reduced by forcing the voltage across the pixels to zero for a short duration of time at the beginning or end of the select time [6], [7]. Therefore, we have also estimated the power dissipation of BAT, HAT, and IHAT when such duty cycle control is introduced in them. The three addressing techniques are reviewed briefly, before presenting the analysis of power consumption.

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## II. BRIEF REVIEW OF THE ADDRESSING TECHNIQUES

### A. Binary Addressing Technique (BAT)

The state of the pixels in a column of the matrix display corresponds to a binary pattern when they are driven to either ON or OFF state. Hence, all the rows in the matrix display are selected with voltages corresponding to an  $N$ -bit binary pattern. Column (data) voltage is obtained by comparing the select and data patterns such that the voltage is favorable to maximum number of pixels in the column as explained in [2] and [7]. The  $N$  rows are selected with voltages corresponding to all the  $2^N$  binary patterns (equivalent to a set of  $N$  Rademacher functions) to complete a cycle. BAT has several advantages like simple driver circuit, lowest supply, etc. However, number of time intervals in a cycle increases exponentially with  $N$  and hence, it is not useful for large  $N$ .

### B. Hybrid Addressing Technique (HAT)

It extends the binary addressing technique by selecting a few rows ( $s$ -rows) at a time with voltages corresponding to a binary pattern while remaining  $(N - s)$  rows are not selected as in the line-by-line addressing. A cycle is complete when all the sets of rows ( $N/s$ ) each consisting of  $s$  rows are selected with  $2^s$  binary patterns. Number of time intervals  $2^s(N/s)$  to complete a cycle is small as compared to  $2^N$ . Both the BAT and HAT have a lower selection ratio (ratio of RMS voltage across ON pixels to that across OFF pixels) because the number of voltages in the data (column) waveforms is limited to just two. Number of rows that is selected simultaneously in BAT and HAT is odd because the data voltage is decided by a majority decision.

### C. Improved Hybrid Addressing Technique (IHAT)

The IHAT is same as the HAT, except for the column waveforms that has  $(s + 1)$  voltages as compared to 2 in HAT. This improves the selection ratio, and IHAT is the first multi-line addressing technique that has the maximum selection ratio that is achievable by any addressing technique. Moreover, the value of  $s$  can be odd or even in this technique. Supply voltage of the driver circuit can be reduced with a proper choice of  $s$ , the number of lines that are selected simultaneously. The supply voltage is a minimum when  $N = s^2$ . Steps involved in refreshing matrix displays with BAT, HAT, and IHAT i.e., MLA techniques using Rademacher functions are summarized in the following text.

### D. Summary of MLA With Rademacher Functions

- 1) A set of  $s$ -address lines is selected with voltages corresponding to one of the  $2^s$  binary number

$[(r_1, r_2, \dots, r_{s-1}, r_s)]$ , referred to as select vector] because they are the discrete version of the Rademacher functions.

- 2) Elements of the select vectors are assigned a +1 for logic-0 and -1 for logic 1.
- 3) Select voltages are  $+V_r$  for logic-0 and  $-V_r$  for logic-1 of the binary number.
- 4)  $(N - s)$  non-selected address lines (rows) are held at 0, average of the two select voltages.
- 5) Data vector  $(d_1, d_2 \dots d_{s-1}, d_s)$  represents the state of the pixels in the selected rows of a column.
- 6) Dot product of the data vector with the select vector is computed for each column to assign data (column) voltages.
- 7)
  - a) Data voltages are proportional to the dot product for IHAT. Hence the number of data voltages is  $(s+1)$ .
  - b) Data voltages are restricted to just two in BAT and HAT and hence the sign of the dot product is assigned to the data voltages.

The row and column voltages are applied simultaneously for a duration  $T$  and the process is repeated with all the select vectors ( $2^s$ ) and also by selecting all the sets  $(N/s)$  of address lines to refresh the display continuously at a rate that is fast enough to avoid flicker.

### III. EFFECT OF TRANSITIONS IN THE ADDRESSING WAVEFORMS

Passive matrix displays are modeled as an array of capacitors that are located at the intersection of the scanning (row) and data (column) electrodes. Capacitance of the pixel depends on its state; capacitance of ON pixels is usually higher than that of OFF pixels because twisted nematic and super twisted nematic displays use liquid crystal mixtures with positive dielectric anisotropy. Power is dissipated in the output resistance of the drivers while charging and discharging of pixels depending upon the addressing waveforms. Scanning (row) waveforms are independent of the image whereas the data (column) waveforms depend on the actual image that is displayed in a column. Hence, it is not possible to get a closed form expression for the power dissipation. Even the computation of average power dissipation by considering all the data patterns could be time consuming because  $(2^N)$  is too large even for a moderate value of  $N$ . Power dissipation for a few specific patterns are computed by adding the power dissipation due to each and every transition in a cycle of the addressing waveforms as in the following equation:

$$\sum_{\text{all transits in a cycle}} \frac{1}{2} C (\Delta V_k)^2. \quad (1)$$

Here,  $\Delta V_k$  is the voltage transition across a pixel that is governed by the addressing technique and the scanning sequence. As a first step, power dissipation is computed for all the binary patterns that can be displayed in the selected rows when  $s$ -address lines are selected with all the possible binary patterns sequentially (it corresponds to using Rademacher functions). The number of transitions in the Rademacher functions has a minimum of two and it increases by a factor of 2 to a maximum of  $2^s$  transitions in one of the waveforms. A decrease in RMS voltage across pixels (from the ideal value) due to distortion in the select waveform will be proportional to the number of transitions

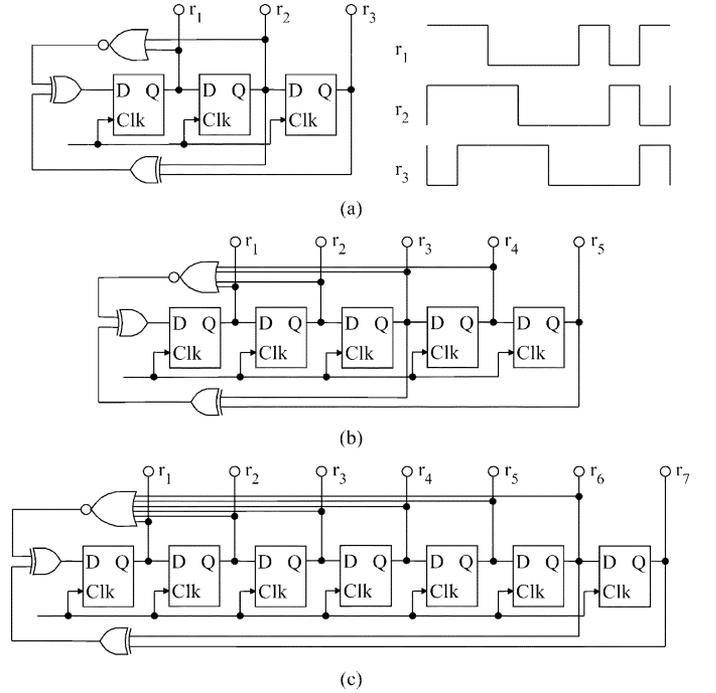


Fig. 1. Modified PRBS generators that are used to obtain the  $2^s$  binary combinations of Rademacher functions so as to include the all zero state in the standard PRBS for (a)  $s = 3$ , (b)  $s = 5$  and (c)  $s = 7$ .

in that waveform. It is preferable to have the number of transitions in the select waveforms to be equal to avoid brightness nonuniformity among pixels that are driven to the same state but located in different rows. Therefore, we have used the modified pseudorandom binary sequence (PRBS) generators (for  $s = 3, 5$ , and  $7$ ) shown in Fig. 1 to obtain the select waveforms with equal number of transitions. The number of transitions is the same and it is equal to  $2^{(s-1)}$  in all the  $s$ -waveforms that are outputs of modified PRBS generators. For example, see Fig. 1(a) that shows all the three outputs for  $s = 3$ . We have normalized the power dissipation of the  $2^s$  patterns to that of  $s$ -pixels in OFF state i.e., “all OFF pattern”. Capacitances of ON and OFF pixels are assumed to be equal to study the effect of just the transitions on the power dissipation. Although the power dissipation of binary patterns varies depending on the states of the pixels in the  $s$ -address lines (in Figs. 2–4), the following observations can be made about the power dissipation.

- 1) It increases with the number of ON pixels in a column, as shown in Figs. 5 and 6, for  $s = 5$  and  $7$ , respectively, where the histogram of power dissipation is rearranged in the order of increasing number of ON pixels (0 to  $s$ ).
- 2) It also increases with the number of transitions in the state of the pixels in a column, i.e., “alternate ON and OFF pixels” dissipate more energy than “all ON” or “all OFF” states in a column. For example, the power dissipation is more when the state of the pixels in a column is “ON-OFF-ON-OFF-ON-OFF-ON” as compared to that of “ON-ON-ON-ON-OFF-OFF-OFF” state.

Power dissipation is a maximum for the “ON-OFF-ON-OFF-ON-OFF-ON” state and “OFF-ON-OFF-ON-OFF-ON-OFF” has the second highest. Power dissipation for the 32 states of pixels in a display addressed with BAT when  $N = 5$

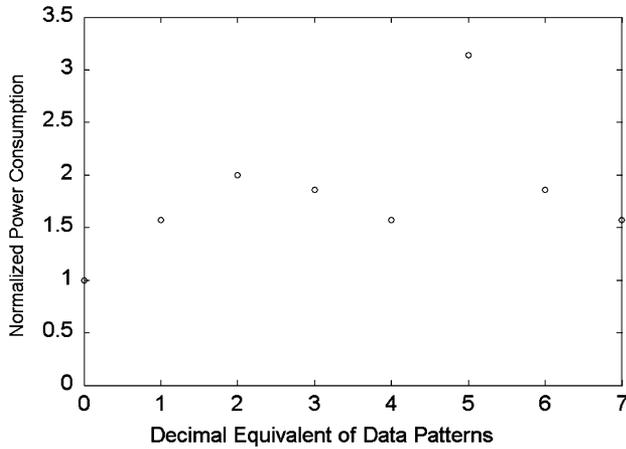


Fig. 2. Estimate of power consumption due to transitions in the waveform for different data patterns when three rows are selected with modified PRBS sequences that contain all the 8 select patterns. Here the capacitance is assumed to be independent of the state of the pixels and the values are normalized to that of “all OFF” pattern in a column because it is the lowest of all values (less number of transitions in the waveform across pixels).

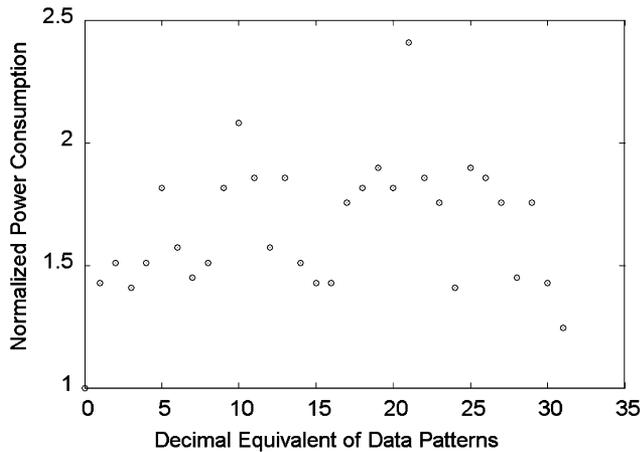


Fig. 3. Estimate of power consumption due to transitions in the waveform for different data patterns when five rows are selected with modified PRBS sequences that contain all the 32 select patterns. Here the capacitance is assumed to be independent of the state of the pixels and the values are normalized to that of “all OFF” pattern in a column because it is the lowest of all values (less number of transitions in the waveform across pixels).

is shown in Table I. Power dissipation is also estimated for the HAT (BAT is a special case of HAT when  $N = s$ ) and IHAT when the pixels in a column are “all OFF”, “all ON” and “alternate ON and OFF pixels” as described here.

- 1) Power dissipation of an OFF pixel in a column with all its pixels in OFF state; it will have the lowest power dissipation because the capacitance of the OFF pixel is less than that of an ON pixel and the number of transitions in the states of the pixel is zero i.e., a minimum.
- 2) Power dissipation of an ON pixel in a column when all the pixels are ON; here again the number of transitions will be a minimum but the capacitance of the ON pixels is higher than that of OFF pixels.
- 3) Power dissipation of an OFF pixel in a column when the state of the pixels changes from one row to another such that the neighboring pixels are driven to opposite states i.e., “alternate ON and OFF” pixels in a column.

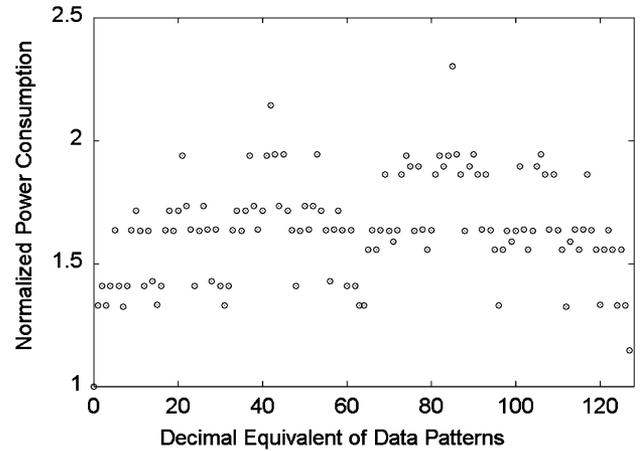


Fig. 4. Estimate of power consumption due to transitions in the waveform for different data patterns when seven rows are selected with modified PRBS sequences that contain all the 128 select patterns. Here the capacitance is assumed to be independent of the state of the pixels and the values are normalized to that of “all OFF” pattern in a column because it is the lowest of all values (less number of transitions in the waveform across pixels).

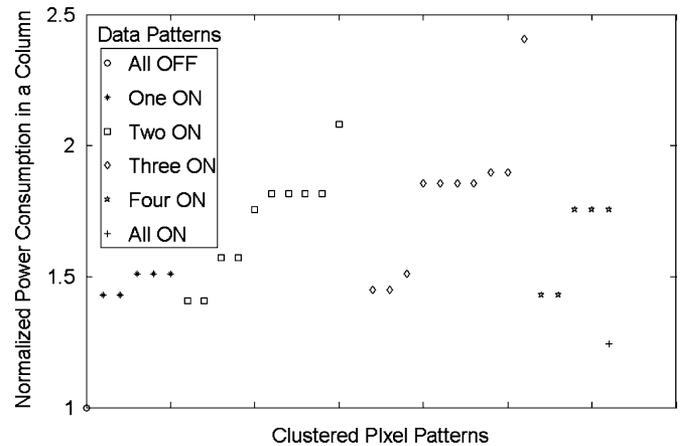


Fig. 5. Normalized Power Consumption per column for all 32 data patterns when  $s$  is 5. All the values have been normalized to the value when all pixels are in OFF state because it is the lowest of all values (less number of transitions in the waveform across pixels). Data patterns having the same number of ON and OFF pixels are arranged to be neighbors to show the dependence on the number of transitions in data patterns.

- 4) Power dissipation of an ON pixel in a column with alternating ON and OFF pixels.

Power dissipation is plotted separately for the OFF and ON pixels because they are normalized to two different factors, i.e.,  $(C_{\text{OFF}}V_{\text{th}}^2/2)$  and  $(C_{\text{ON}}V_{\text{th}}^2/2)$ , respectively [half of the respective capacitances and square of the threshold voltage ( $V_{\text{th}}$ )]. Power dissipation of OFF and ON pixel in the three specific states of pixels (i.e., “all OFF”, “all ON” and “alternate ON and OFF”) in a column when the display is driven by the line-by-line addressing, HAT ( $s = 3$  and  $7$ ) and IHAT ( $s = 3$  and  $7$ ) are shown in Figs. 7–11, respectively. The actual value of the power dissipation can be obtained by multiplying the normalized power dissipation with the factors that correspond to the state of the pixel. As one can see, the power dissipation depends on the pattern that is displayed in a column and to some extent on the addressing technique that is employed to refresh the

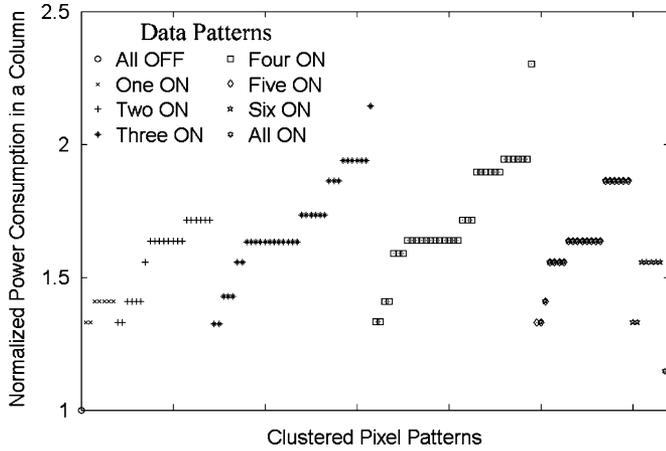


Fig. 6. Normalized Power Consumption per column for all 128 data patterns when  $s$  is 7. All the values have been normalized to the value when all pixels are in OFF state because it is the lowest of all values (less number of transitions in the waveform across pixels). Data patterns having the same number of ON and OFF pixels are arranged to be neighbors to show the dependence on the number of transitions in data patterns.

TABLE I  
NORMALIZED POWER CONSUMPTION OF DIFFERENT STATES OF PIXELS IN A COLUMN OF BAT WHEN  $N = 5$

| State of Pixels | Number of transitions of amplitude V | Number of transitions of amplitude 2V | Power consumption normalized to all zero state |
|-----------------|--------------------------------------|---------------------------------------|--|
| 00000           | 74                                   | 6                                     | 1.0  |
| 10000           | 64                                   | 19                                    | 1.428571                                       |
| 00001           | 64                                   | 19                                    | 1.428571                                       |
| 01000           | 60                                   | 22                                    | 1.510204                                       |
| 00100           | 68                                   | 20                                    | 1.510204                                       |
| 00010           | 60                                   | 22                                    | 1.510204                                       |
| 11000           | 74                                   | 16                                    | 1.408163                                       |
| 00011           | 74                                   | 16                                    | 1.408163                                       |
| 01100           | 82                                   | 18                                    | 1.571429                                       |
| 00110           | 82                                   | 18                                    | 1.571429                                       |
| 10001           | 68                                   | 26                                    | 1.755102                                       |
| 10100           | 66                                   | 28                                    | 1.816327                                       |
| 10010           | 74                                   | 26                                    | 1.816327                                       |
| 01001           | 74                                   | 26                                    | 1.816327                                       |
| 00101           | 66                                   | 28                                    | 1.816327                                       |
| 01010           | 80                                   | 31                                    | 2.081633                                       |
| 11100           | 74                                   | 17                                    | 1.44898  |
| 00111           | 74                                   | 17                                    | 1.44898  |
| 01110           | 68                                   | 20                                    | 1.510204                                       |
| 11010           | 66                                   | 29                                    | 1.857143                                       |
| 10110           | 74                                   | 27                                    | 1.857143                                       |
| 01101           | 74                                   | 27                                    | 1.857143                                       |
| 01011           | 66                                   | 29                                    | 1.857143                                       |
| 11001           | 82                                   | 26                                    | 1.897959                                       |
| 10011           | 82                                   | 26                                    | 1.897959                                       |
| 10101           | 80                                   | 39                                    | 2.408163                                       |
| 11110           | 64                                   | 19                                    | 1.428571                                       |
| 01111           | 64                                   | 19                                    | 1.428571                                       |
| 11101           | 60                                   | 28                                    | 1.755102                                       |
| 11011           | 68                                   | 26                                    | 1.755102                                       |
| 10111           | 60                                   | 28                                    | 1.755102                                       |
| 11111           | 74                                   | 12                                    | 1.244898                                       |

display. Power dissipation will also depend on the scanning sequence, i.e., the order in which the select vectors are used to scan the display. We have used the scanning sequence wherein each set of  $s$  rows is selected with all the possible select vectors before selecting the adjacent set of rows.

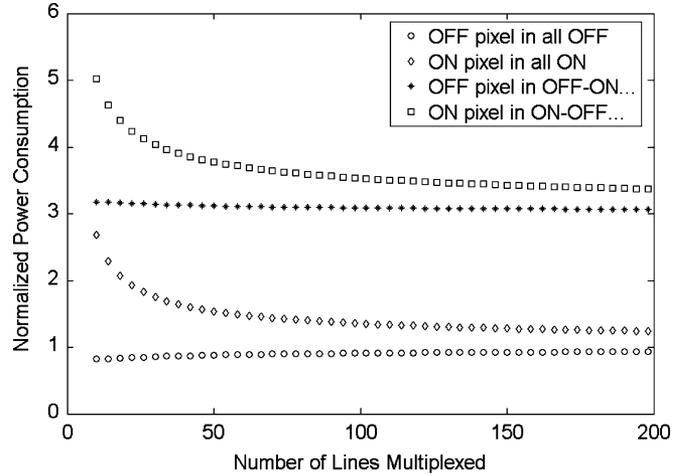


Fig. 7. Plots of normalized power consumption of an OFF and ON pixel when the patterns in a column are "all OFF", "all ON" and "alternating ON and OFF" when the matrix display is driven using line by line addressing technique. Actual power can be obtained by multiplying it with the corresponding normalizing factor viz.  $(C_{OFF}V_{th}^2/2)$ ,  $(C_{ON}V_{th}^2/2)$ , and  $\sim ((C_{OFF}+C_{ON})V_{th}^2/4)$ , respectively.

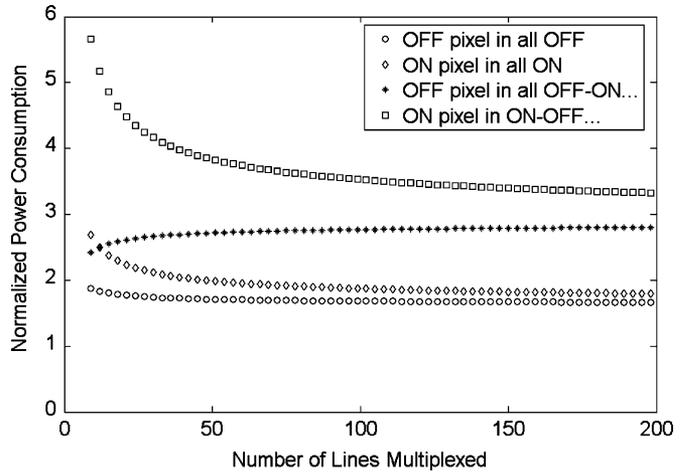


Fig. 8. Plots of normalized power consumption of an OFF and ON pixel when the patterns in a column are "all OFF", "all ON" and "alternating ON and OFF" when the matrix display is driven using HAT ( $s = 3$ ). Actual power can be obtained by multiplying it with the corresponding normalizing factor viz.  $(C_{OFF}V_{th}^2/2)$  for all OFF,  $(C_{ON}V_{th}^2/2)$  for all ON,  $\sim ((2.C_{OFF} + C_{ON})V_{th}^2/6)$  for (OFF-ON pattern) and  $((C_{OFF} + 2.C_{ON})V_{th}^2/6)$  (for ON-OFF pattern), respectively.

#### IV. COMPUTATION OF AVERAGE POWER DISSIPATION

Average power dissipation of the BAT, HAT and IHAT are estimated as described here by assuming that all the  $2^s$  states of the pixels in  $s$  address lines are equally probable.

- 1) Average power dissipation of all the ON pixels i.e.,  $2^{(s-1)}$  ON pixels in the  $2^s$  states in the selected rows is computed when the amplitude of the select and data voltages meet the condition for maximum selection ratio; i.e.,  $V_r = V_c \cdot \sqrt{(N/s)}$  for the HAT and  $V_r = V_c \cdot \sqrt{(N/s)}$  for IHAT. Here,  $V_r$  and  $V_c$  are the amplitude of the select and data voltages, respectively.
- 2) Similarly, the average power dissipation of  $2^{(s-1)}$  OFF pixels in the  $2^s$  states in the selected rows is also computed.

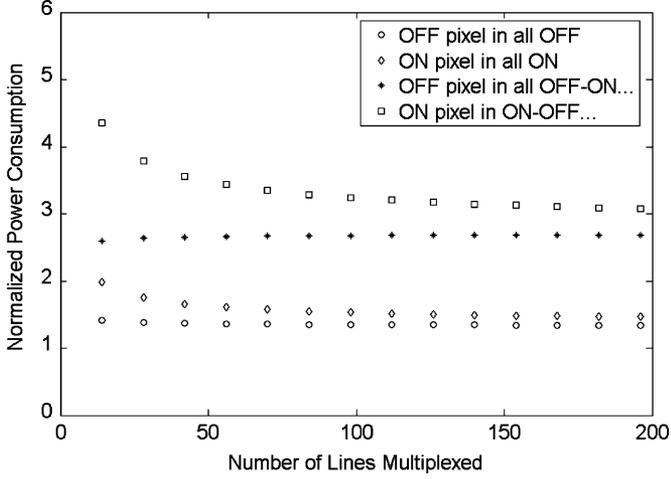


Fig. 9. Plots of normalized power consumption of an OFF and ON pixel when the patterns in a column are “all OFF”, “all ON” and “alternating ON and OFF” when the matrix display is driven using HAT ( $s = 7$ ). Actual power can be obtained by multiplying it with the corresponding normalizing factor viz.  $(C_{\text{OFF}}V_{\text{th}}^2/2)$  for all OFF,  $(C_{\text{ON}}V_{\text{th}}^2/2)$  for all ON,  $\sim ((4.C_{\text{OFF}} + 3.C_{\text{ON}})V_{\text{th}}^2/14)$  for (OFF-ON pattern) and  $((3.C_{\text{OFF}} + 4.C_{\text{ON}})V_{\text{th}}^2/14)$  (for ON-OFF pattern), respectively.

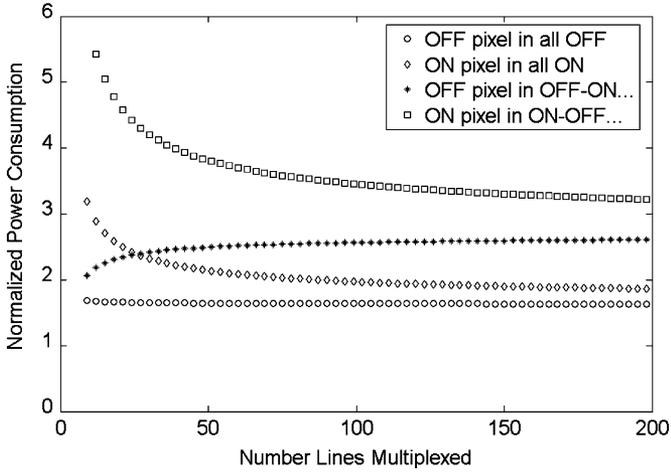


Fig. 10. Plots of normalized power consumption of an OFF and ON pixel when the patterns in a column are “all OFF”, “all ON” and “alternating ON and OFF” when the matrix display is driven using IHAT ( $s = 3$ ). Actual power can be obtained by multiplying it with the corresponding normalizing factor viz.  $(C_{\text{OFF}}V_{\text{th}}^2/2)$  for all OFF,  $(C_{\text{ON}}V_{\text{th}}^2/2)$  for all ON,  $\sim ((2.C_{\text{OFF}} + C_{\text{ON}})V_{\text{th}}^2/6)$  for (OFF-ON pattern) and  $((C_{\text{OFF}} + 2.C_{\text{ON}})V_{\text{th}}^2/6)$  (for ON-OFF pattern) respectively.

- 3) Average power dissipation due to all the possible transitions in the data voltages for all  $2^s$  states in the non-selected rows is also computed by substituting  $V_r = 0$ .

The average power dissipation of an ON pixel is computed as a weighted sum as shown in the following equation:

$$\begin{aligned} &\text{Average power of ON pixels} \\ &= \text{Average power of ON pixels during select time} \\ &\quad + \left(\frac{N}{s} - 1\right) \text{Average power of data waveforms} \\ &\quad \text{for all the states (during non-select time).} \end{aligned} \quad (2)$$

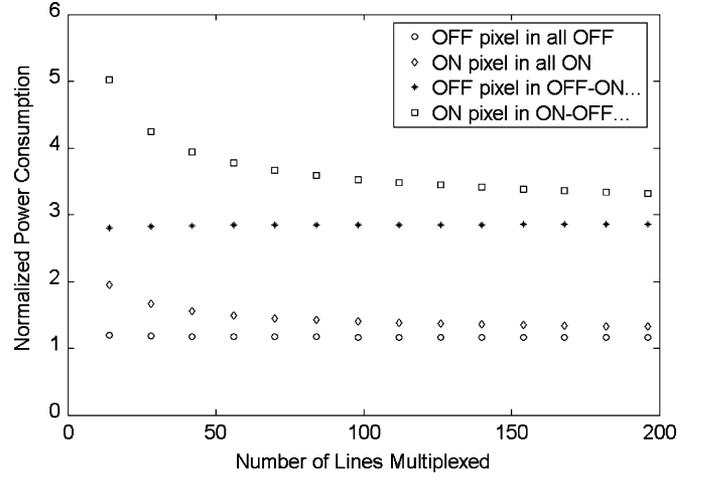


Fig. 11. Plots of normalized power consumption of an OFF and ON pixel when the patterns in a column are “all OFF”, “all ON” and “alternating ON and OFF” when the matrix display is driven using IHAT ( $s = 7$ ). Actual power can be obtained by multiplying it with the corresponding normalizing factor viz.  $(C_{\text{OFF}}V_{\text{th}}^2/2)$  for all OFF,  $(C_{\text{ON}}V_{\text{th}}^2/2)$  for all ON,  $\sim ((4.C_{\text{OFF}} + 3.C_{\text{ON}})V_{\text{th}}^2/14)$  for (OFF-ON pattern) and  $((3.C_{\text{OFF}} + 4.C_{\text{ON}})V_{\text{th}}^2/14)$  (for ON-OFF pattern), respectively.

The average power dissipation of an OFF pixel is also estimated in the same manner as shown in the following equation.

$$\begin{aligned} &\text{Average power of OFF pixels} \\ &= \text{Average power of OFF pixels during select time} \\ &\quad + \left(\frac{N}{s} - 1\right) \text{Average power of data waveforms} \\ &\quad \text{for all the states (during non-select time).} \end{aligned} \quad (3)$$

The average power dissipation here is an estimate because it does not include the actual effect of transitions in  $((N/s))$  data voltages when the selection of  $s$  rows shifts from one set to another because the magnitude of the transitions will depend on the state of the pixels in the neighboring sets. We have assumed the states in the neighboring sets to be in natural binary order for our estimation. Average power dissipation of HAT and IHAT are shown in Figs. 12 and 13, respectively. Here, the average power dissipation of ON pixels is normalized to the average power dissipation of the OFF pixels. The increase in power dissipation of HAT with decrease in  $s$  is mainly due to higher selection ratio of HAT for lower values of  $s$ . Such a trend is not present in the plots of IHAT because the selection ratio of IHAT is independent of  $s$  and it just depends on  $N$ .

## V. ANALYSIS OF POWER DISSIPATION WITH DUTY CYCLE

Transitions in the select waveforms depend on the orthogonal functions. It is possible to ensure that the number of transitions in the select waveforms to be equal at least in some cases; for example, the modified PRBS sequences for Rademacher functions that was presented in Section III. However it is difficult to control the number of transitions in the data waveforms because it depends on the state of the pixels. Hence, it is not possible to derive an expression for power. However, the select voltage as well as the data voltage can be made zero at the end of the select time for a very short duration (say 5%–10% of the select time).

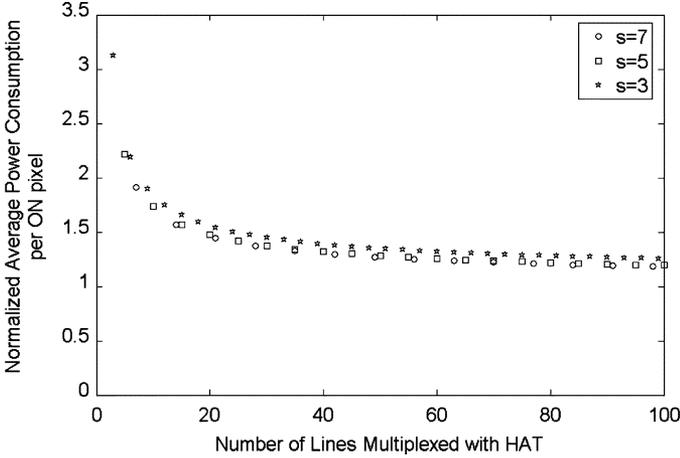


Fig. 12. Average power consumption of ON pixels when the display is addressed with HAT. The selection ratio of the HAT decreases with increase in  $s$  apart from the decrease due to increasing  $N$ . Average power consumption per pixel decreases with decrease in selection ratio.

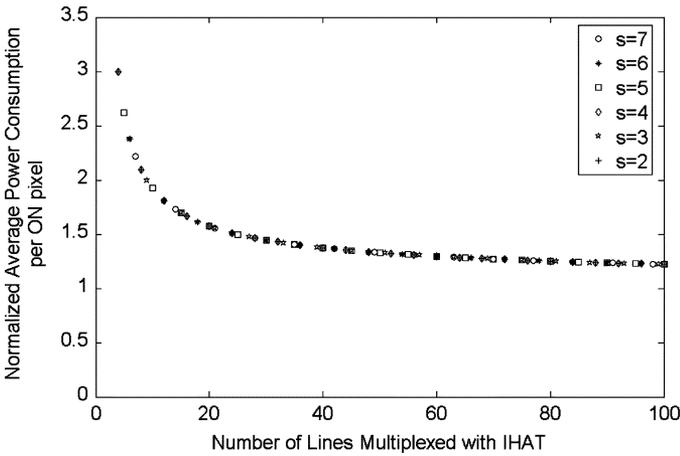


Fig. 13. Average power consumption of ON pixels when the display is addressed with IHAT. The selection ratio of the IHAT decreases with  $N$  but it is independent of  $s$ . Average power consumption per pixel of IHAT also decreases with increase in  $N$ .

Then the number of transitions will be the same across all the pixels in the display and the amplitude of the transitions will also be independent of the data in the neighboring pixels. Although the number of transitions in the addressing waveforms is increased, large transitions from voltages of one polarity to another is eliminated by the introduction of duty cycle. It is important to note that the increase in power dissipation is proportional to the square of the voltage and it is advantageous to decrease the amplitude of the transition and the increase in power dissipation due to increase in the number of transitions can be absorbed to some extent. Introduction of duty cycle improves the brightness uniformity among pixels that are driven to the same state because the distortions in the addressing waveforms will be independent of the state of the pixels in the column. Let  $V_i$  be the instantaneous voltage across a pixel, which is the difference between the instantaneous voltages applied to the row and column of a matrix display. Power dissipated while charging the pixel to  $V_i$  from 0 is  $(C_{\text{pixel}}V_i^2/2)$ . Similarly, the power dissipated in the driver circuit while discharging instantaneous voltage to 0 is

TABLE II  
NORMALIZED POWER DISSIPATION PER PIXEL WHEN BINARY ADDRESSING TECHNIQUE (BAT) IS USED TO REFRESH THE DISPLAY

| Number of lines | BAT without duty cycle |          | BAT with duty cycle |         |
|-----------------|------------------------|----------|---------------------|---------|
|                 | multiplexed            | control  | control             | control |
|                 | ON                     | OFF      | ON                  | OFF     |
| 3               | 3.12                   | 1.125    | 3.0                 | 1.0     |
| 5               | 2.219                  | 1.018752 | 2.2                 | 1.0     |
| 7               | 1.91264                | 1.003552 | 1.909               | 1.0     |

All values for ON pixels are normalized to  $C_{\text{ON}}V_{\text{th}}^2$ . All values for OFF pixels are normalized to  $C_{\text{OFF}}V_{\text{th}}^2$ .

also  $(C_{\text{pixel}}V_i^2/2)$ . Average power of a pixel when the display is refreshed at  $f$  Hz is as follows:

$$P_{\text{pixel}} = f \cdot \sum_{\text{all } i \text{ in a cycle}} C_{\text{pixel}}V_i^2$$

$$= C_{\text{pixel}} \cdot \left( \frac{1}{\text{Period}} \cdot \sum_{\text{all } i \text{ in a cycle}} V_i^2 \right). \quad (4)$$

Here, the summation of the square of the voltage transitions is for all the transitions in a cycle. The term within the parenthesis is the square of the RMS voltage  $V_{\text{pixel RMS}}^2$ . Amplitude of the addressing waveforms has to be increased by a factor  $\sqrt{(T/T_a)}$  when duty cycle is introduced. Here  $T_a$  is the active period of the select and data pulses during the period  $T$ . Average power dissipation in the display depends on the number of pixels in the ON state ( $\alpha_{\text{ON}}$ ), number of pixels in the OFF state ( $\alpha_{\text{OFF}}$ ), capacitance of the pixel in ON state ( $C_{\text{ON}}$ ) and the capacitance of the pixel in OFF state ( $C_{\text{OFF}}$ ) as shown the following expression:

$$P_{\text{display}} = \frac{T}{T_a} \left( \alpha_{\text{ON}} \cdot C_{\text{ON}} \cdot V_{\text{ON (RMS)}}^2 \right. \\ \left. + \alpha_{\text{OFF}} \cdot C_{\text{OFF}} \cdot V_{\text{OFF (RMS)}}^2 \right). \quad (5)$$

Expressions for the RMS voltages in displays that are refreshed by HAT [3] are

$$V_{\text{ON (RMS)}} = V_{\text{th}} \cdot \sqrt{\frac{2^s \left(\frac{N}{s}\right) + \sqrt{\frac{N}{s}}(4A - 2^s)}{2^s \left(\frac{N}{s}\right) - \sqrt{\frac{N}{s}}(4A - 2^s)}} \quad (6)$$

$$V_{\text{OFF (RMS)}} = V_{\text{th}} \quad (7)$$

where in  $V_{\text{th}}$  is the threshold in the electro-optic response of the display and

$$A = \sum_{m=0}^{\frac{s-1}{2}} \frac{(s-1)!}{m!(s-1-m)!}. \quad (8)$$

BAT can be considered as the special case of HAT when  $N = s$ . Normalized average power dissipation of a pixel is shown in Table II for the ON and OFF pixels. Average power dissipation of pixels when the display is addressed without duty cycle; under the assumption that all the  $2^s$  patterns are equally probable is also shown in the table for comparison. Average power

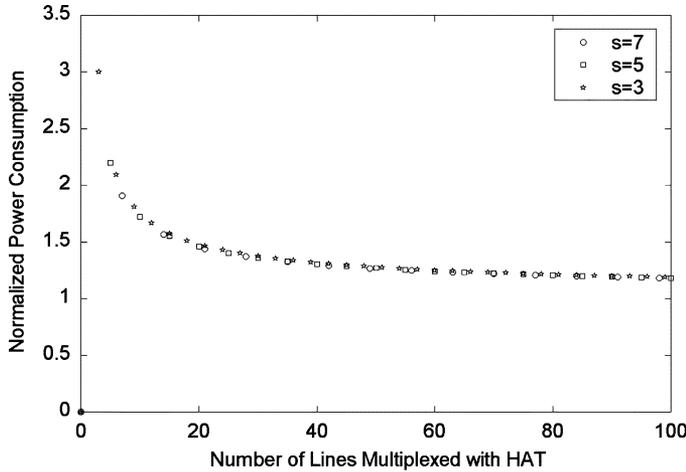


Fig. 14. Normalized power consumption of an ON pixel when duty cycle is introduced in the select and data pulses of IHAT.

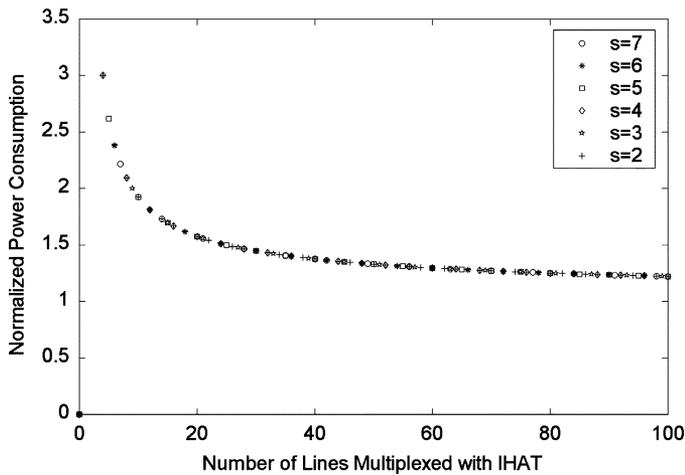


Fig. 15. Normalized power consumption of an ON pixel when duty cycle is introduced in the select and data pulses of IHAT.

dissipation that is normalized to  $C_{ON} \cdot ((T/T_a)) \cdot V_{th}^2$  is plotted in Fig. 14. Expression for the RMS voltage across ON and OFF pixels for IHAT is given in (9) and (10) respectively.

$$V_{ON (RMS)} = V_{th} \cdot \sqrt{\frac{(\sqrt{N} + 1)}{(\sqrt{N} - 1)}} \quad (9)$$

$$V_{OFF (RMS)} = V_{th} \quad (10)$$

Normalized power dissipation of an ON pixel that is driven by IHAT is shown in Fig. 15. The actual power dissipation in the driver circuit can be obtained by multiplying with  $C_{ON} \cdot ((T/T_a)) \cdot V_{th}^2$ .

## VI. CONCLUSION

Power dissipation does not increase drastically with the introduction of duty cycle. Increase in dissipation due to increase in number of transitions gets compensated by the reduction in maximum amplitude of the transitions. For example, transition from  $\pm(V_r + \Delta V_1)$  to  $\mp(V_r + \Delta V_2)$  resulting in an amplitude swing of about  $2V_r$  is split into two transitions of about  $V_r$ . The brightness uniformity of pixels that are driven to the same state is good if the duty cycle is introduced in the select and data pulses.

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## REFERENCES

- [1] S. Ihara, Y. Sugimoto, Y. Nakagawa, T. Kuwata, H. Hasebe, and T. N. Ruckmongathan, "A color STN-LCD with improved contrast, uniformity and response times," in *SID Int. Symp. Dig. Tech. Papers*, 1992, pp. 232–235.
- [2] N. V. Madhusudana and T. N. Ruckmongathan, S. Chandrasekhar, Ed., "A convenient multiplexing scheme for addressing small liquid crystal matrix displays," in *Proc. of Int. Conf. on Liquid Crystals*, 1980, pp. 499–503, Hyden,.
- [3] T. N. Ruckmongathan and N. V. Madhusudhana, "New addressing techniques for multiplexed liquid crystal displays," in *Proc. Soc. Inf. Display*, 1983, vol. 24, no. 3, pp. 259–262.
- [4] T. N. Ruckmongathan, "A generalized addressing technique for RMS responding matrix LCDs," in *Proc. IDRC*, 1988, pp. 80–85.
- [5] B. W. Marks, "Power consumption of multiplexed liquid crystal displays," *IEEE Trans. Electron Devices*, vol. ED-29, no. 8, pp. 1218–1222, 1982.
- [6] B. W. Marks, "Power reduction in liquid crystal display modules," *IEEE Trans. Electron Devices*, vol. ED-29, no. 12, pp. 1884–1886, Dec. 1982.
- [7] T. N. Ruckmongathan, M. Govind, S. V. Ashoka, and G. Deepak, "Binary addressing technique with duty cycle control for LCDs," *IEEE Trans. Electron Devices*, vol. 52, no. 3, pp. 345–351, Mar. 2005.

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