Chapter 1

Introduction

In our information dominated age, the display of information is becoming increasingly essential in many aspects of daily life. Cathode ray tubes (CRTs), electroluminescence devices, plasma display panels (PDPs), field emission devices, flat CRT, vacuum fluorescence, Organic light emitting diode (OLED) displays and liquid crystal displays (LCDs) are some of the display devices available for displaying information in various products. Each of these displays has its own special characteristics and the proper choice of display for a particular use, depends on a number of factors such as power consumption, operating voltage, size, cost, brightness, life, temperature range, drive circuits etc. Of all these displays, the LCDs have emerged as the market leader among the flat panel displays. The importance arises from many of its advantages, including low power consumption, low driving voltages, high definition, good readability in high ambient lighting condition, thin and light weight.

The passive matrix LCDs are used in mobile telephones, Personal Digital Assistants (PDAs) and other medium and low information content displays for portable applications. This is because of low power consumption (without backlight) and low cost due to simple fabrication process. The main objective of this study is to develop addressing techniques for passive matrix LCDs, based on multi-line addressing. In this thesis three different problems have been investigated to improve the performance of passive matrix LCDs. The three different aspects of this investigation are displaying restricted patterns, displaying gray shades and reducing supply voltage of the drive electronics.

Addressing techniques for displaying general patterns, restricted patterns and gray shades in passive matrix LCD are reviewed in the chapter **2.**

A detailed analysis of multi-line addressing for displaying restricted patterns is given in chapter **3.** Hardware complexity of column driver as well as supply voltage has been reduced while displaying multiple waveforms based on multi-line addressing. Steps involved in the design and development of a display controller to demonstrate this technique are also discussed in this chapter.

Chapter 4 covers displaying gray shades using successive approximation and multi-line addressing. This approach reduces the hardware complexity of the drive electronics and hence the cost. Here 2^g gray shades are displayed using g frames without any compromise on selection ratio. Successive approximation has been used in conjunction with multi-line addressing so as to keep the supply voltage low. Details of design and development of a display controller to demonstrate this technique are also discussed in this chapter.

Several addressing techniques with sub-optimal selection ratios are considered in chapter 5 to reduce supply voltage of the drive electronics. A considerable reduction in supply voltage is achieved in the case of Hybrid Addressing Technique (HAT), Improved Hybrid Addressing Technique-S3 (MAT-S3) and Iinproved Hybrid Addressing Technique-S4 (MAT-S4) as compared to supply voltage reductions while using Improved Hybrid Addressing Technique (MAT) or MLA for some values of N, by using liquid crystals with steeper electro-optic response than necessary for an application.

Types of liquid crystalline phases, some of the physical properties related to display applications, electro-optic characteristics of twisted nematic (TN) and super twisted nematic (STN) LCDs are outlined in Appendix A. Generation of the orthogonal functions used for driving passive matrix LCDs and their matrix representation are covered in Appendix B. Single pixel electro-optic setup for measuring the display parameters of the liquid crystal cell is given in Appendix C.

Chapter 2

2. Driving Passive Matrix Liquid Crystal Displays – A Review

Driving Passive Matrix Liquid Crystal Displays – A Review

2.1. Introduction

Addressing techniques for driving passive matrix liquid crystal displays and the techniques for displaying gray shades are reviewed in this chapter. In many applications like logic analyzers, oscilloscope, ECGs etc., one need to display waveforms. The techniques for displaying multiple waveforms are also covered. Apart from description of the technique and analysis, several aspects like condition for optimum selection ratio to achieve good contrast in the display, supply voltage requirement and the hardware complexity of the addressing techniques are discussed in this chapter.

2.2. Direct addressing

Direct addressing (or static drive) is used when the number of segments (or pixels) in a display is small. Each segment has two electrodes and electrodes of all the segments on one of the glass plates are interconnected to form a common back-plane which is taken out as a single connection. Electrodes on the other glass plate of each segment is taken out independently to connect them externally. The intersection of top and bottom electrodes forms a segment. The number of connections ($n+1$) increases with the number of segments(n). Here each segment in a display is addressed individually. Hence, each segment needs a separate display driver to drive it.

A square waveform with 50% duty cycle having an amplitude V is applied to the back-plane. When the waveform applied to the segment electrode is in phase with the waveform applied to the back-plane then segment is driven to OFF state. A segment is ON when the waveforms applied to the segment electrode and the back-plane are out of phase. The voltage across the segment is the difference between the voltages applied to the back-plane and the segment electrodes. The rms voltage across the segment is zero when the waveform applied to it is in phase with the back-plane waveform hence the segment will be OFF. The rms voltage across the segment is V when the waveforms applied to the segment electrode is out of phase with the back-plane and the segment is ON which is dc free as shown in the Figure 2-1. The rms voltage across the ON segment should be greater than the saturation voltage (V_{sat}) to turn it ON. This type of driving is called direct addressing. The rms voltage across the ON segments is chosen to be about three times the

threshold voltage (V_{th}) to get wide viewing angle. CMOS ICs consumes very less power and can be operated over a wide range of supply voltage. Hence they are suitable for driving LCDs, which are low power devices. CMOS Ex-OR gate can be used to control each segment in direct addressing as shown in the Figure 2-1. The one input of the Ex-OR gate is connected to the back-plane waveform and the other input is connected to the data input. When the data input is logic 0 the output of the Ex-OR gate is in phase with the back-plane waveform and the pixel is OFF. The output of the EX-OR gate is out of phase with respect to the back-plane waveform when data input is logic 1 and the pixel is ON. The waveform across the pixel is dc free, which is important to ensure a long life of the display. As the frequency of the square waveform increases, the power consumed by the display also increases. Hence, square waveforms within the frequency range of **30** to **100Hz** is used in direct addressing.

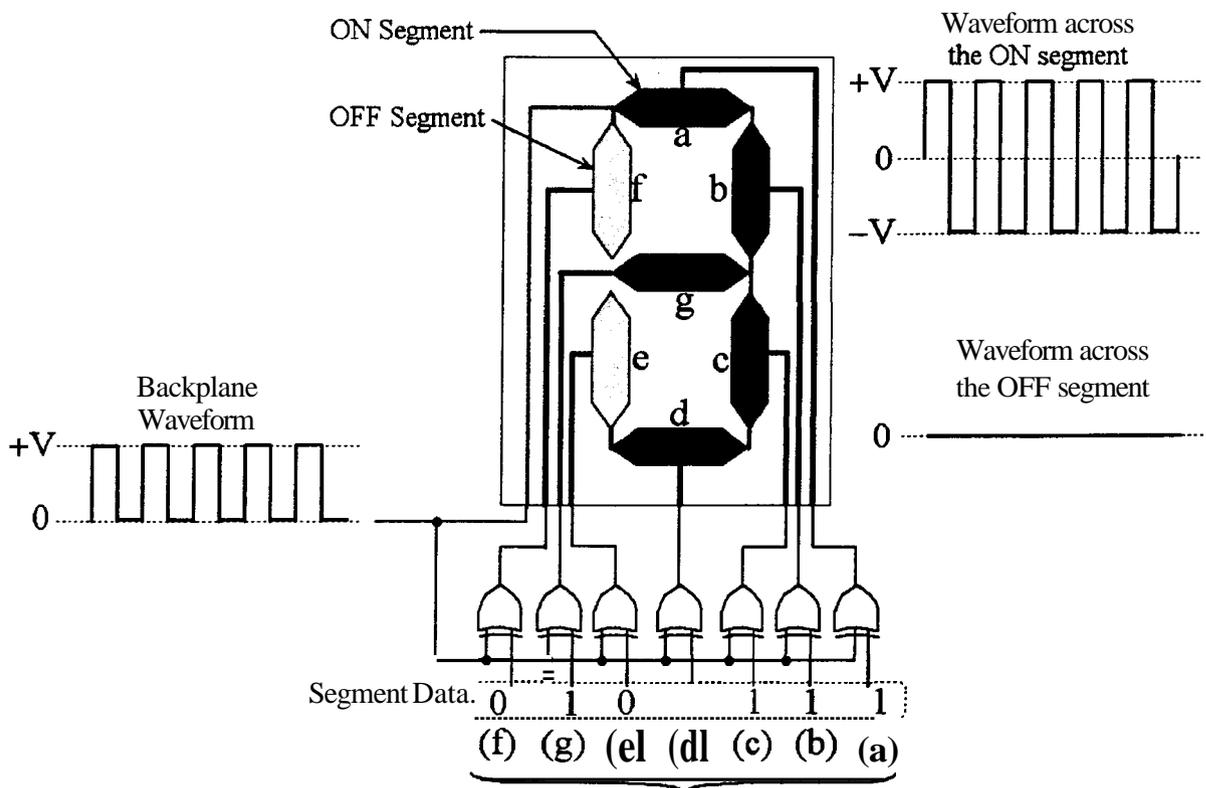**Figure 2-1 Direct addressing for driving segmented liquid crystal displays.**

It is possible to reduce the power consumption of the LCD by modifying the waveforms applied to the ON segments as shown in the Figure 2-2. A delay introduced in the waveform that is applied to the ON segments with respect to the waveform applied to the backplane. Here, the instantaneous voltage is zero across the ON segment for a time

duration, which corresponds to the delay. This allows the charge across the ON segment to discharge without drawing any current from the power supply at every half cycle. About 40% reduction in power consumption has been achieved in practical circuits [1].
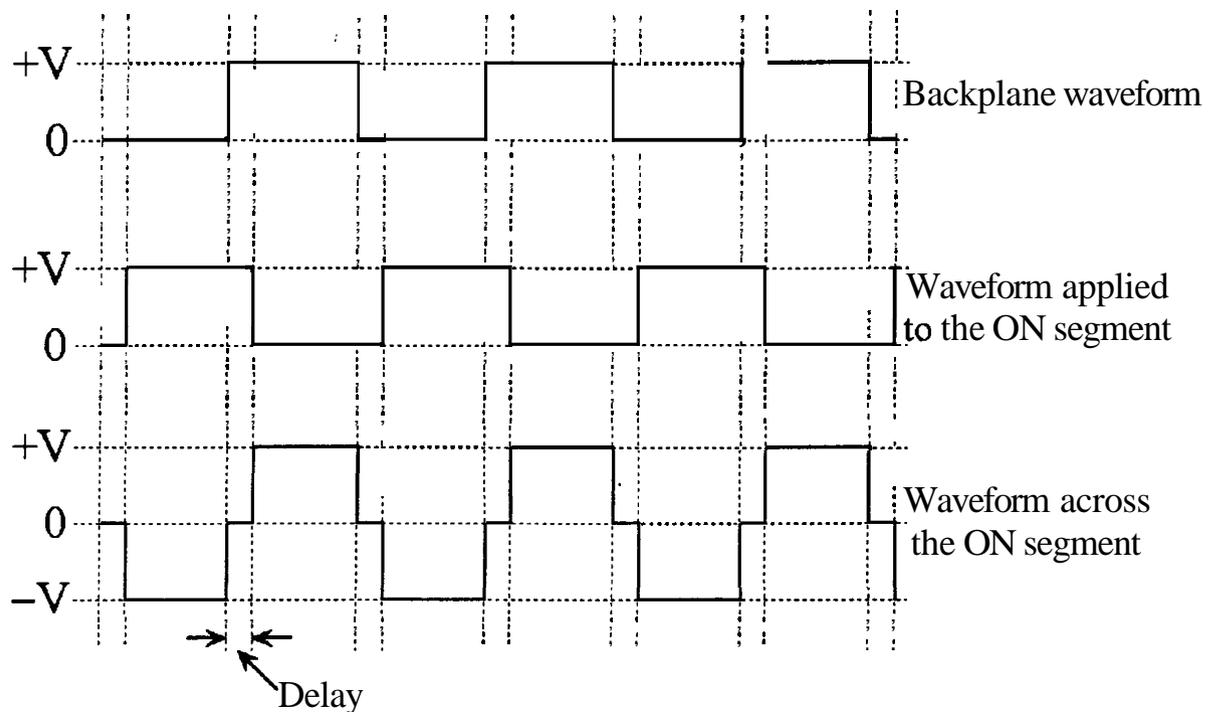

Figure 2-2 Addressing waveforms used to reduce the power consumption in direct addressing.

2.3. *Matrix addressing*

In order to reduce the number of connections to drive the pixels and also to increase the reliability, pixels are arranged in the form of matrix with row and column electrodes. The process of activating pixel in a matrix with out affecting the state of the other pixels is called matrix addressing. Matrix addressing is also referred to as multiplexing as the data to be displayed is time multiplexed through the row or column electrodes. Matrix addressing is essential when the number of pixels in the LCD panel is relatively high. Here, two sets of electrodes are placed orthogonal to each other. One set of electrode is called row electrodes and the other is called column electrodes. Intersections of these row and column electrodes form the pixels. This will reduce. the total number of connections to (N + M), instead of ($N \times M$+1) when the pixels are addressed individually. Where, N and M are the total number of rows and columns in a matrix display and ($N \times M$) is the number of pixels at the intersection of rows and columns electrodes. Here, one set of electrodes (rows or columns) is used for scanning, while the other set (columns or rows) is used for data. Voltages applied to columns electrodes correspond to the data of pixels in selected

rows. The other pixels in the display, which are not selected also get the same voltage and this reduces the display contrast. Intrinsic non-linear electro-optic characteristics.(see appendix A, section A.7.1) of the liquid crystal displays is useful for multiplexing or matrix addressing. LCDs do not respond to the instantaneous voltage due to the slow response of the liquid crystal molecules. The optical state of the pixels does not change as long as the rms voltage across the pixels is lower than the threshold voltage. These two conditions are taken into consideration while addressing the matrix displays.

Matrix LCDs using the intrinsic non linearity of the electro-optic characteristics for addressing are called passive matrix LCDs (PMLCDs). PMLCDs have poor contrast when the number of lines in the matrix is large [5]. On the other hand a non-linear switching device may be integrated at each pixel to achieve a good contrast. This type of matrix LCDs is called active matrix LCDs (AMLCDs). As compared to PMLCDs, AMLCDs have no inherent limitation to the number of address lines. There are many kinds of AMLCDs depending on the switching device used as shown in the Figure 2-3. External non-linear device like Diode[70] or Varistors[71] or Metal-Insulator-Metal(MIM)[72] or Thin Film Transistor (TFT)[73] are used to control each state of the pixel.
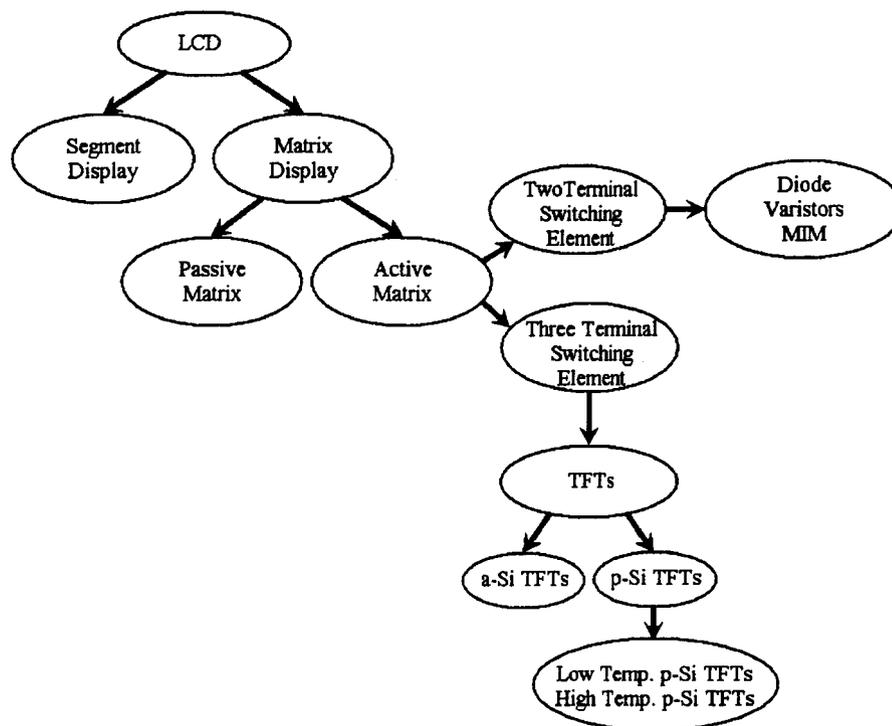

Figure 2-3 Different types of liquid crystal displays.

Two terminal device as a switching element is generally cheaper to fabricate because of fewer process steps and the potential for higher yields. To get dc free operation, simple combination of two or more a-Si diodes are used. These techniques are called **back-to-back** diodes and ring diodes. To address large matrix LCDs multiple diodes are used, but this has the drawback of reducing the aperture size of the pixels. Active matrix LCDs with MIM show better performance as compared to non linear element based on a-Si diodes. The capacitance of the MIM diode should be less than the LC pixel capacitance for proper pixel charging and minimizing the crosstalk. It is essential to minimize the MIM capacitance value. Hence, for very high resolution displays the size of the MIM place a constraint due to large capacitance of the diode. The minimum practical diode size is limited by the resolution capabilities of the processing equipment. Hence, this approach of using MIM is used in low and medium resolution displays.

For a superior image quality, active matrix LCDs use three terminal device like TFTs as a switching element associated with each pixel. Typically, a storage capacitance is incorporated at each pixel to reduce the pixel voltage offset to improve display uniformity. Initially, CdSe TFTs were developed as active matrix switching element. The CdSe **TFT** features a high carrier mobility, now the CdSe **TFT** technology is replaced by the **a-Si** TFT technology due to its similarities to the well established semiconductor silicon technology. The most common TFTs are fabricated as a switching device in LCDs is using amorphous silicon (a-Si). Amorphous silicon can be easily deposited on large area inexpensive glass substrates at a temperature below **300°C** for TFI' fabrication. Almost all **TFT** LCDs which are available in the market are fabricated using a-Si because of the technology's economy and maturity, but the electron mobility of a poly-crystalline silicon (p-Si) TFI' is one or two orders of magnitude greater than that of an a-Si TFT. This makes the p-Si a good candidate for a TFT array containing integrated drivers. p-Si TFT fabrication requires high temperature processing (−600°C) and therefore use expensive quartz substrates. The basic structure of passive matrix and active matrix LCDs are shown in Figure **2-4(a)** and (b), respectively. The main advantages and disadvantages of these LCDs are listed in Table 2-1. The passive matrix LCDs are now being used in mobile telephones, Personal Digital Assistants **(PDAs)** and other medium and low information content displays for portable applications. This is because of low cost, low power consumption (without backlight) and more importantly simple fabrication process.
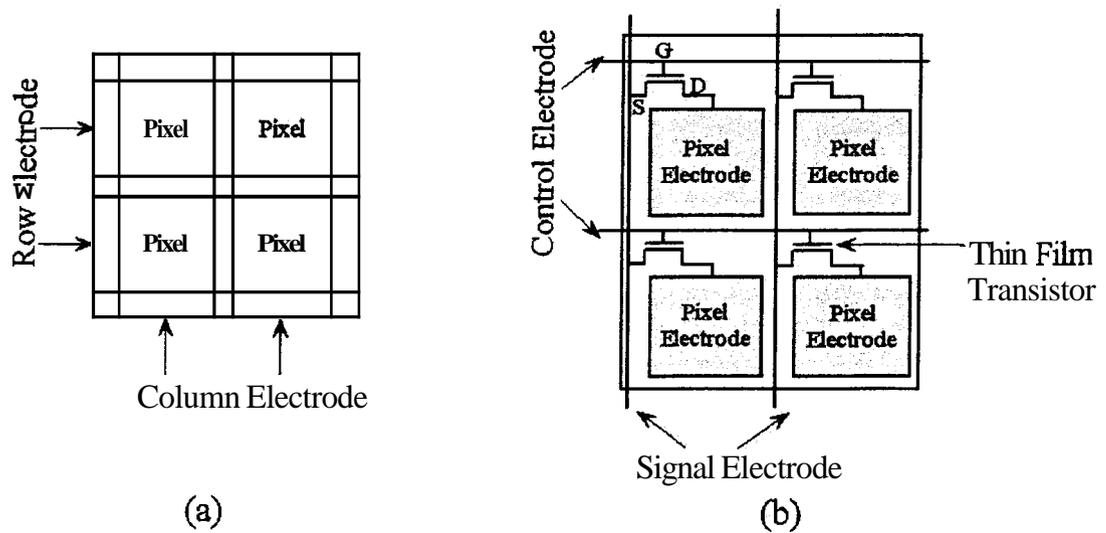
Figure 2-4 Schematic representation of (a) passive matrix (b) active matrix liquid crystal displays.

Table 2-1   A comparison of PM and AM LCDs

Passive Matrix (PM) LCDs	Active Matrix (AM) LCDs
Non-linear electro-optic characteristics in the display device is essential for multiplexing	Non-linear electro-optic characteristics not essential for multiplexing
Intrinsic non-linear electro-optic characteristics is used for multiplexing	External non-linear device (diode or varistors or MIM or TFTs) is fabricated with each pixel.
Contrast ratio and supply voltage depends on matrix size	Contrast ratio and supply voltage can be made independent of matrix size.
Number of gray shades are limited	Large number of gray shades are possible
Simple construction, low cost and good yield	Manufacturing cost is high, fabrication process is complex
Suitable for portable applications like mobile phones and personal digital assistant	High information content display applications like notebook computers, laptop and TV

The main object of this thesis is to study the addressing technique for passive matrix LCDs especially the multi-line addressing technique. The addressing techniques for driving passive matrix LCDs are classified into three types based on scanning of address lines. They are line by line addressing, multiple line addressing and active addressing. These addressing techniques are discussed in the following sections.

2.4. Line by line addressing

The addressing techniques based on the line by line selection are Half Select Technique (HST)[2], One-third Select Technique (OST)[3.], Alt and Pleshko Technique (APT)[4] and Improved Alt and Pleshko Technique (IAPT)[6]. Half select and One-third select techniques do not exploit the rms behavior of the electro-optic response and hence they have lower contrast. These two addressing techniques are covered for historical reasons. Alt and Pleshko showed that the contrast of the display can be enhanced drastically by using the rms behavior of the LCDs in the year 1974. The state of the pixel does not change dramatically by instantaneous voltage due to the slow response of the LCD. That is instantaneous voltage across an OFF pixel can exceed threshold voltage (V_{th}) of the LCD as long as the rms voltage across the pixel is below V_{th}. The addressing techniques based on selecting one line at a time are discussed in the next following sections.

2.4.1. Half select technique(HST)

In half select technique the rows in a matrix LCD are sequentially selected one at a time with a row select voltage $+\dfrac{V}{2}$, while the rest of the unselected rows are grounded. The column voltage is chosen to be $+\dfrac{V}{2}$ for an OFF pixel in the selected row, while the column voltage is $-\dfrac{V}{2}$ for an ON pixel. Both the row and column voltages are applied simultaneously to the matrix display for a time duration τ (refer to as the row select time). Similarly, rest of the rows in the matrix are selected sequentially. A frame is complete when all the rows in a matrix display are selected once. To ensure the long life of the display, the voltage across the pixels should be dc free. This can be achieved by reversing the polarities of both row and column voltages after every frame or within the row select time. A cycle is complete when all the rows in a matrix are selected once, with both polarities. The display is refreshed continuously with a frame frequency greater than 30Hz to avoid flicker. If the display is refreshed with high frame frequencies the row select time decreases. The distortion in row and column waveforms due to the RC time constant of the display panel become significant with short row select times. This will increase the brightness non-uniformity in the display in addition to the increased power consumption due to higher refresh rate. Thus it is always preferable to refresh the display at the rate of

30–60Hz. The rms voltage across the ON and **OFF** pixel while multiplexing **N** row matrix for HST is given by

$$V_{on} = \sqrt{\frac{V^2 + (N-1)\left(\frac{V}{2}\right)^2}{N}}$$

(2. 1)

$$V_{off} = \sqrt{\frac{(N-1)\left(\frac{V}{2}\right)^2}{N}}$$

(2. 2)

The selection ratio *(SR)* is defined as ratio between the rms voltage across the ON pixel to the **OFF** pixel.

$$SR_{HST} = \frac{V_{on}}{V_{off}} = \sqrt{\frac{N+3}{N-1}}$$

(2. 3)

The selection ratio decreases as the number of rows in the matrix increases. The off pixels are biased near the threshold voltage (V_{th}) of the liquid crystal mixture to achieve good contrast. The supply voltage requirement of **HST** is obtained by equating V_{off} to V_{th}.

$$V_{off} = \sqrt{\frac{(N-1)\left(\frac{V}{2}\right)^2}{N}} = V_{th}$$

(2. 4)

The maximum swing in the addressing waveforms is V, hence the supply voltage of HST is given by,

$$V_{sup}(HST) = \sqrt{\frac{4N}{N-1}}\; V_{th}$$

(2. 5)

2.4.2. One-third select technique (OST)

The rows in a matrix **LCD** are selected one at a time sequentially in one-third select technique with a row select voltage $+\dfrac{2v}{3}$, while the rest of the unselected rows are grounded. The column voltage is chosen to be $+\dfrac{V}{3}$ for an OFF pixel in the selected row, while it is $-\dfrac{V}{3}$ for an ON pixel. Both the row and column voltages are applied

simultaneously to the matrix display for a time duration τ. Similarly, rest of the rows are selected one after another. A frame is complete when all the rows in a matrix display are selected once. A dc free operation can be achieved by reversing the polarities of both row and column voltages after every frame or within the row select time. A cycle is complete when all the rows in a matrix are selected with both the polarities once. The display is refreshed continuously at the rate of 30–60Hz. The rms voltage across the ON and OFF pixel while multiplexing a matrix with N rows using OST is given by

$$V_{on} = \sqrt{\frac{V^2 + (N-1)\left(\frac{V}{3}\right)^2}{N}}$$

(2. 6)

$$V_{off} = \sqrt{\frac{\left(\frac{V}{3}\right)^2 + (N-1)\left(\frac{V}{3}\right)^2}{N}}$$

(2. 7)

The selection ratio is given by,

$$SR_{OST} = \frac{V_{on}}{V_{off}} = \sqrt{\frac{N+8}{N}}$$

(2. 8)

The selection ratio of one-third select technique is higher than that of half select technique (see Figure 2-6). Thus by using OST it is possible to multiplex more number of rows in the matrix LCD or achieve better display contrast as compared to HST. The OFF pixels are biased near the threshold voltage (V_{th}) of the liquid crystal mixture to achieve good contrast. The supply voltage requirement of OST is obtained by equating V_{off} to V_{th}.

$$V_{off} = \sqrt{\frac{\left(\frac{V}{3}\right)^2 + (N-1)\left(\frac{V}{3}\right)^2}{N}} = V_{th}$$

$$v = 3\, V_{th}$$

(2. 9)

Supply voltage is independent of the number of rows to be multiplexed but selection ratio decreases as N increases. The maximum swing in the addressing waveforms is $\frac{4\,v}{3}$.

$$V_{sup}(OST) = \frac{4V}{3} = 4\, V_{th}$$

(2. 10)

The supply voltage may be reduced to $3\,V_{th}$ by modifying the addressing waveforms similar to Improved Alt and Pleshko Technique (IAPT) to be discussed in **2.4.4.**

2.4.3. Alt and Pleshko Technique(APT)

In Alt and Pleshko technique **[4]** the rows in a matrix LCD are selected one at a time with a row select voltage $+V_r$, while the rest of the unselected rows are grounded. The column voltage is $+V_c$ for an OFF pixel in the selected row. Here the polarity of the column voltage is same as that of the row select voltage. On the other hand, the column voltage is $-V_c$ for an ON pixel. The polarity of the column voltage is out of phase with the row select voltage for an ON pixel. The row and column voltages are applied simultaneously to the matrix display for a time duration τ. Similarly, rest of the rows are selected sequentially and both the row and column voltages are applied simultaneously to the matrix display for the same duration of time (τ). A frame is complete when all the rows in a matrix display are selected once. In the next frame, amplitudes of the row and column voltages are the same but polarities of both row and column voltages are revered to achieve dc free operation. The dc free operation can also be achieved by reversing the row and column voltages within the row select time. A cycle is complete after selecting all the rows in a matrix once with both positive and negative polarities. The display is refreshed continuously at the rate of **30–60Hz.** Typical addressing waveform for driving a matrix LCD using APT is shown in Figure **2-5.** The instantaneous voltage across the ON and OFF pixels during the row select time is $|V_r + V_c|$ and $|V_r - V_c|$, respectively. The rest of the unselected time intervals the voltage across the pixel is $|V_c|$. The state of the pixel does not change dramatically by instantaneous voltage due to the slow response (~15–100ms) of the LCD. The period of the addressing waveforms is smaller than the response times. In this case, the state of the pixel depends on the rms voltage across the pixel rather than the instantaneous voltage. That is instantaneous voltage across an OFF pixel (i.e., $|V_r - V_c|$) can exceed V_{th} of the LCD as long as the rms voltage across the pixel is below V_{th}. Thus, Alt and Pleshko technique achieves the maximum selection ratio by exploiting the rms behavior of the liquid crystal display.
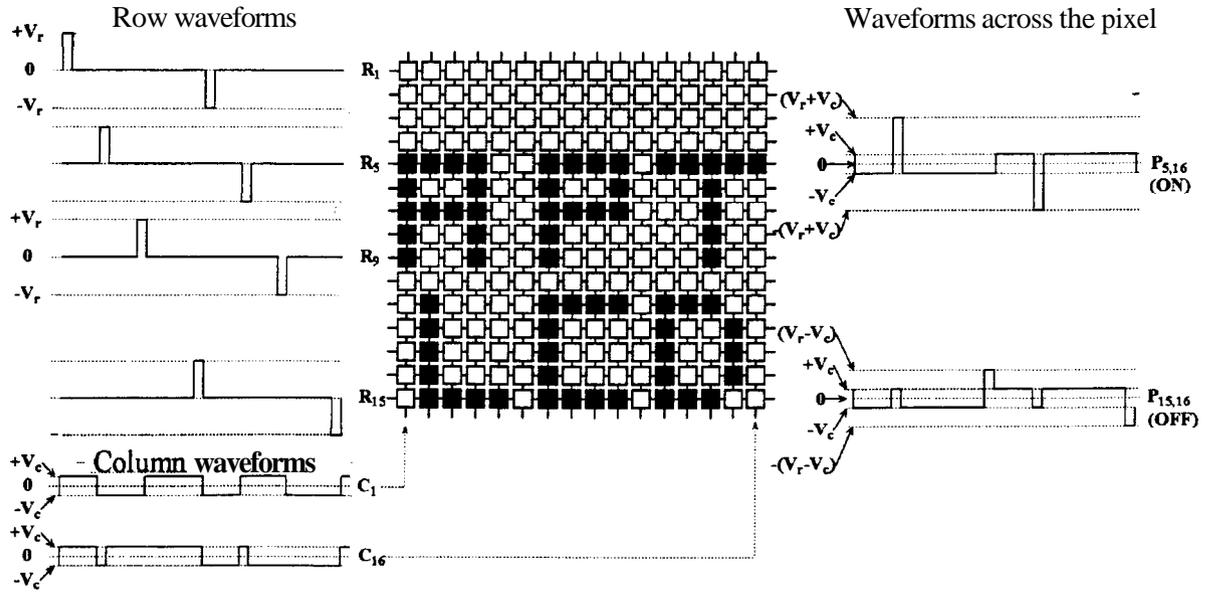
Figure 2-5 Typical addressing waveforms of **APT**

The rms voltage across the ON and OFF pixels in a matrix display with N rows is given by,

$$V_{on} = \sqrt{\frac{(V_r + V_c)^2 + (N-1)V_c^2}{N}}$$

$$V_{on} = \sqrt{\frac{V_r^2 + 2V_rV_c + NV_c^2}{N}} \tag{2.11}$$

$$V_{off} = \sqrt{\frac{(V_r - V_c)^2 + (N-1)V_c^2}{N}}$$

$$V_{off} = \sqrt{\frac{V_r^2 - 2V_rV_c + NV_c^2}{N}} \tag{2.12}$$

$$\frac{V_{on}}{V_{off}} = \sqrt{\frac{V_r^2 + 2V_rV_c + NV_c^2}{V_r^2 - 2V_rV_c + NV_c^2}}$$

The selection ratio (SR) is maximum when

$$V_r = \sqrt{N} \ V_c \tag{2.13}$$

and the selection ratio of the APT is given by,

$$SR_{APT} = \frac{V_{on}}{V_{off}} = \sqrt{\frac{\sqrt{N}+1}{\sqrt{N}-1}} \tag{2.14}$$

The selection ratio of APT is plotted as a function of number of rows or address lines (N) in Figure 2-6. Selection ratios of HST and OST are also plotted in the same figure for comparison. Selection ratios of HST and OST are lower as compared to the APT. The selection ratio of OST is equal to that of APT when N = 4. Hence, the selection ratio of OST is optimum just for four row multiplexing.
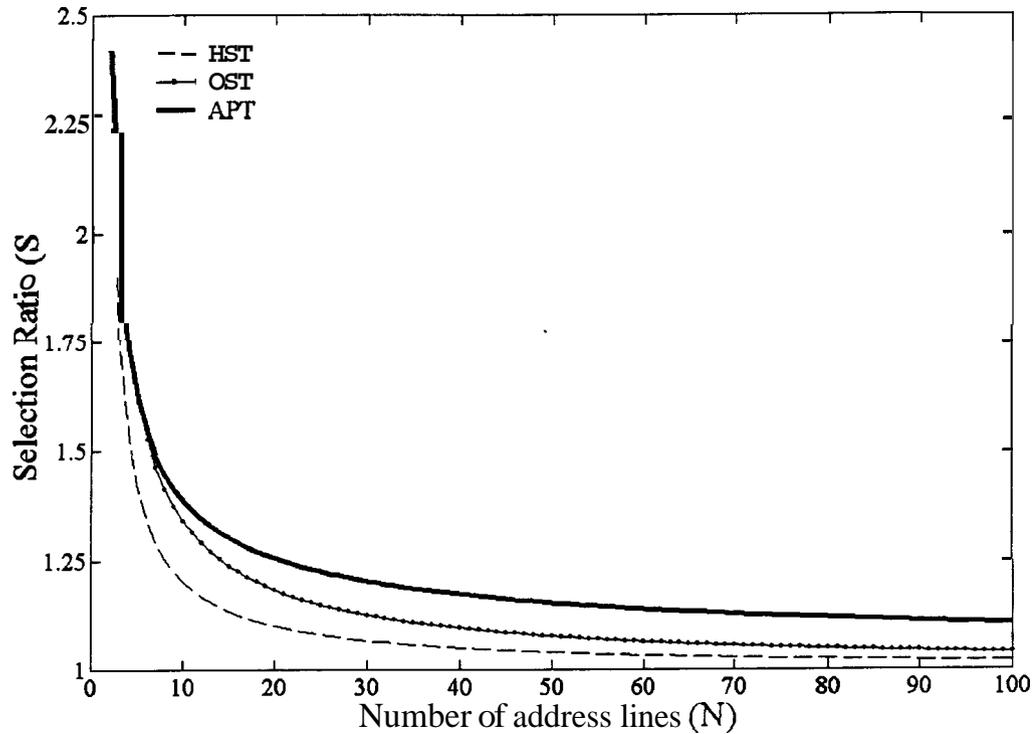

Figure 2-6 Selection ratio versus number of address lines for Half select, One-third select and Alt and Pleshko addressing techniques

Supply voltage of the drive electronics depends on the maximum swing in the addressing waveforms. The maximum swing in the addressing waveforms of APT is $2V_r$. The OFF pixels are biased near the threshold voltage (V_{th}) of the liquid crystal mixture to get good contrast. Hence,

$$V_{off} = \sqrt{\frac{V_r^2 - 2V_r V_c + NV_c^2}{N}} = V_{th}$$

For the maximum selection ratio, $V_r = \sqrt{N}\ V_c$ by substituting this value we have

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$$V_c = \sqrt{\frac{N}{2(N-\sqrt{N})}} \, V_{th} \qquad\qquad (2.15)$$

The supply voltage (V_{sup}) of APT is given by

$$V_{sup(APT)} = 2V_r$$

$$V_{sup(APT)} = 2\sqrt{N} \sqrt{\frac{N}{2(N-\sqrt{N})}} \, V_{th}$$

$$V_{sup(APT)} = \sqrt{\frac{2N\sqrt{N}}{(\sqrt{N}-1)}} \, V_{th} \qquad\qquad (2.16)$$

The maximum instantaneous voltage across any pixel in the display is $|V_r + V_c|$. Hence, it is possible to reduce the supply voltage of APT to be proportional to $(V_r + V_c)$ instead of $2V_r$. Kawakami *et.al.*, [6] have modified the addressing waveforms of APT to reduce the maximum swing to $(V_r + V_c)$. The modified APT is referred to as Improved Alt and Pleshko Technique (IAPT) and is discussed next.

2.4.4. Improved Alt and Pleshko Technique (IAPT)

The modification in the row and column waveforms of APT to reduce the supply voltage is as follows. When the polarity of the row select voltage in APT is positive, then both the row and column voltages are shifted by $+V_c$. When the row select voltage is negative, both row and column voltages are shifted by $+V_r$ as shown in Figure **2-7.** These shifts in the addressing waveforms of both rows and columns do not alter the rms voltage across the pixels. This is because both row and column voltages are shifted by the same amount. Hence, the selection ratio remains same as that of APT but the maximum swing in the addressing waveforms decreases to $(V, +V_c)$.

The supply voltage of IAPT is given by,

$$V_{sup(IAPT)} = (V_r + V_c)$$

Where $V_r = \sqrt{N} \, V_c$, for the maximum selection ratio, hence,

$$V_{sup(IAPT)} = (\sqrt{N} + 1) \, V_c$$

$$V_{\text{sup}(IAPT)} = \left(\sqrt{N} + 1\right)\sqrt{\frac{N}{2\left(N - \sqrt{N}\right)}} \ V_{th}$$

$$V_{\text{sup}(IAPT)} = \left(\sqrt{N} + 1\right)\sqrt{\frac{\sqrt{N}}{2\left(\sqrt{N} - 1\right)}} \ V_{th} \qquad\qquad (2.17)$$
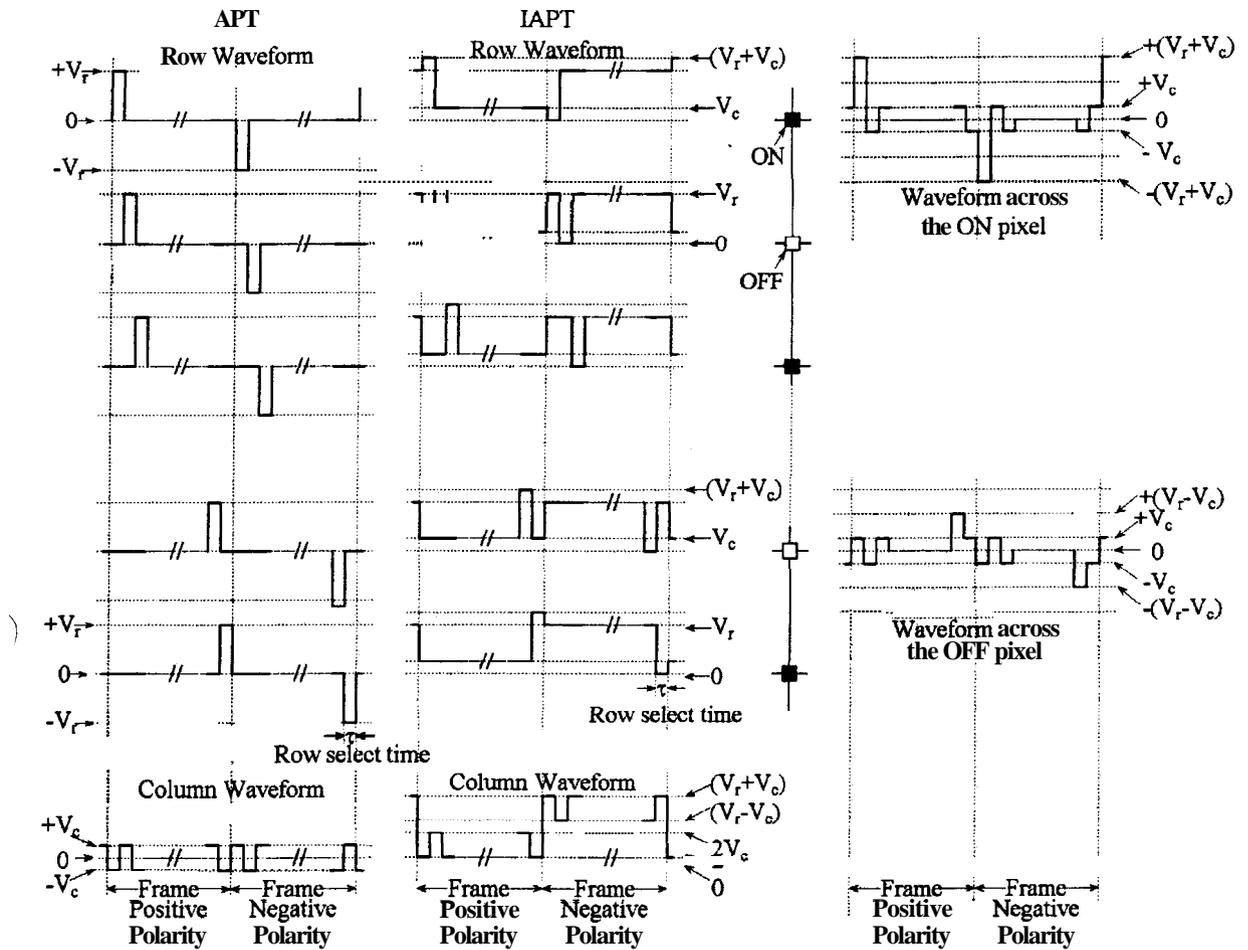

Figure 2-7 Typical addressing waveforms of APT and IAPT.

Figure 2-8 shows the supply voltage (normalized to V_{th}) of IAPT (equation 2.17) and APT (equation 2.16) versus the number of address lines in a matrix LCD (N). When N ≥ 100, more than 45% reduction in supply voltage (i.e., $= \dfrac{V_{sup}(APT) - V_{sup}(IAPT)}{V_{sup}(APT)} \times 100$) is possible in IAPT as shown in the Figure 2-9.
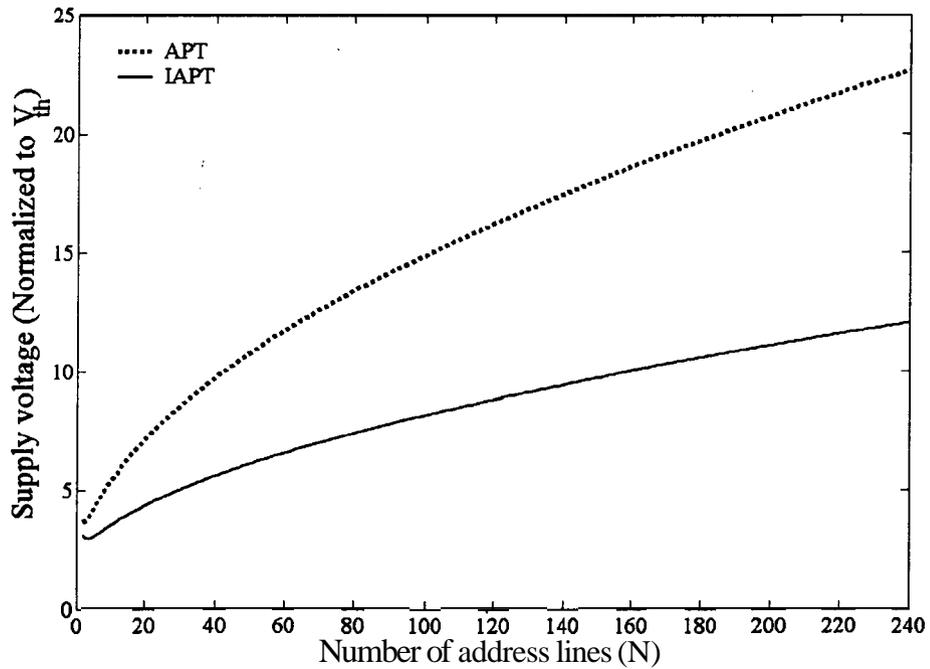
Figure 2-8 Supply voltage (normalized to V_{th}) versus number of address lines of APT and IAPT
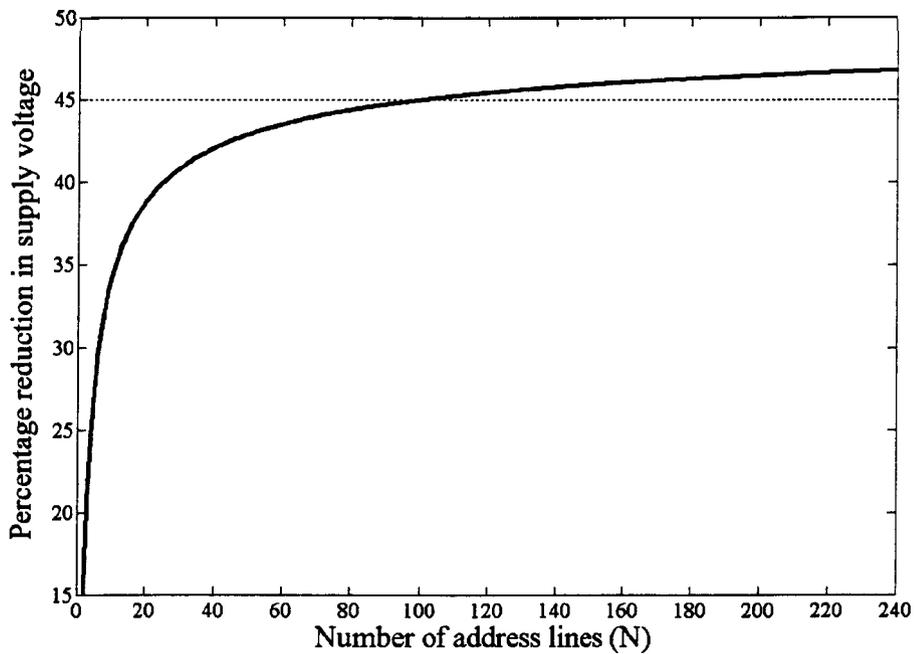

Figure 2-9 Percentage reduction in supply voltage of IAPT as compared to APT for various values of N.

The number of voltages in both row and column waveforms are four in IAPT. In the case of APT number of voltages in row and column waveforms are three and two respectively.

However the number of voltage levels at any instant of time is just two in both IAPT and APT. As the number of address lines increases the supply voltage to display drivers also increases. Supply voltage of IAPT is lower than APT, hence IAPT is the most widely used line by line addressing technique.

In line by line addressing techniques brightness uniformity of the pixels is dependent on the information to be displayed. If the response time of the display is comparable to the frame period (i.e., time between the successive row select pulses) the contrast of the display decreases. This decrease in contrast is observed when line by line addressing technique was used to drive large matrix fast responding LCDs (i.e., response time < 30ms). This decrease in contrast is due to a phenomenon called frame response. Both the brightness non-uniformity and frame response reduce the quality of the displayed image. The cause and the method used to overcome these problems are discussed in the next sections.

2.4.5. Brightness uniformity

The main cause of brightness non uniformity is the distortion of the addressing waveforms. Even a 1% deviation in the rms voltage across the pixels is sufficient to introduce noticeable brightness non-uniformity in the display [7]. When the voltages from the voltage level generator are different from the optimum value, the rms voltage across the pixels also different from the desired value. Hence, the precise voltage levels are necessary while driving the display.

Frequency spectrum of the waveform across the pixels depends on the information being displayed in a column. If the pixels in a column alternate between ON and OFF, then the number of transitions in the column waveform is high. If the pixels in a column are all ON or OFF, then the number of transitions in the column waveform is zero. Thus the frequency spectrum of the waveform across the pixels also varies depending on the information being displayed in a column. The threshold voltage of the liquid crystal mixtures has the frequency dependence (see appendix A.6.1) and this may lead to variations in light transmission across the pixels. Better brightness uniformity is achieved if the frequency spectrum of the pixels lies within the flat region of threshold (or dielectric anisotropy) of the liquid crystal mixture used in the display.

At every transition the waveform get distorted and it changes the rms voltage across the pixels. The distortion depends on the number of transitions in the waveforms and it is due to RC time constant of the display panel. Lowering the RC time constant of the panel can reduce the distortion. However, reducing C (i.e., capacitance) is difficult and lowering R(i.e., resistance) is limited by ON resistance of the drivers and resistance of ITO electrode in practical application. If the transitions are more, the pixels in that column will get a lower rms voltage across them as compared to the case with less number of transitions. This will vary light transmission through the pixels, resulting in brightness non-uniformity of the display. By reversing the polarity of the addressing waveforms after few rows it is possible to lower the drastic variations in the number of transitions [8]. The polarity of the addressing waveforms can be reversed at every L rows, where L is an integer less than the number of address lines in the matrix LCD[9]. The dc component in some cases may remain if the polarity of the address lines is same after m stages, if $\left(\dfrac{m}{L}\right)$ is even. Where, m is the least common multiple of N and L. Hence, after every m stages the polarity of the entire sequence should be reversed, to ensure dc free operation. Brightness uniformity across the pixels cam not be achieved just by reversing the polarities if the data patterns matches with the polarity reversal sequence, again the number of transitions will vary drastically. The polarity reversal sequence can be shifted by one row at every beginning of the sequence [10]. This shift in the polarity reversal sequence helps to make the number of transitions in the column waveforms not to vary drastically with the display patterns. Polarity reversal schemes helps to reduce the brightness non-uniformity problem up to some extent. It is not possible to achieve equal number of voltage transitions at every pixel so that number of transitions are made independent of the data to be displayed. A correction voltage can be superimposed on the column waveform whenever it undergoes a voltage transition to compensate for the distortion of the waveform [11][12][13].

Nishitani *et.al.,* [14] demonstrated the driving method called column voltage compensation driving method to achieve good brightness uniformity. Here, column voltages are made equal to non-select row voltage level for about **20%** at every horizontal period (τ). The voltage across the pixels are momentarily zero for about **20%** of the τ makes the number of transitions constant. The distortion that occurs across the pixels at every voltage transition are same. This results in good brightness uniformity in the display.

2.4.6. Frame response phenomenon

In LCDs, when the response time of the display is comparable to the period of the addressing waveforms, the contrast of the display decreases and it is referred to as frame response phenomenon [15]. The liquid crystal molecules in ON state relaxes due to the large time between successive selection of the row as shown in the Figure 2-10.
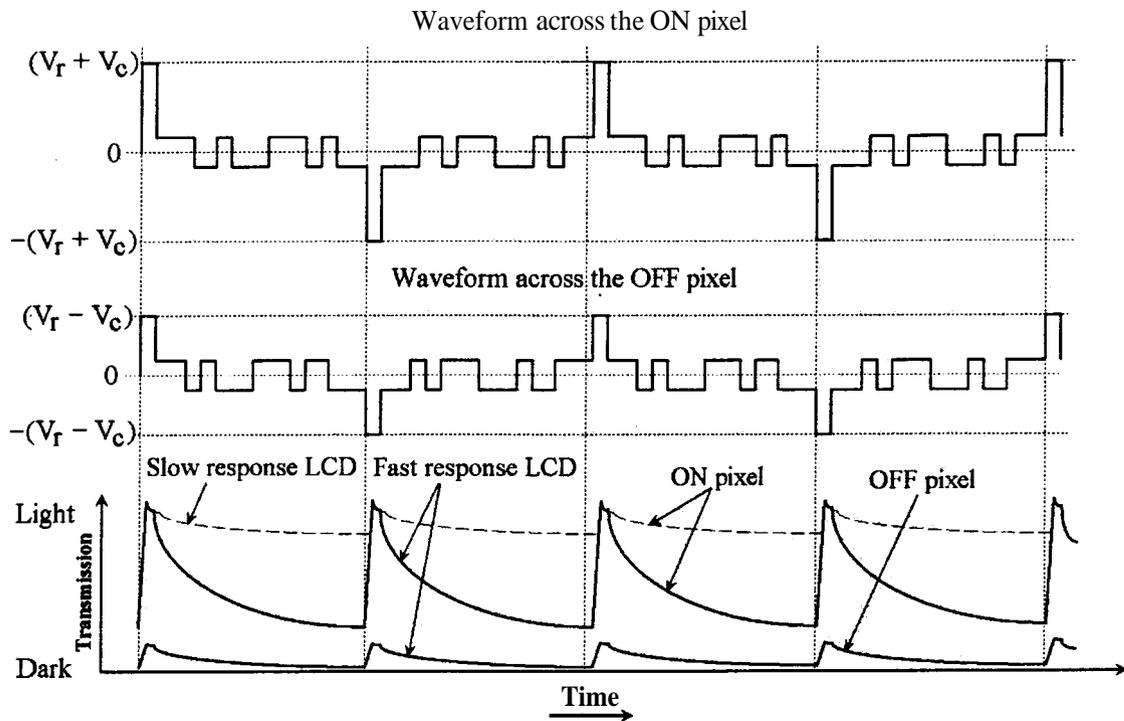

Figure 2-10 Frame response phenomenon in line by line addressing.

The instantaneous voltage across the ON and OFF pixels as well as V_c (normalized to V_{th}) are shown in Figure 2-11 as a function of number of address lines (N). The instantaneous voltage across the OFF (i.e., $V_r - V_c$) pixel is higher than the threshold voltage of the LCD (when the corresponding row is selected (τ)). The liquid crystal molecules start responding to the instantaneous voltage pulses rather than rms voltage. During the row select time interval (τ) light transmission across the OFF pixel increases due to the large amplitude of the pulse. This increase in the light transmission of OFF pixels (see Figure 2-10) and decreases the contrast ratio of the display. The frame response can be suppressed by decreasing $\left(\dfrac{V_r}{V_c}\right)$ ratio from the optimum condition of $\sqrt{N}$. This reduces the amplitude of

the instantaneous voltage across pixels when the row is selected but the selection ratio decreases, resulting in poor contrast of the display. Second approach is to increase the frame frequency so that time between successive row select time decreases. But this increases the power consumption and also results in brightness non-uniformity of the display. This brightness non-uniformity is due to the relatively narrow pulses (i.e., row select time decreases) in the addressing waveforms. The row and column waveforms get distorted due to RC time constant of the display panel. The effect of distortion increases as the row select time is decreased.
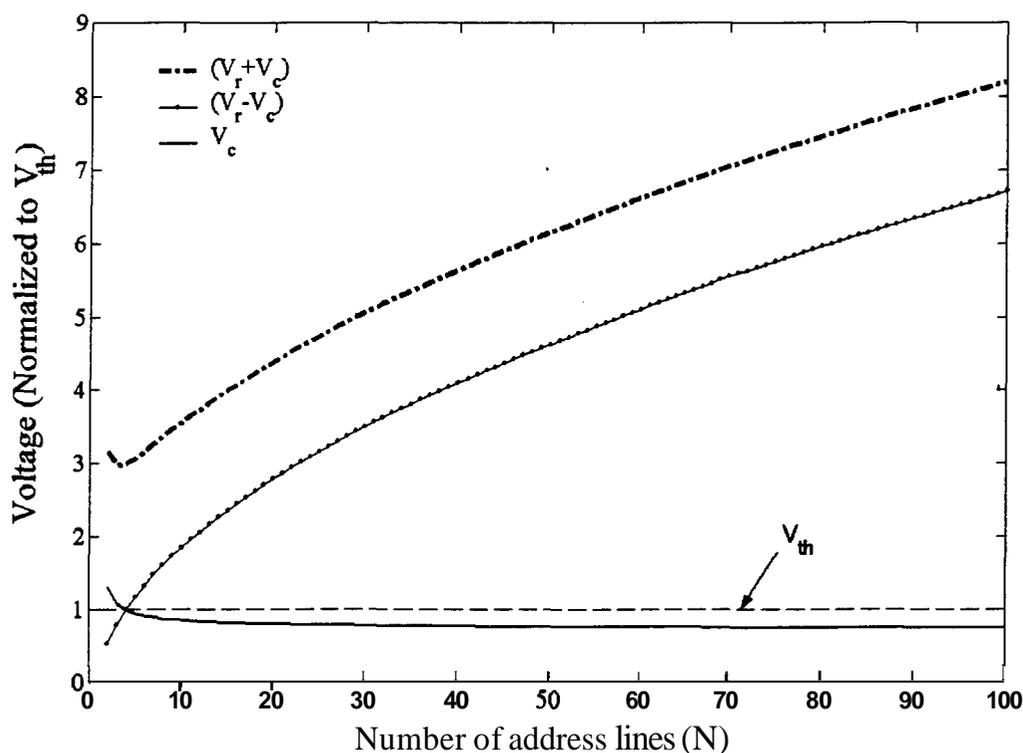

Figure 2-11 Instantaneous voltage across the ON and OFF pixels (normalized to V_{th}) versus number of address lines (N).

It is difficult to suppress the frame response in fast responding LCDs when line by line addressing technique is used. It is possible to get the good brightness uniformity and high contrast if the pixels are made to respond to rms voltage instead of instantaneous voltage even for fast responding LCDs. Multiple line addressing technique (with distributed waveforms in each frame) and active addressing technique have distributed low amplitude pulses in each frame and this is useful for the suppression of frame response. Multiple line addressing and active addressing techniques are outlined in the following sections.

2.5. Selecting a few lines at a time (Multiple line addressing)

A matrix display may also be scanned by selecting a few lines at a time instead of selecting one line at a time. Addressing techniques based on selecting few lines at a time are called as multiple line addressing techniques. [17,22,20,21]. The various multiple line addressing techniques are discussed in the next sections.

2.5.1. Improved Hybrid Addressing Techniques

In Improved hybrid addressing technique (IHAT)[18], the N rows in a matrix display are divided into $\left(\dfrac{N}{s}\right)$ non-intersecting subgroups, each subgroup consists of s address lines. One subgroup is selected at a time with voltages corresponding to a row select pattern derived from the Rademacher functions, while $(N - s)$ unselected rows are grounded. The Rademacher functions are orthogonal and its matrix representation is given in appendix B. The columns of the orthogonal matrix are called row select patterns. The row select voltages are chosen to be $-V_r$ for logic 1 and $+V_r$ for logic 0. The logic 1 and logic 0 are correspond to -1 and $+1$ respectively in the orthogonal matrix of the Rademacher functions. The data for an OFF pixel is chosen to be logic 0 and the data for an ON pixel is chosen to be logic 1. The data to be displayed in the kth selected subgroup is an s-bit word represented by $d_{ks+i}\left(= d_{ks+1}, d_{ks+2}, \ldots\ldots d_{ks+i}, \ldots\ldots d_{ks+s}\right)$. Where, $\left(k = 0,1,2,\ldots\ldots\left(\dfrac{N}{s} - 1\right)\right)$ and $i = 0,1,2,\ldots\ldots s$. The row select pattern is also s-bit word represented as $O(i, j) = O(1, j), O(2, j)\ldots\ldots O(i, j)\ldots\ldots O(s, j)$, where j ranging from 1 to 2'. The column voltage is decided by counting the number of mismatches between the s-bits row select pattern and the data pattern. The number of mismatches (I) is given by

$$I = \sum_{i=1}^{s} O(i, j) \oplus d_{ks+i} \qquad (2. 18)$$

Where, $\oplus$ denotes the Ex-OR operation. The column voltage for each column in the matrix is determined independently depending on the number of mismatches given by the expression,

$$V_I = \left(s - 2\ I\right) V_c \qquad (2. 19)$$

This is same as computing dot product of the row select pattern and the data as explained in section 2.5.2. Once the column voltage is determined for all the columns in the matrix, both row and column voltages are applied simultaneously to the display for a time duration τ. A new row select pattern is chosen next and the column voltages of all the columns in the matrix are determined. The new set of row and column voltages are applied to the matrix display for the same duration τ. A cycle is complete when all the $\left(\dfrac{N}{s}\right)$ subgroups with all the 2^s row select patterns are selected once. That is $2^s\left(\dfrac{N}{s}\right)$ time intervals are necessary to complete a cycle. The display is refreshed continuously repeating the process at 30–60Hz.
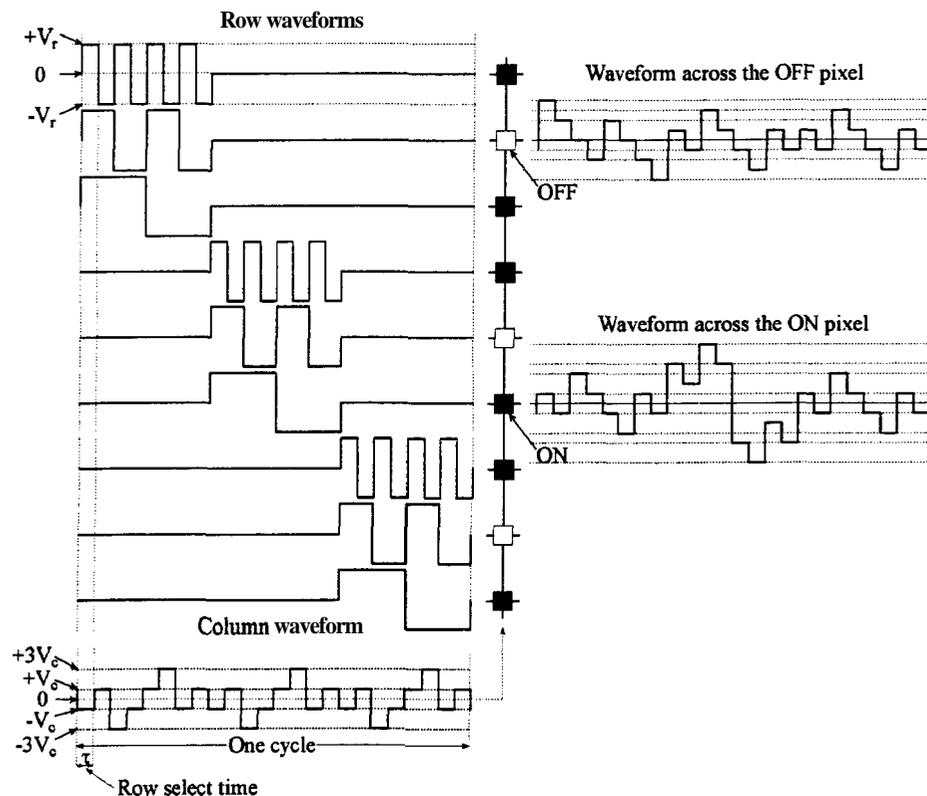

Figure 2-12 Typical addressing waveforms of IHAT, for $N=9$ and $s=3$.

In MAT, when s rows are selected simultaneously number of mismatches between the s-bits row select pattern and data pattern ranges form 0 to s. Hence, $(s+1)$ voltage levels are necessary in the column waveform as shown by the expression (2.19). Figure 2-12 shows the typical addressing waveforms of MAT while selecting **3** rows at a time in a matrix display with nine rows (N = *9)*.
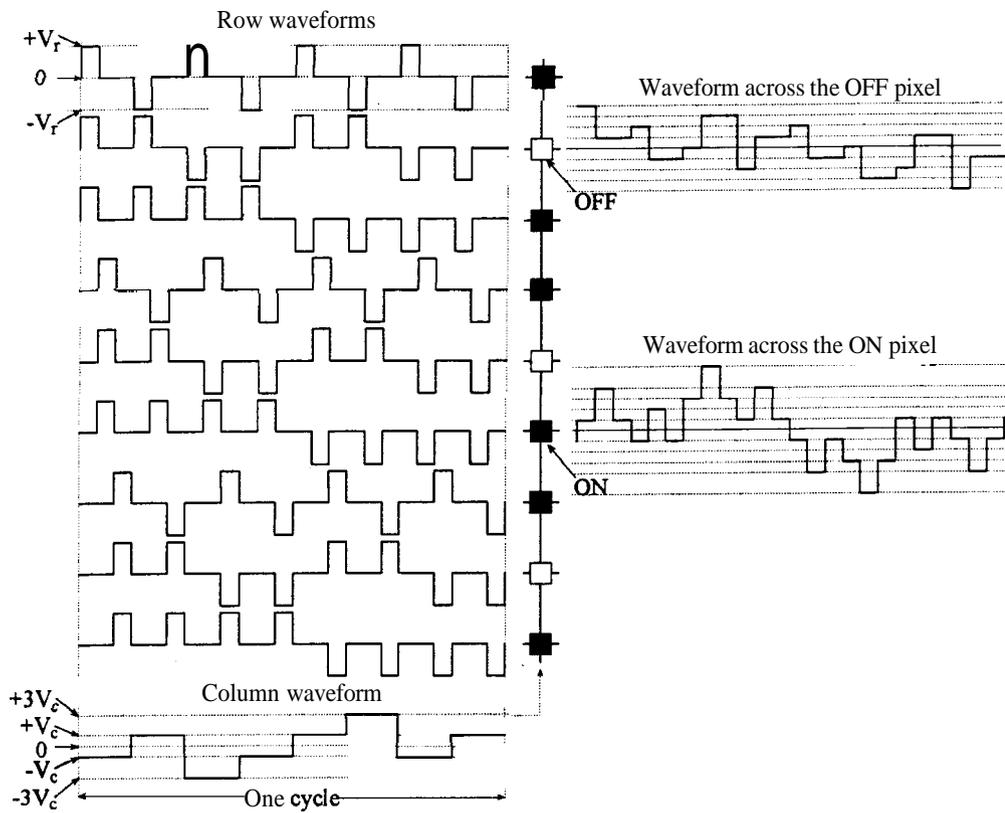
Figure 2-13 Typical addressing waveforms of IHAT (N = 9 and s = 3), row select pulses are distributed in a cycle.
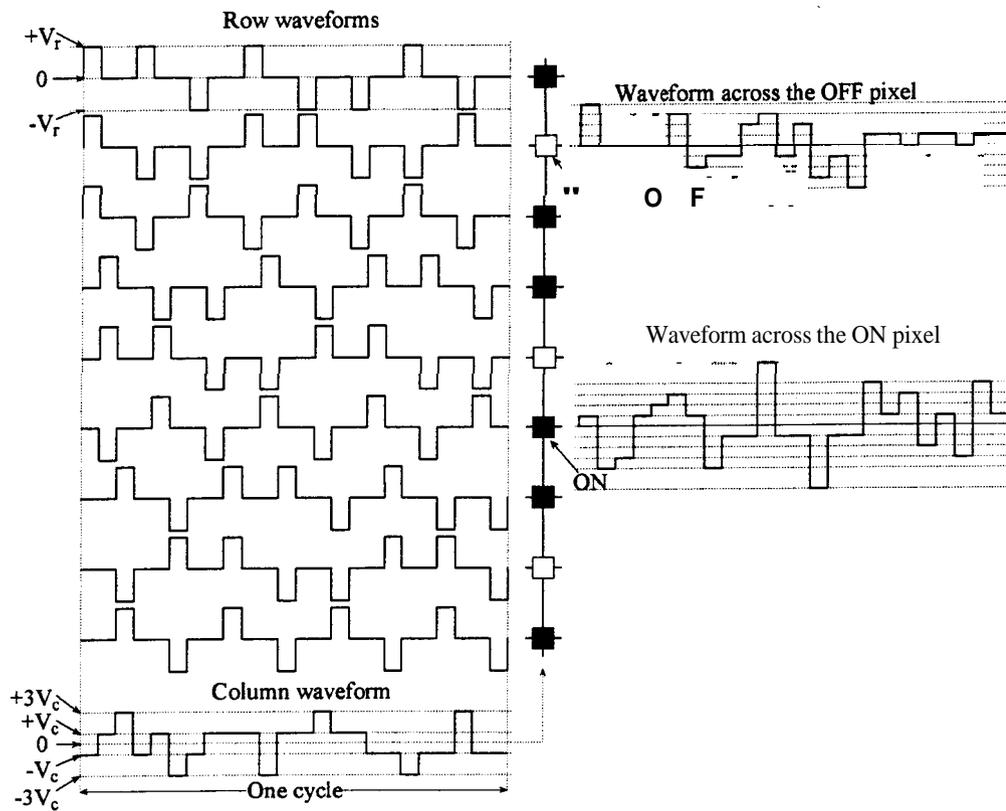

Figure 2-14 Typical addressing waveforms of IHAT (N = 9 and s =3), row select pulses are changed whenever a new subgroup is selected.

The row select pulses are adjacent to each other in case each subgroup is selected with all the row select patterns once before selecting the next subgroup (as shown in the Figure 2-12). This could lead to frame response phenomenon in larger matrix LCDs. The frame response can be suppressed when each subgroup is selected successively with just one row select pattern, as shown in the Figure 2-13. This distributes the row select pulses over the entire cycle uniformly. Good brightness uniformity can be obtained by changing the row select pattern whenever a new subgroup is selected as shown in the Figure 2-14.

The selection ratio (SR) of MAT is a maximum when $V_r = \sqrt{N} \ V_c$, and it is

$$SR = \sqrt{\frac{\sqrt{N}+1}{\sqrt{N}-1}}$$ (2. 20)

Which is same as that of the APT.

The supply voltage $\left(V_{\text{sup}}\right)$ of MAT is determined by the maximum swing in the row and column waveforms and is given by the following expressions.

Case I : when $(N \leq s^2)$

$$V_{\text{sup}} = \sqrt{\frac{2s\sqrt{N}}{\left(\sqrt{N}-1\right)}} \ V_{th}$$ (2. 21)

Case II : when $(N \geq s^2)$

$$V_{\text{sup}} = \sqrt{\frac{2N\sqrt{N}}{s\left(\sqrt{N}-1\right)}} \ V_{th}$$ (2. 22)

Supply voltage of HAT is a minimum when $N = s^2$ [17], that is when number of rows in each subgroup is equal to the square root of total number of rows in the matrix LCD. In this case peak to peak voltage of row and column waveforms are equal. The complexity of the column driver increases with s since $(s+1)$ voltage levels are necessary in the column waveforms. The number of voltage levels in the column waveform in MAT may be restricted to two, three and four depending on grouping of mismatches [17] are called Hybrid Addressing Technique (HAT)[16], Improved Hybrid Addressing Technique−S3 (IHAT−S3)[19] and Improved Hybrid Addressing Technique−S4 (IHAT−S4)[19] respectively. The grouping of mismatches between the row select pattern and the data

vector for HAT, MAT–S3 and MAT–S4 are tabulated in the Table 2-2. The typical addressing waveforms of HAT, MAT–S3 and MAT–S4 are shown in figures 2-15, 2-16 and 2-17 respectively.

Table 2-2

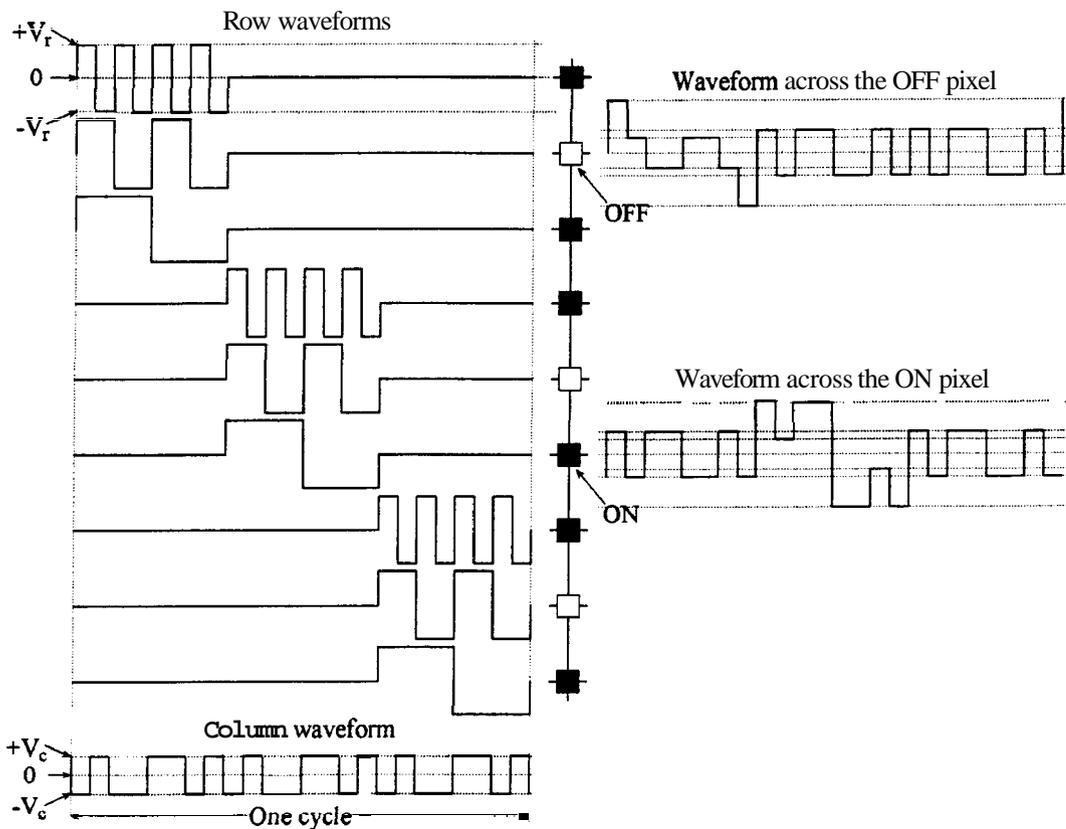| Technique	Mismatches (I)	Column Voltage (V_c)	Number of voltage levels in the column waveform
HAT (odd s)	$I < \left(s/2\right)$ $I > \left(s/2\right)$	$+V_c$ $-V_c$	2
MAT-S3 (even s)	$0 \leq I \leq m$ $m < I < (s - m)$ $(s - m) \leq I \leq s$	$+V_m$ 0 $-V_m$	3
IHAT-S4 (odd s)	$0 \leq I \leq m_1$ $m_1 < I < s/2$ $s/2 \leq I \leq (s - m_1)$ $(s - m_1) \leq I \leq s$	$+V_{m1}$ $+v_{m2}$ $-V_{m2}$ $-V_{m1}$	4

Figure 2-15 Typical addressing waveforms of HAT, for N = 9 and s = 3.

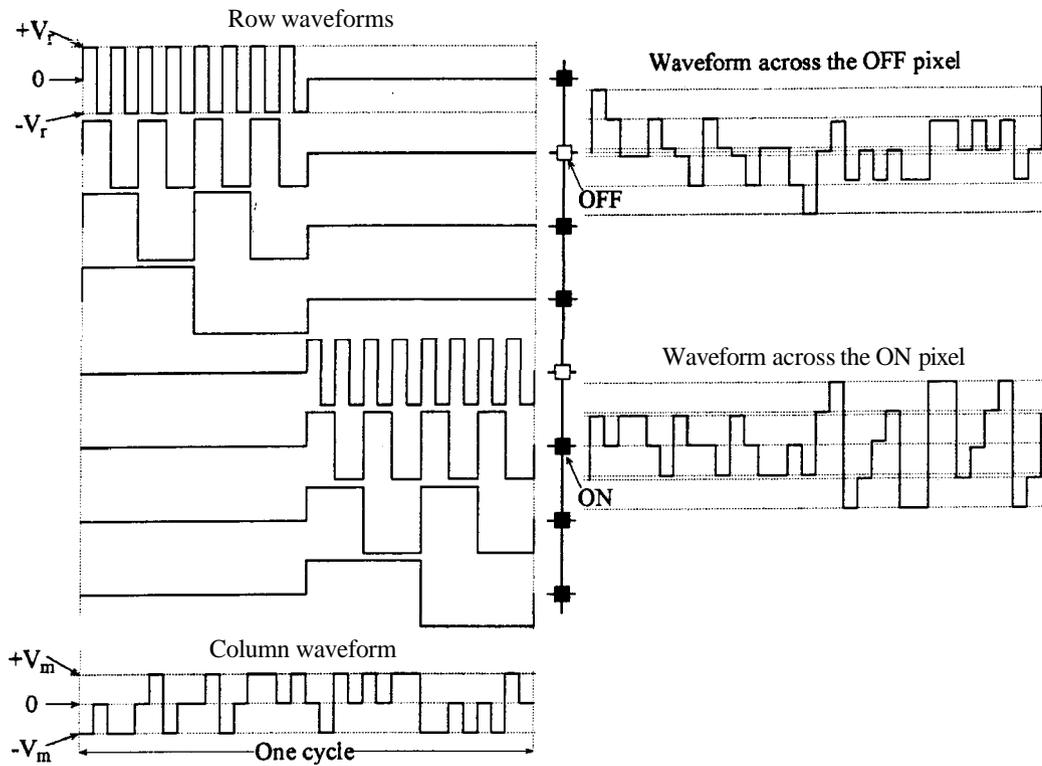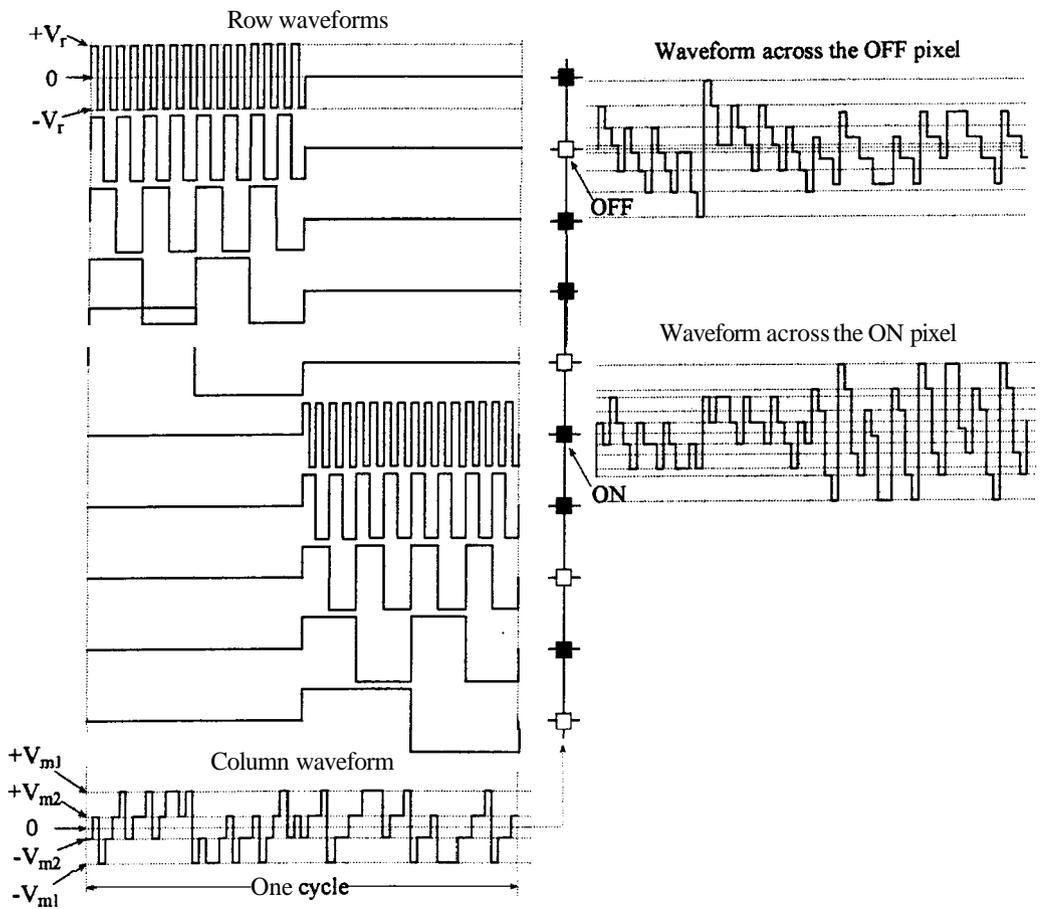**Figure 2-16 Typical addressing waveforms of IHAT–S3, for N = 8 and s = 4.**

Figure 2-17 Typical addressing waveforms of IHAT–S4, for N = 10 and s = 5.

Table 2-3

Technique	s	Grouping of mismatches (I) and the corresponding voltages			
		$+V_m$	0	$-V_m$	
IHAT–S3	4	(0)	(1,2,3)	(4)	
		(0,1)	(2)	(3,4)	Best grouping
	6	(0)	(1,2,3,4,5)	(6)	
		(0,1)	(2,3,4)	(5,6)	
		(0,1,2)	(3)	(4,5,6)	Best grouping

The selection ratio of HAT, MAT–S3 and IHAT–S4 are lower than the maximum due to the restriction imposed on the number of voltage levels in the column waveforms. The Selection ratio of MAT–S3 and MAT–S4 depends on the grouping of mismatches [17] as well as the number of rows in a subgroup (s). For example, two possible grouping of the mismatches for two different values of s in case of IHAT–S3 as well as IHAT–S4 are tabulated in the Table 2-3 and Table 2-4 respectively. Best grouping of mismatches resulting in higher selection ratio is marked in the same tables. The percentage decrease in selection ratio of HAT, IHAT–S3 and MAT–S4 are calculated with respect to the maximum selection ratio for various matrix sizes and for a set of s values is shown in Figure 2-18.

Table 2-4

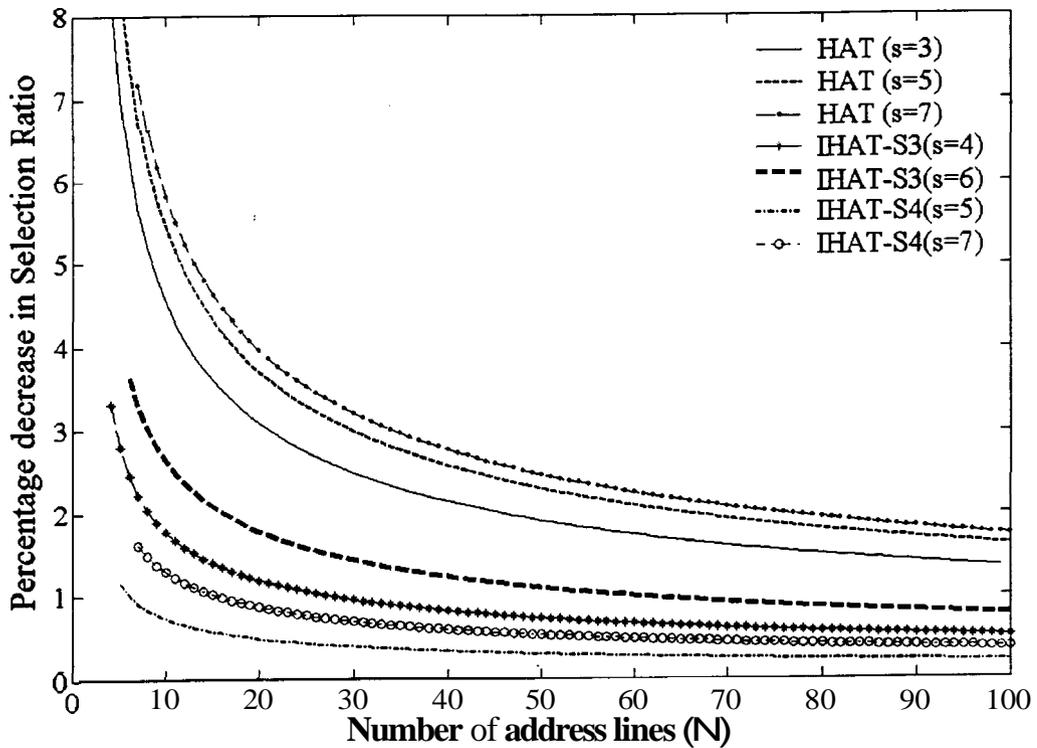| Technique	s	Grouping of mismatches (I) and the corresponding voltages				
		$+V_{m1}$	$+V_{m2}$	$-V_{m2}$	$-V_{m1}$	
IHAT–S4	5	(0)	(1,2)	(3,4)	(5)	
		(0,1)	(2)	(3)	(4,5)	Best grouping
	7	(0)	(1,2,3)	(4,5,6)	(7)	
		(0,1)	(2,3)	(4,5)	(6,7)	
		(0,1,2)	(3)	(4)	(5,6,7)	Best grouping

Figure 2-18 Percentage decrease in selection ratios of HAT, IHAT–S3 and IHAT–S4 as compared to IHAT for various number of address lines (N) for different s values.
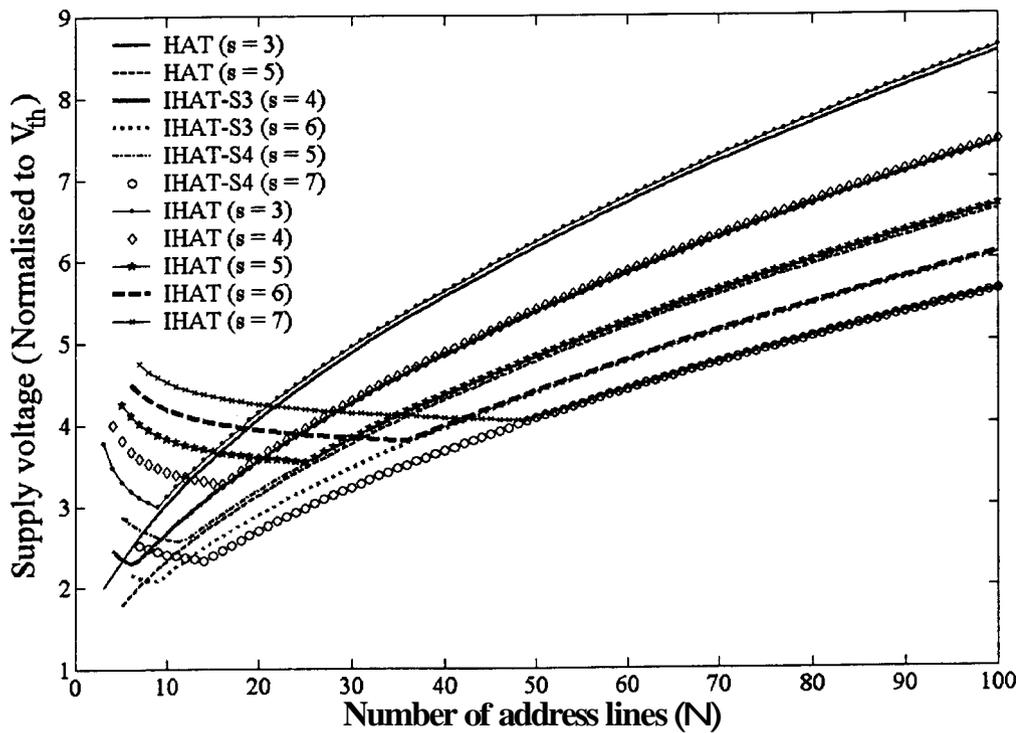

Figure 2-19 Supply voltage (Normalized to V_{th}) versus number of address lines N for IHAT, HAT, IHAT–S3 and IHAT–S4.

Figure 2-19 shows the supply voltage (normalized to V_{th}) versus number of address lines in the matrix LCD. The supply voltage of HAT, MAT−S3 and MAT−S4 are slightly lower than MAT for a given values of s. MAT gives the maximum selection ratio but $2^s\left(\dfrac{N}{s}\right)$ time intervals are needed to complete a cycle. It is preferable to have less number of row select patterns for a given value of s, so that display can be refreshed with less number of time intervals in a cycle. The orthogonal functions derived from Hadarnard matrices and Walsh functions are preferred because number of time intervals in the orthogonal functions are less as compared to Rademacher functions. If the row select patterns are derived from Hadamard matrices or Walsh functions, then the addressing techniques are referred to sequency addressing technique (SAT) or popularly known as multi-line addressing (MLA) [20][21] and these techniques are outlined in the next section.

2.5.2. Multi-line addressing technique

Multi-line addressing (MLA) techniques are similar to MAT, N rows in the matrix LCD are divided in to $\left(3\right)$ subgroups, each subgroup consists of s address lines. At a given instant of time, one subgroup is selected with voltages corresponding to a row select pattern derived from orthogonal functions like Walsh functions, Hadamard matrices, or Pseudo random binary sequence. The generation of these orthogonal functions and their matrix representation are given in Appendix B. Each column of the orthogonal matrix is called a row select pattern. The s rows in a subgroup are selected with either $+V_r$ or $-V_r$ corresponding to a $+1$ or -1 in the row select pattern, while the remaining $(N - s)$ unselected rows are grounded. The data to be displayed in the selected subgroup is chosen to be $+1$ for an OFF pixel and -1 for an ON pixel. The column voltage is the dot product between the row select pattern and data pattern in the selected subgroup. The column signal $C_k(j)$ (normalized to V_c) for a given column when the kth subgroup is selected and can be mathematically represented by,

$$C_k(j) = \sum_{i=1}^{s} O(i,j) \cdot d_{ks+i} \qquad\qquad (2.23)$$

Where, $d_{ks+i} (= d_{ks+1}, d_{ks+2}, ...d_{ks+i}, ...d_{ks+s})$ is the data pattern in the kth subgroup

$\left(k = 0,1,2, .. \left(\dfrac{N}{s} - 1 \right) \right)$ and $O(i, j) = O(1, j), O(2, j)......O(i, j)......O(s, j)$ is the j^{th^-} row

select pattern (i.e., $1 \leq j \leq q$). Here, q is the total number of row select patterns in the selected orthogonal matrix. The column signal for all the columns are computed and transferred to the column driver. Then both row and column voltages are applied simultaneously to the matrix display for a time duration τ. The process is repeated with another row select pattern by computing the column data for all the columns and shifting it into the column driver. The new row and column voltages are applied to the matrix display for the same duration τ. The process is repeated with another row select pattern by selecting the same subgroup or a different subgroup. Good brightness uniformity can be obtained when changing the row select pattern whenever a new subgroup is selected. The display is refreshed continuously by repeating the entire process at **30** to **60Hz.** Figure 2-20 shows the typical addressing waveforms of multi-line addressing technique while selecting **3** rows at a time for $N = 9$. The row waveforms used in the Figure 2-20 are derived from a set of Hadamard matrices.
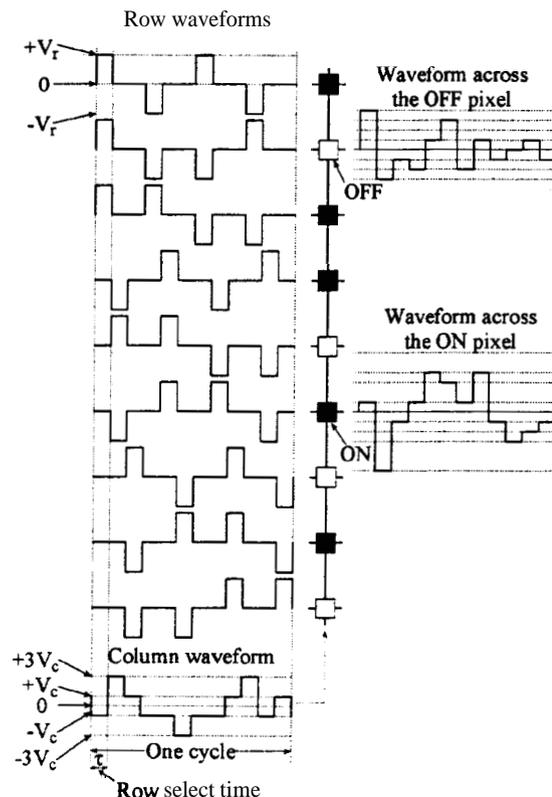

Figure 2-20 Typical addressing waveforms of MLA while selecting three rows at a time.

The rms voltage across the ith pixel in the kth subgroup of a column is given by

$$V_{ks+i}(rms) = \sqrt{\frac{\sum_{j=1}^{q}[O(i,j)V_r - C_k(j)V_c]^2 + \sum_{\substack{n=0 \\ n\neq k}}^{N/s-1}\sum_{j=1}^{q}[C_n(j)V_c]^2}{(N/s)q}}$$ (2. 24)

$$V_{ks+i}(rms) = \sqrt{\frac{V_r^2\sum_{j=1}^{q}[O(i,j)]^2 - 2V_rV_c\sum_{j=1}^{q}O(i,j)C_k(j) + V_c^2\sum_{n=0}^{N/s-1}\sum_{j=1}^{q}[C_n(j)]^2}{(N/s)q}}$$ (2. 25)

Substituting equation (2.23) in (2.25), then

$$V_{ks+i}(rms) = \sqrt{\frac{V_r^2\sum_{j=1}^{q}O(i,j)^2 - 2V_rV_cd_{ks+i}\sum_{j=1}^{q}O(i,j)^2 + V_c^2\sum_{n=0}^{N/s-1}\sum_{i=1}^{s}\sum_{j=1}^{q}O(i,j)^2(d_{ns+i})^2}{(N/s)q}}$$

By substituting orthogonal condition i.e., $\sum_{j=1}^{4}O(i,j)^2 = q$,

$$V_{ks+i}(rms) = \sqrt{\frac{qV_r^2 - 2qV_rV_cd_{ks+i} + qV_c^2\sum_{n=0}^{N/s-1}\sum_{i=1}^{s}(d_{ns+i})^2}{(N/s)q}}$$ (2. 26)

The data for the pixels in a column is $d_{ns+i} = +1$ or -1, hence the last term in the above

equation (2.26) is $\quad qV_c^2\sum_{n=0}^{\frac{N}{s}-1}\sum_{i=1}^{s}(d_{ns+i})^2 = qV_c^2N$.

Then the expression for the rms voltage across the pixel is given by

$$V_{ks+i}(rms) = \sqrt{\frac{V_r^2 - 2V_rV_cd_{ks+i} + NV_c^2}{(N/s)}}$$ (2. 27)

This is the general expression for the rms voltage across the pixel. It is important to note that the number of row select patterns (i.e., q) is not present in the above expression

(equation 2.27) for the rms voltage across the pixel. That is rms voltage across the pixels in the matrix does not depend on the set of orthogonal functions (Walsh, Hadamard, PRBS or Rademacher functions) used to scan the matrix. If the ith pixel in the kth selected subgroup is ON, then $d_{ks+i} = -1$. The rms voltage across the ON pixel is given by

$$V_{on} = \sqrt{\frac{V_r^2 + 2V_rV_c + NV_c^2}{\left(N/s\right)}} \qquad (2.28)$$

Similarly if the pixel is OFF that is $d_{ks+i} = +1$, then the rms voltage across the OFF pixel is given by

$$V_{off} = \sqrt{\frac{V_r^2 - 2V_rV_c + NV_c^2}{\left(N/s\right)}} \qquad (2.29)$$

The selection ratio (SR) is given by

$$SR = \frac{V_{on}}{V_{off}} = \sqrt{\frac{V_r^2 + 2V_rV_c + NV_c^2}{V_r^2 - 2V_rV_c + NV_c^2}} \qquad (2.30)$$

The selection ratio is maximum when $V_r = \sqrt{N}$ V, , that is

$$SR = \sqrt{\frac{\sqrt{N} + 1}{\sqrt{N} - 1}} \qquad (2.31)$$

Which is same as that of APT and MAT.

The OFF pixels are biased near the threshold voltage (V_{th}) of the liquid crystal to achieve maximum contrast in the display. Hence,

$$V_{off} = \sqrt{\frac{V_r^2 - 2V_rV_c + NV_c^2}{\left(N/s\right)}} = V_{th}$$

$$V_c = \sqrt{\frac{\sqrt{N}}{2s\left(\sqrt{N} - 1\right)}} \ V_{th} \qquad (2.32)$$

$$V_r = \sqrt{N} \ V_c$$

$$V_r = \sqrt{\frac{N\sqrt{N}}{2\, s\, \left(\sqrt{N} - 1\right)}}\ V_{th} \qquad\qquad (2.33)$$

The maximum column voltage amplitude (V_c(max)) is sV_c, that is

$$V_c(\text{max}) = \sqrt{\frac{s\sqrt{N}}{2\left(\sqrt{N} - 1\right)}}\ V_{th} \qquad\qquad (2.34)$$

The amplitude of the row select voltage (V_r) (equation 2.33) and the maximum column voltage (V_c(max)) (equation 2.34) are plotted in the Figure 2-21 as a function of s considering 100 rows in a matrix LCD. As the s increases, the amplitude of row select voltage (V_r) decreases and the amplitude of the maximum column voltage (V_c(max)) increases. The amplitudes of both row select voltage and the maximum column voltage are equal when $s = \sqrt{N}$ [20].

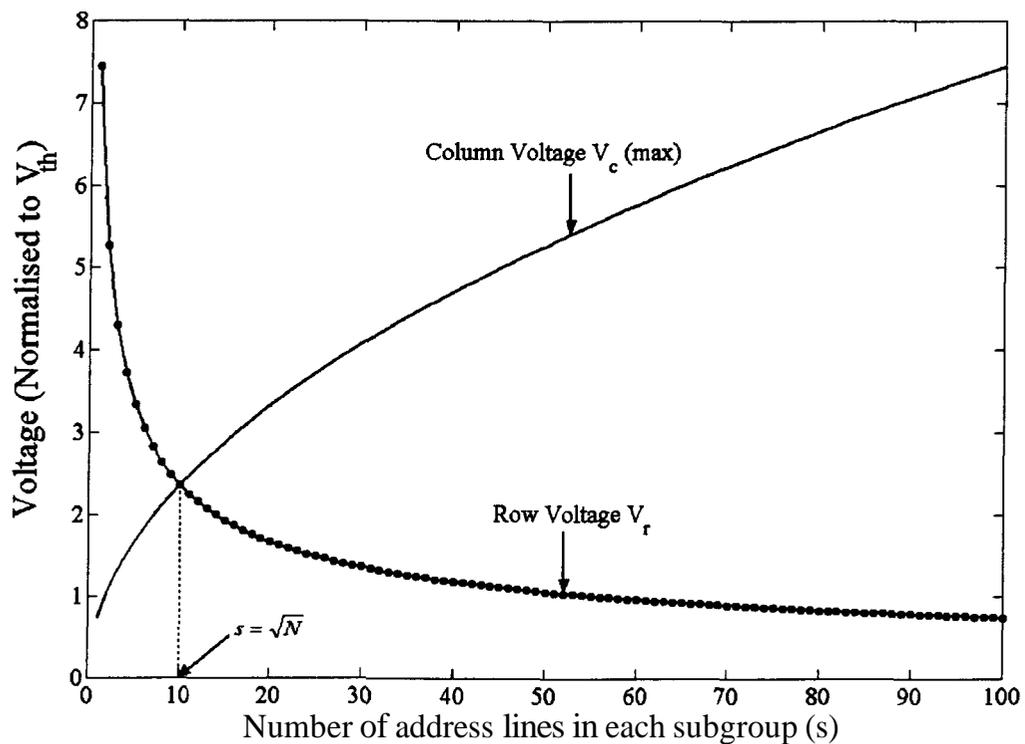Figure 2-21 Row voltage (V_r) and column voltage (V_c(max)) for N = 100 versus number of address lines selected simultaneously (s).

The supply voltage $\left(V_{sup}\right)$ of an addressing technique is calculated from the maximum voltage swing in the row and column waveforms. Hence,

Case *I*: when $\left(N \le s^2\right)$

$$V_{\text{sup}} = 2sV_c$$

$$V_{\text{sup}} = 2s\sqrt{\frac{\left(N/s\right)}{2\left(N - \sqrt{N}\right)}}\ V_{th}$$

$$V_{\text{sup}} = \sqrt{\frac{2s\sqrt{N}}{\left(\sqrt{N} - 1\right)}}\ V_{th} \tag{2.35}$$

Case II: when $\left(N \ge s^2\right)$

$$V_{sup} = 2V_r$$

$$V_{\text{sup}} = 2\sqrt{N}\ V_c$$

$$V_{\text{sup}} = 2\sqrt{N}\sqrt{\frac{\left(N/s\right)}{2\left(N - \sqrt{N}\right)}}\ V_{th}$$

$$V_{\text{sup}} = \sqrt{\frac{2N\sqrt{N}}{s\left(\sqrt{N} - 1\right)}}\ V_{th} \tag{2.36}$$

Figure *2-22* shows the supply voltage of multi-line addressing technique for various values of *s* as a function of number of address lines (N). In the same figure supply voltage of APT and IAPT are also plotted for comparison. Multi-line addressing techniques need lower supply voltages as compared to APT and IAPT when $s \ge 4$. The supply voltage requirement of MLA given in equations *2.35* and *2.36* is same as that of MAT given in equations *2.21* and *2.22* respectively. The supply voltage for multi-line addressing technique is a minimum when $N = s^2$. *In* this case the peak to peak voltage in the row waveforms ($2V_r$) and in the column waveform ($2sV_c$) are equal (Figure *2-21)* [20]. The hardware complexity of the column driver increases when more number of rows are selected at a time. That is $\left(s + 1\right)$ voltage levels are in the column waveforms while selecting *s* rows at a time. The value of *s* has a significant impact on the complexity of the

column driver. The number of lines selected simultaneously should be such that frame response is suppressed with minimum value of s. Good contrast and brightness uniformity in the display can be achieved even seven rows are selected at a time has reported by Ruckmongathan *et.al.,*[22] Same results are obtained by Clifton *et.al.,* while selecting seven rows at a time and shown that contrast degrades when less than seven lines at a time are selected [21]. As a result, by selecting seven rows at a time for large matrix LCDs hardware complexity of the column driver can be reduced considerably. Alternatively, instead of selecting one line or multiple lines at a time, all the lines in the matrix can be selected, which is discussed in the next section.
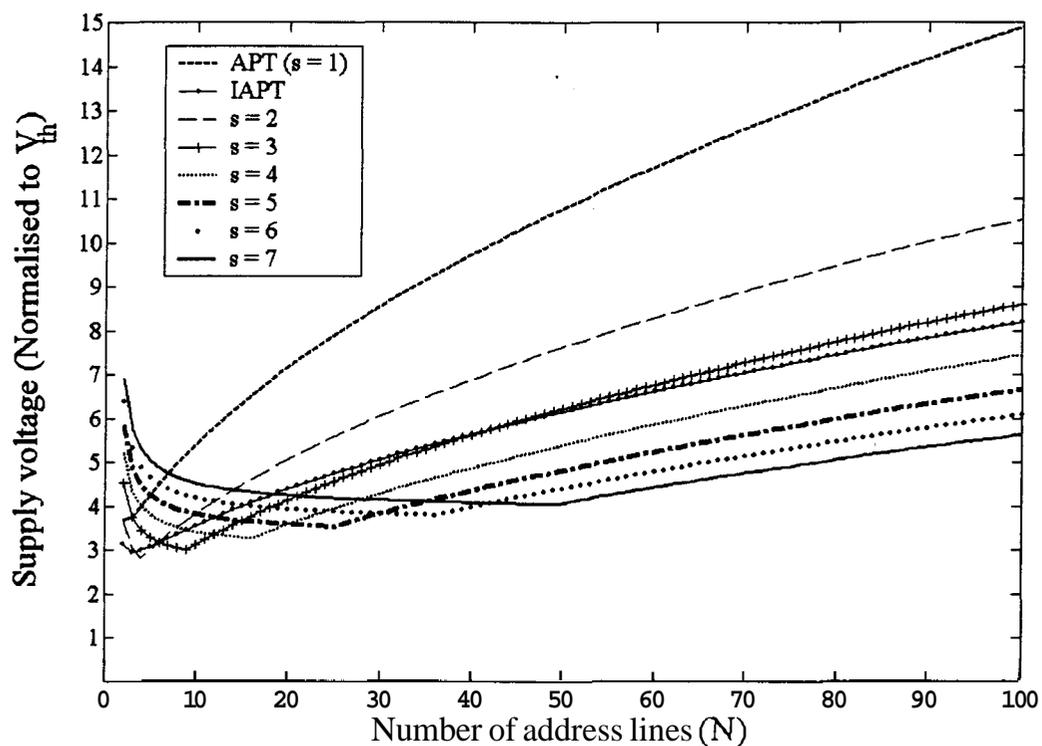

Figure 2-22 Supply voltage (normalized to V_{th}) versus N for various values of s.

2.6. All the lines at a time

The addressing technique based on selecting all the lines simultaneously is called Active Addressing technique [23]. Frame response can be easily eliminated by this technique and good contrast can be achieved even in fast responding LCDs while selecting all the lines at a time and Active Addressing is described in the next sub section.

2.6.1. Active addressing

Walsh functions of order n are used to address N rows simultaneously, wherein $2^{n-1} < N \le 2^n$. The other bilevel orthogonal functions derived from Hadamard matrices or PRBS can also be used to select all the rows. These orthogonal functions are arranged in the form of matrix, the elements in the columns of the orthogonal matrix are called row select pattern. That is $O(i,t)\,(= O(1,t), O(2,t),......,O(i,t),......,O(N,t))$ Wherein $(1 \le i \le N)$ and $(1 \le t \le q)$, q is the total number of row select patterns and it depends on the order of the orthogonal matrix. The N rows in the matrix are selected with voltages $+V_r$ or $-V_r$ corresponding to the $+1$ or -1 in the row select pattern. The data to be displayed in a column is $d_i(= d_1, d_2,......,d_i,......,d_N)$ chosen to be $+1$ for an **OFF** pixel and -1 for an ON pixel and d_i represents the data of the ith **pixel** in a column. The column voltage is the dot product between the row select pattern and the data pattern. This is ($C(t)$, normalized to V_c) mathematically represented as,

$$C(t) = \sum_{i=1}^{N} O(i,t) \cdot d_i \qquad (2.37)$$

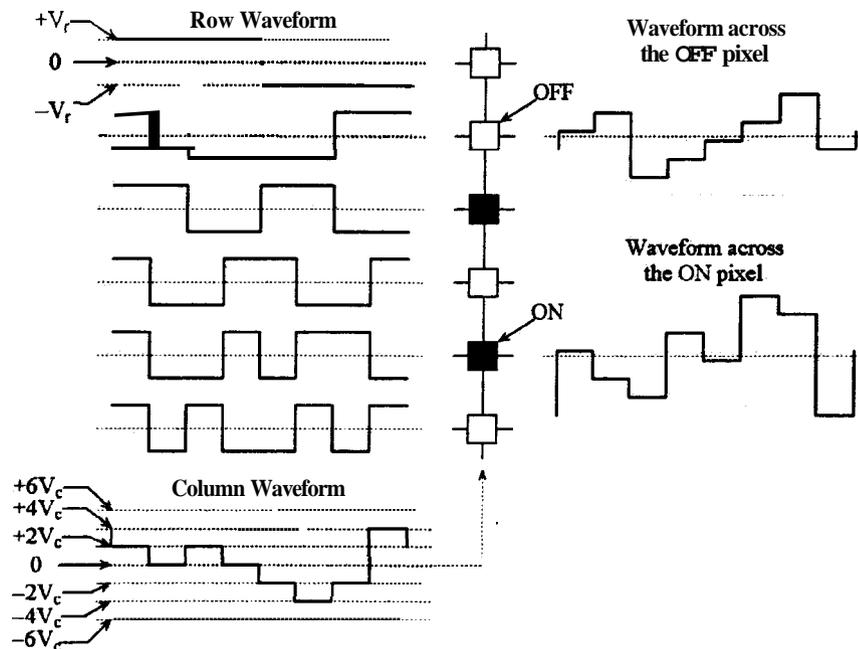The Figure 2-23 shows the typical addressing waveforms of active addressing technique.

Figure 2-23 Typical addressing waveforms of active addressing technique.

The rms voltage (V_k) across the kth pixel in a column is given by

$$V_k = \sqrt{\frac{\sum_{t=1}^{q} (O(k,t)V_r - C(t)V_c)^2}{q}}$$

(2. 38)

By substituting equation 2.37 in 2.38 and by applying orthogonality condition, after simplification the rms voltage across the pixel is given by

$$V_k = \sqrt{\frac{V_r^2 q - 2V_r V_c d_k q + NV_c^2 q}{q}}$$

$$V_k = \sqrt{V_r^2 - 2V_r V_c d_k + NV_c^2}$$

(2. 39)

If the kth pixel is ON then $d_k = -1$, thus the rms voltage across the ON pixel is given by

$$V_{on} = \sqrt{V_r^2 + 2V_r V_c + NV_c^2}$$

(2. 40)

The rms voltage across the OFF pixel when $d_k = +1$ is given by,

$$V_{off} = \sqrt{V_r^2 - 2V_r V_c + NV_c^2}$$

(2. 41)

The selection ratio (**SR**) is given by

$$SR = \frac{V_{on}}{V_{off}} = \sqrt{\frac{V_r^2 + 2V_r V_c + NV_c^2}{V_r^2 - 2V_r V_c + NV_c^2}}$$

The selection ratio (**SR**) is maximum when $V_r = \sqrt{N} \ V_c$, that is

$$SR = \sqrt{\frac{\sqrt{N} + 1}{\sqrt{N} - 1}}$$

(2. 42)

Which is same as that of the APT.

The supply voltage requirement is calculated by considering the peak to peak voltage in the addressing waveforms. The rms voltage across the OFF pixel is equated to threshold voltage (V_{th}) to get good display contrast. That is

$$V_{off} = \sqrt{V_r^2 - 2V_r V_c + NV_c^2} = V_{th}$$

$$V_c = \sqrt{\frac{1}{2\left(N-\sqrt{N}\right)}} \; V_{th}$$

(2. 43)

$$V_r = \sqrt{N} \; V_c = \sqrt{\frac{\sqrt{N}}{2\left(\sqrt{N}-1\right)}} \; V_{th}$$

The supply voltage $\left(V_{sup}\right)$ for active addressing is given by

$$V_{sup} = 2NV_c$$

$$V_{sup} = 2N \sqrt{\frac{1}{2\left(N-\sqrt{N}\right)}} \; V_{th}$$

$$V_{sup} = \sqrt{\frac{2N\sqrt{N}}{\left(\sqrt{N}-1\right)}} \; V_{th}$$

(2. 44)

The supply voltage for active address given in equation (2.44) is same as that of APT (equation (2.16)). The main advantage of active addressing is good brightness uniformity of the pixels. Address duty ratio is very high and this results in good contrast even for fast responding LCDs. The orthogonal function derived from the **PRBS** is the better choice as compared to the Hadamard or Walsh functions. This is because number of transitions in row waveforms while using **PRBS** functions is almost same for large matrices. The frequency spectrums of all the row waveforms are about same. This improves brightness uniformity of pixels in the display. The number of voltages in the column waveforms is $\left(N+1\right)$ as compared to (s+1) as in the case of IHAT or **MLA** while selecting s (i.e., N >> s) rows at a time. This increases the hardware complexity of the column driver enormously and analog column drivers are may be used as in active matrix LCDs. This increases the cost of the drive electronics. Consequently, the active addressing technique is not being used in commercial applications. The column voltage can be as large as $+ NV_c$ or $- NV_c$ depending upon data to be displayed. The probability of getting a very large amplitude of the column voltage (i.e., $\pm NV_c$) is small especially when the number of rows in the matrix display is large. The amplitudes of the column voltage have a binomial distribution with N as parameter. For large N, the binomial distribution may be approximated by normal distribution. In this case most probable column voltage levels is at

the mid level (i.e., zero) between $+NV_c$ and $-NV_c$. The large voltage levels in the column waveforms are less likely to occur. Hence, number of voltage levels in the column waveform is restricted to some reasonable value [23]. It has been reported in the literature that while driving 240 rows matrix LCD using active addressing by limiting the number of voltage levels to 64 does not affect the image quality [23]. This will results in reduction in the hardware complexity of the column driver as compared to 241 voltage levels for a 240 rows matrix display.

A multiplexed LCD in addition to displaying two level images needs to display gray shades. The techniques for displaying gray shades in passive matrix LCDs are discussed in the next section.

2.7. Displaying gray shades

Gray shades are necessary to display images such as photographs and to produce colour images from the three primary colours RGB. In LCDs the amount of light transmitted through the pixels is varied between the OFF and ON states to achieve intermediate gray shades, by applying rms voltages between the threshold voltage(V_{th}) and saturation voltage(V_{sat}) as shown in the Figure 2-24.
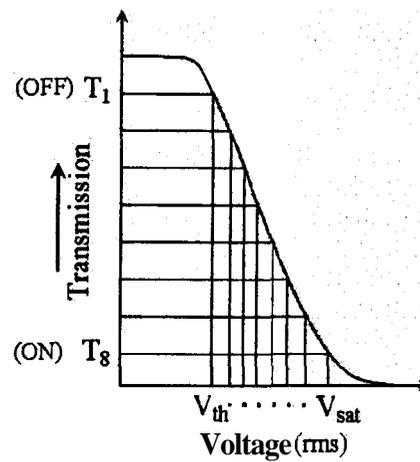

Figure 2-24 Schematic representation of electro-optic characteristics of liquid crystal display.

The various methods used for displaying gray shades in LCDs are Spatial Dither method, Pulse Width Modulation [26], Frame Modulation [27] or Frame Rate control (FRC), Amplitude Modulation or Pulse Height Modulation [28][29] and Row Pulse Height

Modulation[32]. These techniques for generating gray shades are reviewed and compared in this section.

2.7.1. Spatial Dither method

Here, pixels are subdivided into smaller areas (i.e., sub-pixels) that can be selected in any combination to give different gray shades. The sub-pixel size should be small to achieve gray shades. That is size of the sub-pixels should below the resolution of the human eye. Then collective information of sub-pixels gives the effective gray shade for that pixel. For example, using g sub-pixels of same area, then ($g + 1$) gray shades are possible as shown in the Figure 2-25. More number of gray shades (i.e., 2^g gray shades) are possible when the areas of the g sub-pixels are in the ratios 8:4:2:1. This can be achieved by splitting the rows and columns of the matrix display[24][25]. Splitting the rows doubles the number of rows, which increases the number of scanning lines and will result in decrease in contrast of the display. Columns can be split into two or more to achieve gray shades, which in turn increases the number of drivers per pixel.
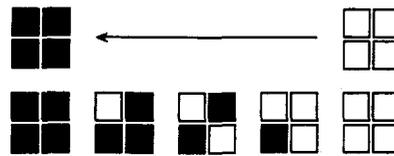

Figure 2-25 Gray shades generation using spatial dither method.

2.7.2. Pulse Width Modulation

Pulse Width Modulation (PWM) [26] is another technique used to display gray shades. Here, each row select time is divided in to g time intervals to display ($g + 1$) gray shades as shown in the Figure 2-26. For example, the row select time may be divided into four equal parts and the corresponding combinations of column voltages for displaying five gray shades are shown in the Figure 2-26. Width of the pulses decrease as the number of gray shades increase. This results presence of high frequency components across the pixels. This will result in brightness non-uniformity of pixels in the display as the number of gray shades is increased. Hence, use of pulse width modulation is usually restricted to display small number of gray shades.
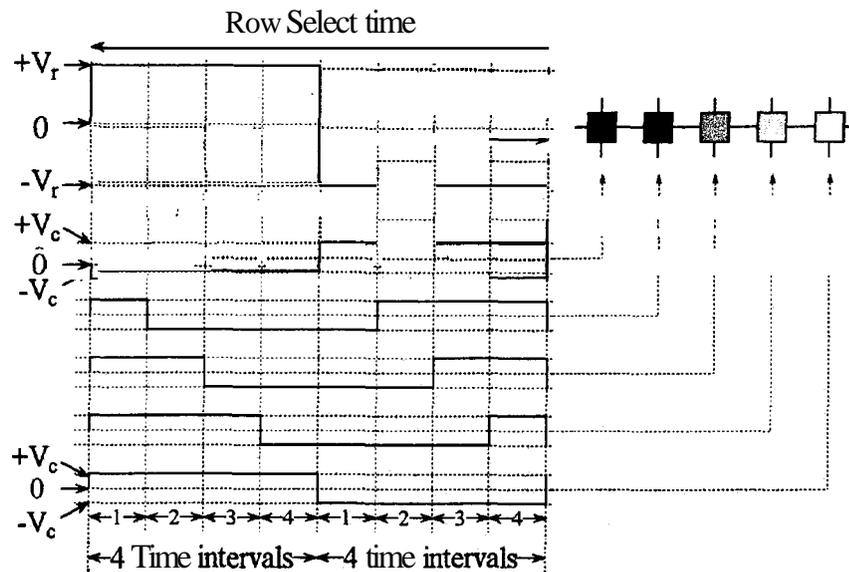
Figure 2-26 Gray shade generation using pulse width modulation method.

2.7.3. Frame Modulation

In Frame modulation [27], gray shades are displayed by turning the pixels ON and **OFF** during different frames. In the Super Twisted Nematic (STN) **LCDs,** frame modulation (or Frame Rate Control (FRC)) is widely used to display gray shades. In **FRC** g frames are used to display ($g + 1$) gray shades. FRC uses standard row and column drivers to display gray shades. Figure 2-27 shows a frame rate control method using four frames to achieve five gray shades. Flicker becomes visible as the number of gray shades increase.
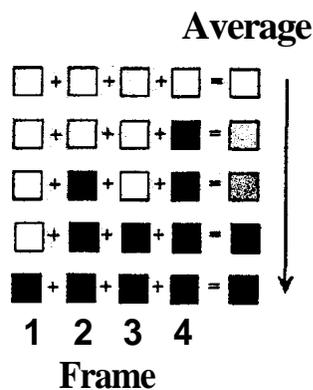

Figure 2-27 Generating gray shades using frame rate control.

2.7.4. Amplitude Modulation

In Amplitude modulation (**AM**)[28] (also referred to as Pulse Height Modulation (PHM)[29]), amplitude of the column voltage is varied to change the rms voltage across

the pixel to display gray shades. But changing the column voltage affects all the other pixels in that column. The N rows of a matrix are scanned one row at a time very similar to APT with the row select voltage V_r. The rest of the $(N-1)$ rows are grounded. The column voltages $(g_k V_c)$ are applied to the column electrode depending on the gray shade (g_k) for the pixel in the selected row. The gray value g_k takes any intermediate gray value between -1 (ON) and $+1$ (OFF). For example, when the kth $(1 \le k \le N)$ row is selected the column voltage $(g_k V_c)$ applied to the column electrode corresponds to the pixel in that column. The rms voltage across the kth pixel in a column when it is selected is given by

$$V_k(rms) = \sqrt{\frac{V_r^2 - 2g_k V_r V_c + \sum_{i=1}^{N}(g_i V_c)^2}{N}} \qquad (2.45)$$

Where, g_i is gray shade value of pixel in the ith row. In equation (2.45) the middle term $(2g_k V_r V_c)$ is the gray shade value for the kth pixel. The summation term $\sum_{i=1}^{N}(g_i V_c)^2$ will

affect the state of the kth pixel gray shade because this term is not a constant. Hence, the gray value of the kth pixel depends not only on gray shade value g_k, but also on all the other information elements from the other pixels in that column. Hence, it is necessary to make the rms voltage across the pixels independent of the data to be displayed in a column. The correction term has to be added so that the change in the column voltage should not affect the state of the other pixels. This is achieved in AM or PHM techniques using *split interval* and *full interval* methods to determine the column voltage levels to enable the desired gray levels for each pixel on the matrix LCD. These two methods are discussed in the next section.

a) Split Interval

In the split interval method the row select time is divided into two equal intervals. Two different column voltages $V_{k1} = \left(g_k + \sqrt{1 - g_k^2}\right)V_c$ and $V_{k2} = \left(g_k - \sqrt{1 - g_k^2}\right)V_c$ are applied in the first and second time intervals respectively. Where g_k is the gray value of

the kth pixel in a column and its value ranges between +1(OFF state) and −1(ON state). Typical addressing waveforms of split interval method is shown in Figure 2-28. The rms voltage across the kth selected pixel is given by

$$V_k(rms) = \sqrt{\frac{(V_r - V_{k1})^2 + (V_r - V_{k2})^2 + \sum_{\substack{i=1 \\ i \neq k}}^{N}(V_{i1}^2 + V_{i2}^2)}{2N}}$$

(2. 46)

$$V_k(rms) = \sqrt{\frac{2V_r^2 - 2V_r V_{k1} - 2V_r V_{k2} + \sum_{i=1}^{N}(V_{i1}^2 + V_{i2}^2)}{2N}}$$

$$V_k(rms) = \sqrt{\frac{2V_r^2 - 2V_r(2g_k V_c) + V_c^2 \sum_{i=1}^{N}\left(\left(g_i + \sqrt{1-g_i^2}\right)^2 + \left(g_i - \sqrt{1-g_i^2}\right)^2\right)}{2N}}$$
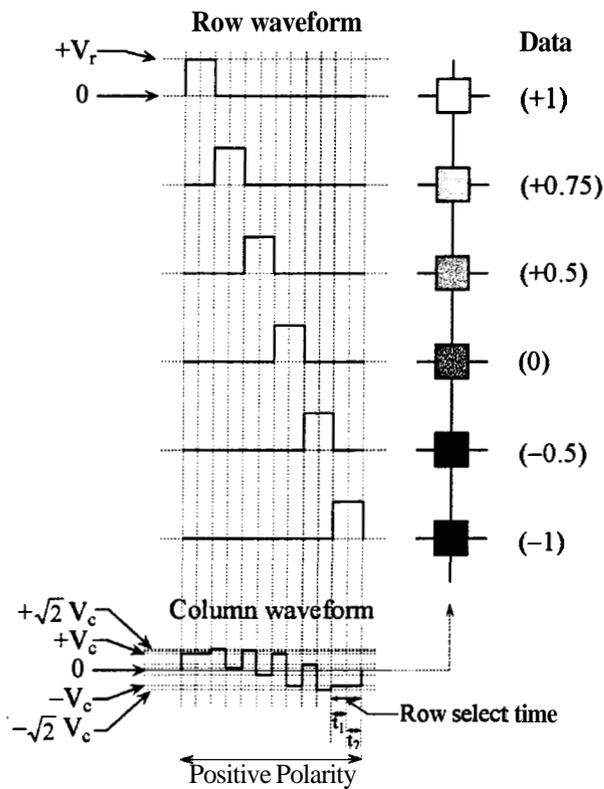

Figure 2-28 Typical addressing waveforms of displaying gray shades using split interval amplitude modulation technique.

$$V_k(rms) = \sqrt{\frac{2V_r^2 - 4V_r V_c g_k + 2NV_c^2}{2N}}$$

(2. 47)

Here, the rms voltage across a pixel depends only on g_k and does not dependent on state of other pixels. If the kth pixel is completely ON then $g_k = -1$, the rms voltage across the ON pixel is

$$V_{on} = \sqrt{\frac{V_r^2 + 2V_rV_c + NV_c^2}{N}}$$

(2. 48)

Similarly, if the kth pixel is *OFF* then $g_k = +1$, then rms voltage across the OFF pixel is

$$V_{off} = \sqrt{\frac{V_r^2 - 2V_rV_c + NV_c^2}{N}}$$

(2. 49)

The selection ratio (SR) is maximum when $V_r = \sqrt{N} \; V_c$, that is

$$SR = \frac{V_{on}}{V_{off}} = \sqrt{\frac{\sqrt{N} + 1}{\sqrt{N} - 1}}$$

(2. 50)

Which is same as APT with out gray shades. The supply voltage $\left(V_{sup}\right)$ requirement is same as that of APT and is determined by maximum swing in the addressing waveforms.

$$V_{sup} = \sqrt{\frac{2N\sqrt{N}}{\left(\sqrt{N} - 1\right)}} \; V_{th}$$

(2. 51)

Figure 2-29 shows the column voltage V_{k1} and V_{k2} (normalized to V_c) to display gray shades $-1 \; \text{I} \; g_k \; \text{I} +1$, wherein V_c is the amplitude of the column voltage with out gray shades. Maximum amplitude of the column voltage is $\sqrt{2} \; V_c$ and the amplitude of row voltage is V_r, where $V_r = \sqrt{N} \; V_c$. Supply voltage can be reduced even in this case by modifying the addressing waveforms as in the case of APT. Both row and column voltages are shifted by $+\sqrt{2} \; V_c$, when row select voltage is positive (i.e., $+V_r$). When the row select voltage is negative (i.e., $-V_r$), both row and column voltages are shifted by $+V_r$. These shifts in the addressing waveforms of both rows and columns do not alter the rms voltage across the pixels. This is because both row and column voltages are shifted by the same amount. The selection ratio is same as that of APT. Supply voltage is reduced to $\left(V_r + \sqrt{2} \; V_c\right)$ instead of $2V_r$. The number of voltage levels in the column waveforms doubles due to the modification in the addressing waveforms.
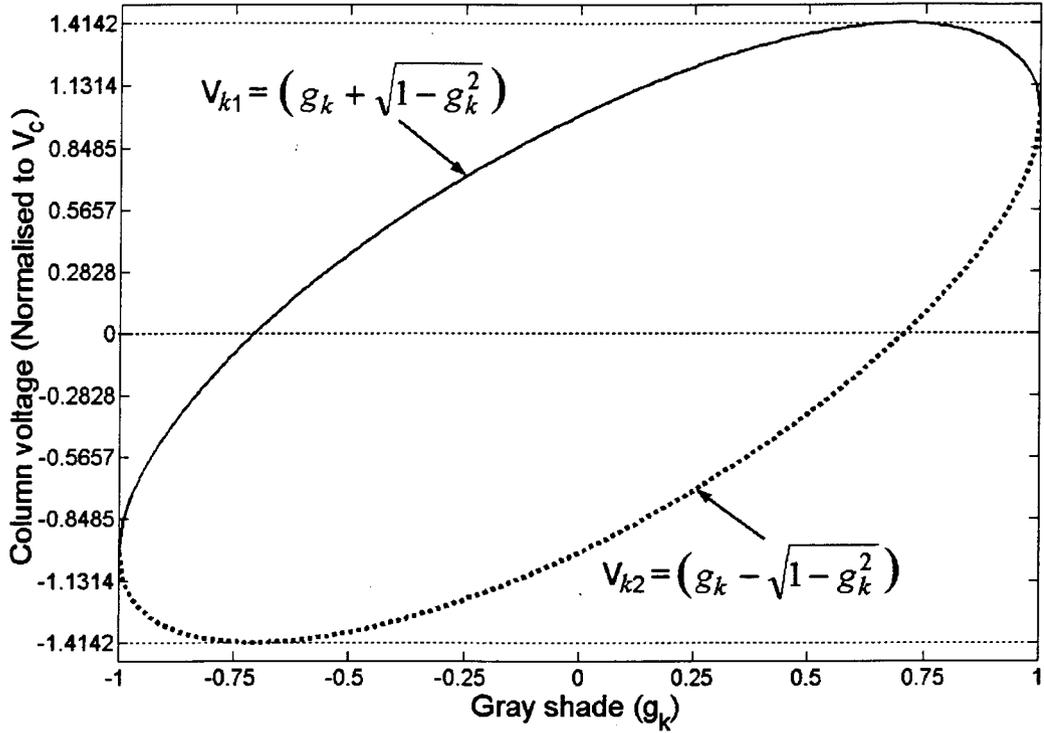
$$V_{k1} = \left(g_k + \sqrt{1 - g_k^2} \right)$$

$$V_{k2} = \left(g_k - \sqrt{1 - g_k^2} \right)$$

Figure 2-29 **Column voltage (Normalized to V_c) V_{k1} and V_{k2} in to time intervals t1 an t2 for displaying gray shades using split interval amplitude modulation technique.**

b) Full Interval

In full interval method [29], the expression for rms voltage across the kth pixel can be made independent of the gray value of other pixels in that column by adding $(N+1)^{th}$ additional row called virtual row. A virtual information that is correction term $d_{(N+1)}$ is added at the $(N+1)^{th}$ interval for the $(N+1)^{th}$ row. Typical addressing waveforms of full interval method is as shown in Figure 2-30. The rms voltage across the kth pixel is given by,

$$V_k(rms) = \sqrt{\frac{V_r^2 - 2g_k V_r V_c + \sum_{i=1}^{N} (g_i V_c)^2 + (d_{(N+1)} V_c)^2}{N+1}} \qquad (2.52)$$

Where,

$$d_{(N+1)} = \sqrt{N - \sum_{i=1}^{N} (g_i)^2} \qquad (2.53)$$

Then the rms voltage across the kth pixel is given by

$$V_k(rms) = \sqrt{\frac{V_r^2 - 2g_k V_r V_c + N V_c^2}{N+1}}$$

(2. 54)

As a result, rms voltage for any pixel in a column depends only on the gray shade information element for that pixel, and not on the state of any other pixel in that column. This is because last term in the numerator of equation (2.54) is a constant. The only term that will change the gray shade of the selected pixel is the middle term i.e., $2g_k V_r V_c$. The selection ratio is the same as that of APT even after adding additional row so called virtual row. This additional $(N+1)^{th}$ row need not be physically present in the display. Only $(N+1)^{th}$ row select time slot must be present and the correction term is applied to the columns during this time interval.
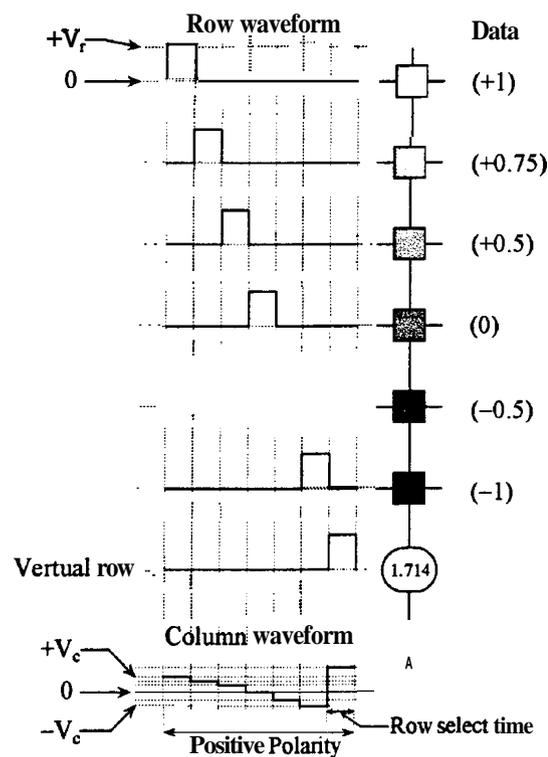

Figure 2-30 Typical addressing waveforms of full interval amplitude modulation technique for displaying gray shades by selecting one row at a time.

Typical waveforms of full interval amplitude modulation [29] using active addressing is as shown in the Figure 2-31. Here also $(N+1)^{th}$ virtual row must be added. The column voltage is the dot product of the row select pattern and the data vector for a given column

as in the case of active addressing without gray shades. The correction term has to be added to the column voltage so that pixels will get the gray shade information assigned to it. Thus, the column voltage after adding the correction term is given by

$$C(t) = \sum_{i=1}^{N} O(i,t) \cdot d_i + O(N+1,t) \cdot d_{N+1}$$

(2. 55)

Where d_{N+1} is the correction term and is given by,

$$d_{N+1} = \sqrt{N - \sum_{i=1}^{N} (d_i)^2}$$

(2. 56)

This will ensure that rms voltage across the pixel depends only on the gray shade information of that pixel and not on the state of the any other pixels in that column. The selection ratio is maximum and same as that of Alt and Pleshko technique.
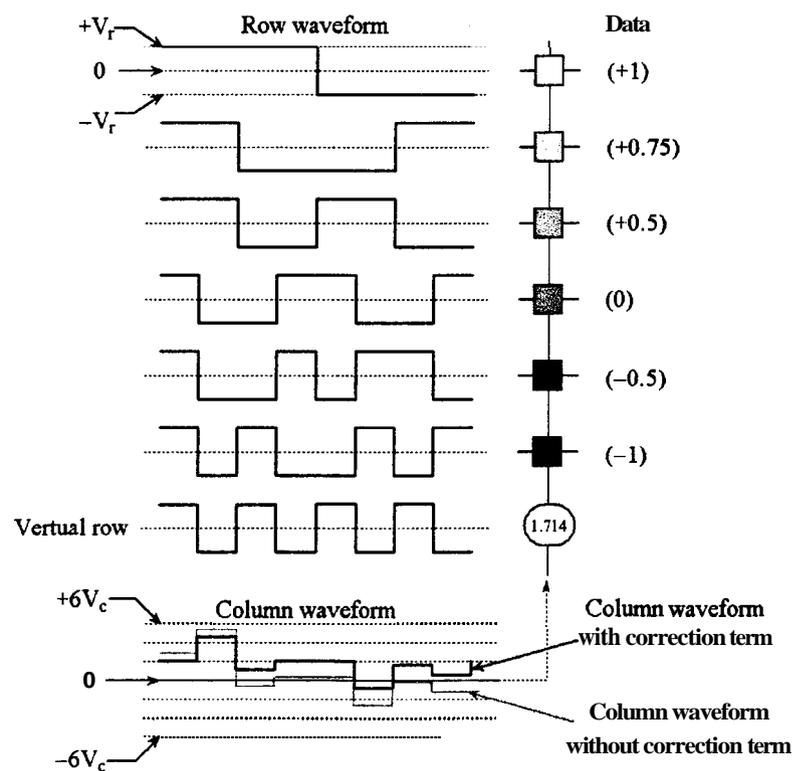

Figure 2-31 Typical addressing waveforms of active addressing amplitude modulation technique for displaying gray shades.

In the case of MLA [20][28][30] an additional virtual row is introduced for every subgroup. This virtual row is considered only for the computation of column voltage and is

not present on the display panel. The column voltage when the kth subgroup is selected for displaying gray shades is given by

$$C_{ks+i}(t) = \sum_{i=1}^{s} \left(O(i,t) \cdot d_{ks+i} \right) + O(s+1,t) \cdot d_{k(s+1)} \qquad (2.57)$$

Where d_{ks+i} is the data for the ith pixel $(1 \le i \le s)$ in the kth $\left(0 \le k \le \left(\dfrac{N}{s} - 1 \right) \right)$ subgroup

and d_{s+1} is the correction term for the kth subgroup and is given by,

$$d_{k(s+1)} = \sqrt{s - \sum_{i=1}^{s} (d_{ks+i})^2} \qquad (2.58)$$

Here, the correction is done for each subgroup. Hence the large amplitude correction term (see equation 2.56) will not be present as in contrast to the fulltime PHM technique [29]. The selection ratio is the maximum and it is same as that of Alt and Pleshko technique. Just one-frame is adequate to achieve the desired gray shade. Hence, a large number of gray shades may be displayed without flicker and brightness non-uniformity. However, the number of voltage levels in the column waveforms is high. Hence, analog column drivers are necessary for displaying gray shades. This will increase the hardware complexity and hence cost of the drive electronics. In general, the split interval line by line addressing method requires fewer simultaneously accessible voltages than other methods like full interval method based on Alt and Pleshko Technique, Multi-Line Addressing or Active Addressing. Split interval amplitude modulation technique requires g simultaneously accessible voltage levels in the column waveforms. Gray shades can be displayed by combining amplitude modulation and frame rate control methods [31]. In this case the number of voltage levels in the column waveform can be reduced considerably. If the gray shades in the first frame are equally spaced then the increase in number of gray shades in combination with FRC does not increase in the number of gray shades. On the other hand if the gray shades are not evenly spaced then their combination over successive frames gives large number of gray shades. In this case the number of gray shades increases almost exponentially with the number of frames used [31].

2.7.5. *Row pulse height modulation*

Here, the amplitudes of the row waveforms are varied in the successive time intervals. The amplitude is reduced by a factor 2 in the successive time intervals from the most significant bit (MSB) to the least significant bit (LSB) [32]. The column signal is generated for each time interval independently by considering data from MSB to LSB. Here, 2^g gray shades may be displayed by dividing each row select time to g equal time intervals. The number of column voltage levels are $(s+1)$, where s is the total number of rows selected simultaneously. The number of voltage levels in the column waveform and their amplitudes are same in all the frames. Hence, the column driver complexity is the same as in the case of displaying bilevel images. Typical addressing waveforms of row pulse height modulation is shown in the Figure 2-32.
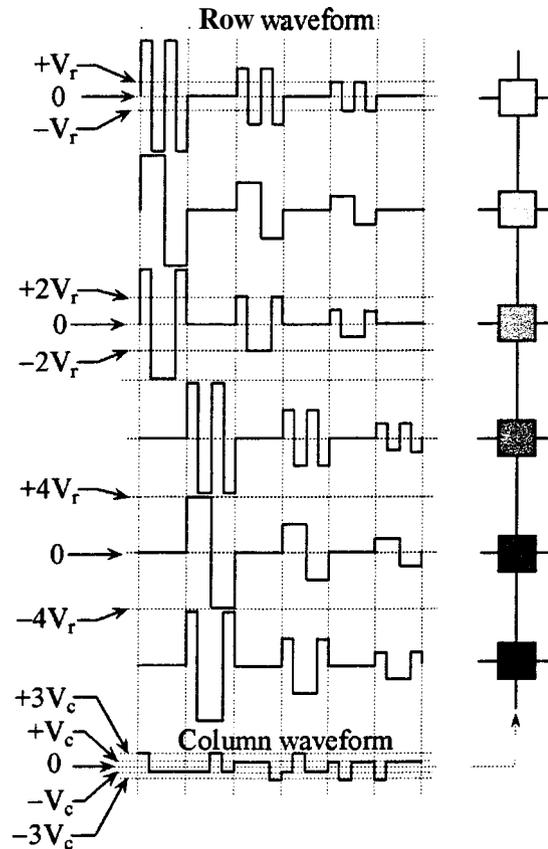

Figure 2-32 Typical addressing waveforms of row pulse height modulation using multi-line addressing technique.

The rms voltage across the ith pixel, $(1 \le i \le s)$ in the kth subgroup $\left(0 \le k \le \left(\dfrac{N}{s}-1\right)\right)$ for displaying 2^g gray shades using g frames is given by

$$V_{ks+i}(rms) = \sqrt{\frac{\sum\limits_{f=1}^{g}\left(\kappa_f^2 V_r^2 q - 2\kappa_f V_r V_c d_{(f,ks+i)}q + gNV_c^2 q\right)}{g\left(N/s\right)q}}$$

(2.59)

Where, data $d_{(f,ks+i)}$ corresponds to f^{th} bit out of g bits (from MSB) for the ith pixel in the kth subgroup represented in binary format, wherein logic 0 and logic 1 are considered as +1 and −1, respectively. q is the number of row select patterns in the orthogonal matrix, s is the number of rows in each subgroup and N is the number of rows in the matrix LCD.

Column voltage is given by $C_{(f,k)}(j) = \sum\limits_{i=1}^{s}\left[O(i,j)d_{(f,ks+i)}\right]V_c$, where $O(i,j)$ is the element of the orthogonal matrix and columns of this matrix are used as row select patterns. The row voltage is decreased from MSB to LSB by a factor two, that is if the row select voltages are $\kappa_1 V_r, \kappa_2 V_r, \kappa_3 V_r, \ldots\ldots\kappa_g V_r$ from MSB to LSB then $\dfrac{\kappa_f}{\kappa_{f+1}} = 2$ wherein

$\kappa_f = 2^{g-f}$. From equation (2.59), the rms voltage across the ON and OFF pixel is given by

$$V_{on} = \sqrt{\frac{\left(\dfrac{2^{2g}-1}{3}\right)V_r^2 + 2\left(2^g - 1\right)V_r V_c + N\ g\ V_c^2}{\left(\dfrac{N\ g}{s}\right)}}$$

(2.60)

$$V_{off} = \sqrt{\frac{\left(\dfrac{2^{2g}-1}{3}\right)V_r^2 - 2\left(2^g - 1\right)V_r V_c + N\ g\ V_c^2}{\left(\dfrac{N\ g}{s}\right)}}$$

(2.61)

The selection ratio is optimum when $V_r = \sqrt{\dfrac{3\ N\ g}{2^{2g}-1}}\ V_c$, that is

$$SR = \sqrt{\frac{\sqrt{N\,g\left(2^{2g}-1\right)} + \sqrt{3}\left(2^{g}-1\right)}{\sqrt{N\,g\left(2^{2g}-1\right)} - \sqrt{3}\left(2^{g}-1\right)}}$$

<div align="right">(2. 62)</div>

The selection ratio of this technique is lower than the maximum. The supply voltage increases when the amplitude of the row waveform is decreased in the successive time intervals. Hence, this technique [32] has been demonstrated in combination with MLA to reduce the supply voltage and suppress the frame response.

2.8. *Displaying restricted pattern*

Liquid crystal displays are used in many applications like Logic analyzers, **ECGs** and Oscilloscopes. In these displays waveforms are displayed, which are single valued function of time. If the matrix size is large then'one can display waveforms with reasonable good resolution. In passive matrix **LCDs** as the number of rows increases the selection ratio decreases [4], which in **turn** decreases the contrast ratio. For example, while displaying single waveform in a display with N rows and M columns, only one pixel in each column carry information and rest of the pixels are background pixels. This restriction as compared to general pattern gives some flexibility while addressing the LCD to improve the display performance. Several addressing methods for displaying waveforms are briefly reviewed in the following sections.

2.8.1. *Displaying single waveform*

In the year 1978, Shanks *et.al.,* have developed an addressing technique for displaying single **waveform[33]**. This technique exploits the fact that only one pixel in each column carries the information (**i.e.,** points on the waveform). This is because waveforms are single valued functions of time. The rows of a matrix LCD are selected sequentially one at a time with a voltage $\left(V\right).$ The column voltage is chosen to be V (in phase with the row select voltage) for an OFF pixel and zero for an ON pixels. Figure 2-33 shows the typical addressing waveforms to display single waveform based on this technique. Here, the rms voltage across the OFF pixels is zero (**i.e.,** points on the waveform) and $\sqrt{\dfrac{2}{N}}$ V across the ON pixels. Hence, the selection ratio is infinite for this technique. The rms voltage across the OFF pixels is lower as compared to the ON pixels. Hence, the waveform looks bright

in the dark background in normally white mode TN **LCDs.** The technique has dc free operation with one frame. Hence, there is no need to reverse the polarity after every frame. Supply voltage is determined by the maximum swing in the addressing waveforms and is equal to V in this case. Here the ON pixels are biased near the saturation voltage (V_{sat}). The supply voltage for this technique is given by

$$V_{on} = \sqrt{\frac{2}{N}} \; V = V_{sat}$$

$$V_{sup} = V$$

$$V_{sup} = \sqrt{\frac{N}{2}} \; V_{sat} \qquad\qquad (2.63)$$

In summary, the selection ratio is infinity and'it is independent of the matrix size. But the supply voltage increases as the matrix size increases and is given by equation (2.63).
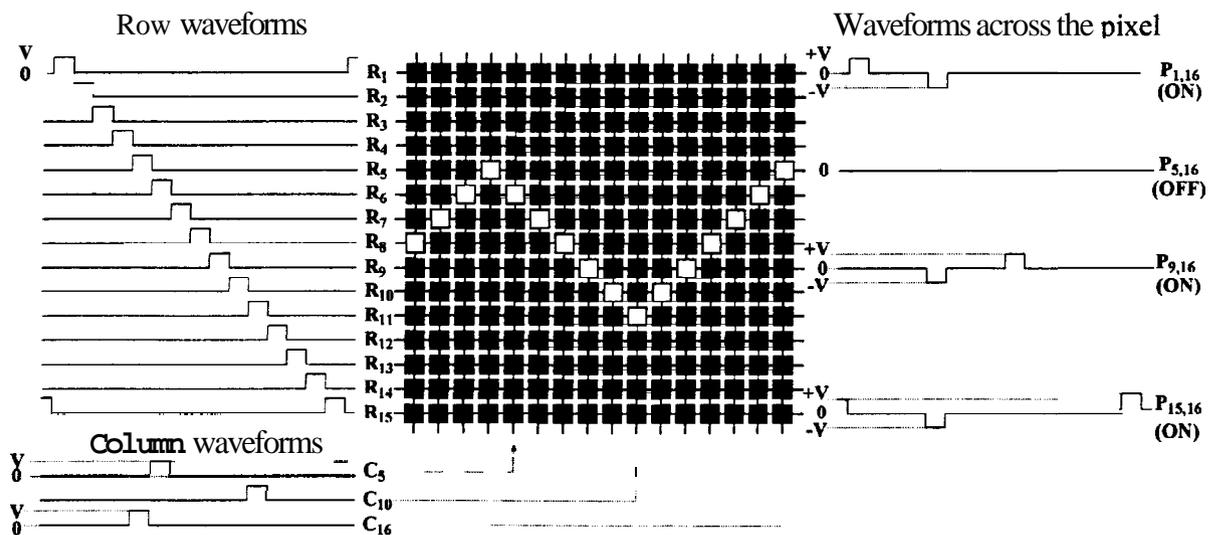

Figure 2-33 Typical addressing waveforms to display single waveform

Selection ratio can be improved as compared to Alt and Pleshko limit when the number of selected pixels in a column is constant. In this case **Kmetz** and **Nehring** have show that the selection ratio depends on number of information carrying pixels in a column [5]. In this case the optimum selection ratio is given by

$$SR = \sqrt{\left[1 + \frac{N}{\sqrt{n(N-n)(N-1)} - n}\right]} \quad \text{for} \quad 0 < n < (N-1) \qquad (2.64)$$

Where, N is the number of rows in a matrix display and n is the number of ON pixels in each column. Selection ratio is infinite when n is (N − 1) which means that only one pixel in each column carries the information. This is same as in the case of displaying single waveform as Shanks and Holland [33]. Selection ratio is a minimum when n is $\dfrac{\left(N - \sqrt{N}\right)}{2}$ and it is equal to that of Alt and Pleshko technique [4]. Selection ratio is higher when the most of the pixels are ON as compared to the case when most of the pixels are OFF. Hence, negative contrast mode has a higher selection ratio as compared to the positive contrast.

Shanks and Holland have demonstrated a technique for displaying single waveform [34] by using Pseudo Random Binary Sequence (PRBS) as row waveforms. All the rows are selected simultaneously using PRBS and its shifted versions as shown in the Figure 2-34. The PRBS can be generated from a shift register with EX-OR or EX-NOR feedback. The maximum length of the PRBS is $\left(2^{L} - 1\right)$, where L is the number of bits used in the shift register to generate the sequence. The PRBS is chosen depending on the number of rows to be multiplexed i.e., $\left(2^{L-1} - 1\right) < N \le \left(2^{L} - 1\right)$. The rms voltage difference between any two waveforms except for zero delay has the constant value and it is zero for the zero delay. The column waveform is chosen exactly same as that of the row waveforms for a selected pixels (i.e., points on the waveforms). This results in zero rms voltage across the selected pixels and constant rms voltage across the rest of the pixels (i.e., background pixels). Hence, the selection ratio is infinite even in this technique. The typical addressing waveforms for displaying single waveform is shown in the Figure 2-34. The ON pixels get a higher rms voltage as compared to the OFF pixels resulting in the negative contrast mode (i.e., bright waveform on dark background) in normally white mode TN LCDs. As one see in the Figure 2-34 the maximum swing in the addressing waveforms is V. The ON pixels are biased to the saturation voltage $\left(V_{sat}\right)$. The rms voltage across the ON pixel is given by

$$V_{on} = \sqrt{\frac{2^{L-1}}{2^{L} - 1}} \; V = V_{sat}$$

$$V_{sup} = V = \sqrt{\frac{2^L - 1}{2^{L-1}}} \ V_{sat}$$

Since, all the rows are selected simultaneously, the address duty ratio is high i.e., $\left(\frac{2^{L-1}}{N}\right)$

as compared to $\left(\frac{1}{N}\right)$ while selecting one row at a time. Supply voltage in this case is lower than selecting one row at a time. Here, the supply voltage is independent of the matrix size and is almost equal to $\sqrt{2} \ V_{sat}$.
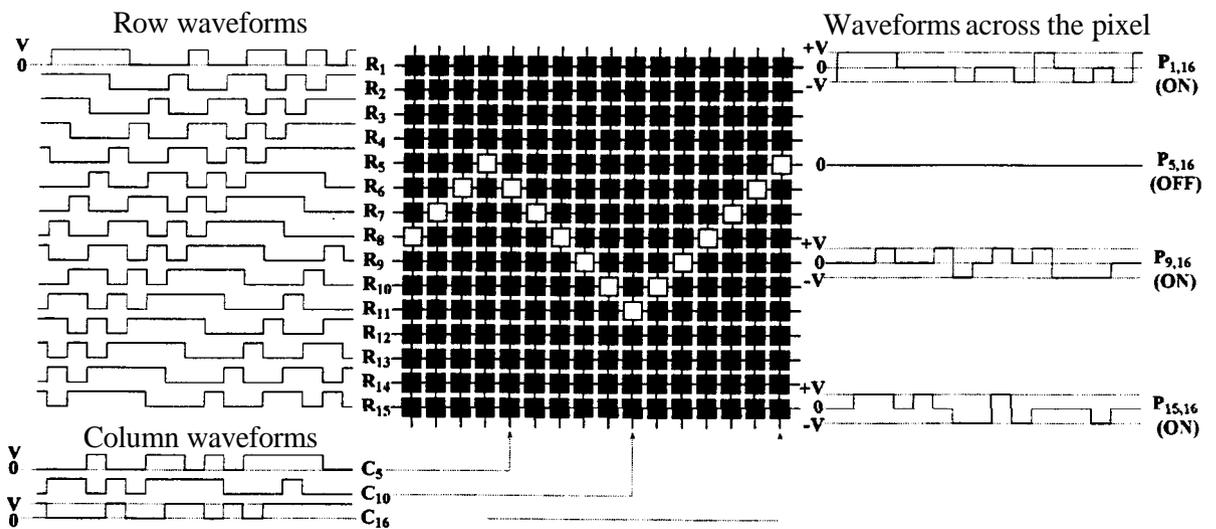

Figure 2-34 Typical addressing waveforms for displaying single waveforms selecting all the rows using pseudo random sequence.

In many applications one has to display more than one waveform. In one technique [35] it has been shown that alternate columns (i.e., vertical electrodes) are used to display two waveforms. In this case horizontal resolution is sacrificed due to the interleaved column electrodes. Selection ratio in this case is again infinite, but horizontal resolution is decreased. Alternatively, multiple waveforms are displayed one after the other repetitively in sequential frames [35]. Here, horizontal resolution is restored, but selection ratio is decreased. Selection ratio decreases because, OFF pixels (i.e., points on the waveforms) will also get some voltage during the $(w-1)$ frames, where w is the number of waveforms to be displayed.

2.8.2. Displaying multiple waveforms

Restricted Pattern Addressing Technique (RPAT)[36] and Pseudo Random Binary Sequence (PRBS) technique [37] are useful for displaying multiple waveforms with higher selection ratio than conventional techniques. These techniques are briefly outlined in the following sections.

2.8.2.1. Restricted Pattern Addressing Technique

Here, scanning is done by selecting one row at a time. If w waveforms to be displayed in a matrix display with N rows and M columns, only w pixels in each column carry the information and the rest of the (N − w) pixels in each column are background pixels. The rows are selected with a voltage $\pm V_r$, and the unselected rows are connected to ground. The sign of the column voltage (V_c) is chosen to be same as that of the row select pulse for the information carrying pixels and zero for the background pixels. This is same as assigning +1 as the data to the w pixels (i.e., points on the waveforms), and 0 as the data to the background pixels. Here, w pixels in each column get lower rms voltage as compared to the background pixels. Hence, the selected pixels (i.e., points on the waveforms) look bright in dark background. This results in Negative Contrast (NC) in normally white mode TN LCDs. This technique is referred to as Restricted Pattern Addressing Technique – Negative Contrast (RPAT – NC). Typical addressing waveforms of RPAT–NC is shown in Figure 2-35. Similarly the column voltage for the w pixels can be chosen to be out of phase with the row select voltage. In this case the selected pixels gets higher rms voltage as compared to the background pixels, results in Positive Contrast(PC). This technique is referred as Restricted Pattern Addressing Technique – Positive Contrast (RPAT – PC). The typical addressing waveforms of RPAT–PC is shown in Figure **2-36.** In both the cases (i.e., PC and NC) the selection ratio is independent of the matrix size and just depends on number of waveforms to be displayed. As mentioned earlier if the number of ON pixels are more as compared to number of OFF pixels, selection ratio is higher. Similarly, the selection ratio of RPAT–NC is higher than RPAT–PC. The selection ratio for RPATs is optimum when $V_r = \sqrt{w} \ V_c$ and is given by

$$SR = \sqrt{\frac{\sqrt{w}}{\sqrt{w}-1}} \qquad \text{for RPAT − NC} \qquad (2.66)$$

and

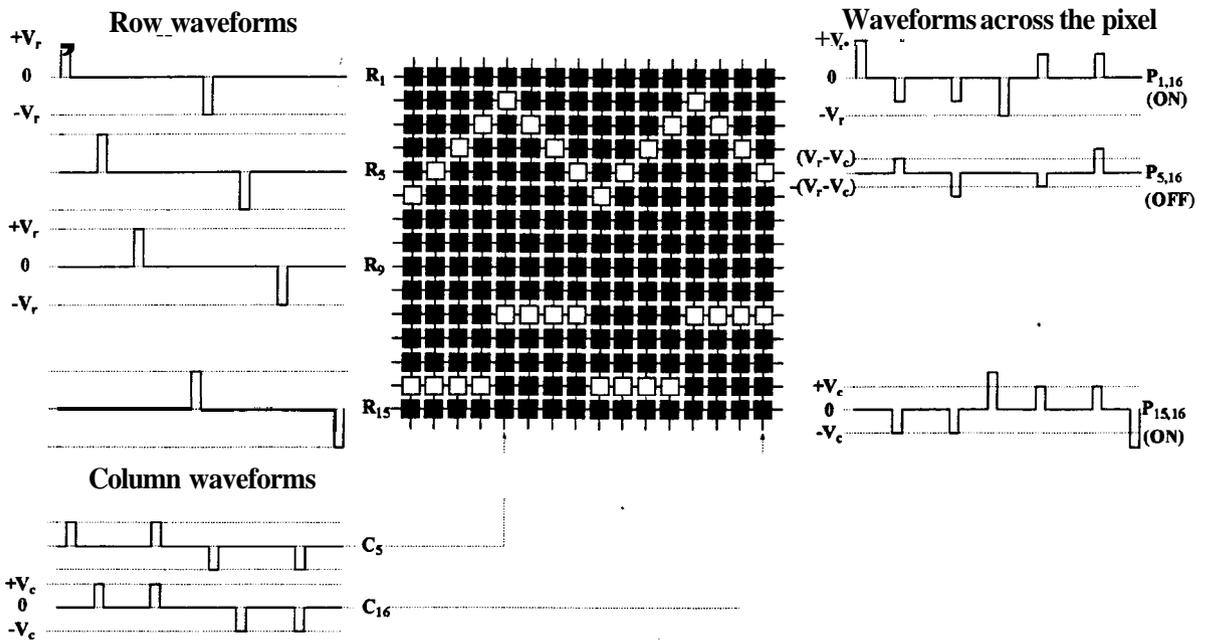$$SR = \sqrt{\dfrac{\sqrt{w}+1}{\sqrt{w}}} \qquad \text{for RPAT} - \text{PC} \qquad\qquad (2.67)$$

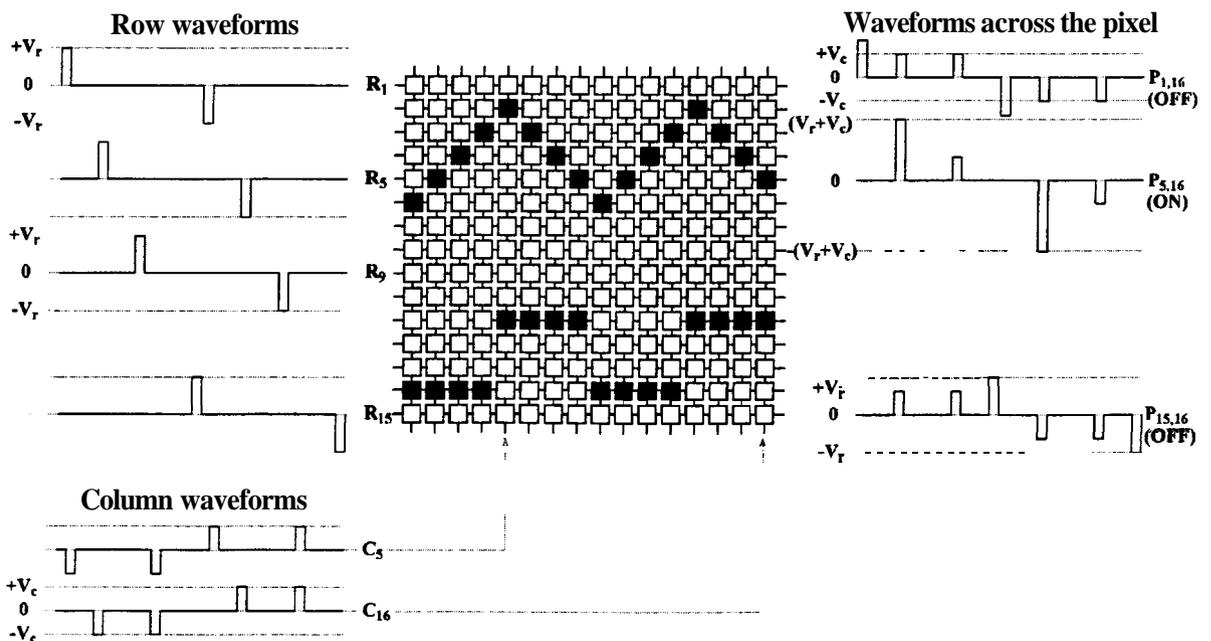Figure 2-35 Typical addressing waveforms of RPAT-NC, displaying two waveforms.

Figure 2-36 Typical addressing waveforms of RPAT-PC, displaying two waveforms.

The selection ratio in both the cases is independent of the total number of rows (N) in the matrix. It is clear from the above equations **(2.66)** and **(2.67)** the selection ratio is higher

for negative contrast mode as compared to the positive contrast mode and is shown in Figure 2-37. The main advantage of RPATs is that, the TN LCDs can be used even for large matrix LCDs to display multiple waveforms. This is because selection is higher as compared to the conventional addressing technique while displaying general pattern. The electro-optic curve of the TN LCDs are not very steep, hence, it is not possible to multiplex more number of rows. For example to display 9 waveforms in negative contrast is equivalent to driving matrix LCD having 25 rows. Hence, good contrast ratio can be achieved even in TN LCDs with large matrix size. As already explained, the selection ratio of both RPAT-NC and RPAT-PC are independent of matrix size. The supply voltage requirement of RPATs increases with matrix size (N). The supply voltage for an addressing technique is determined by the maximum voltage swing in the addressing waveforms (i.e., both row and column). The maximum swing in the addressing waveforms in RPAT–NC and RPAT–PC is $2V_r$ as shown in the Figure 2-35 and Figure 2-36. Like IAPT, the maximum swings can be reduced to V_r for RPAT-NC and $(V_r + V_c)$ for the case of RPAT–PC. The row and column voltages of these techniques are modified as tabulated in Table 2-5.
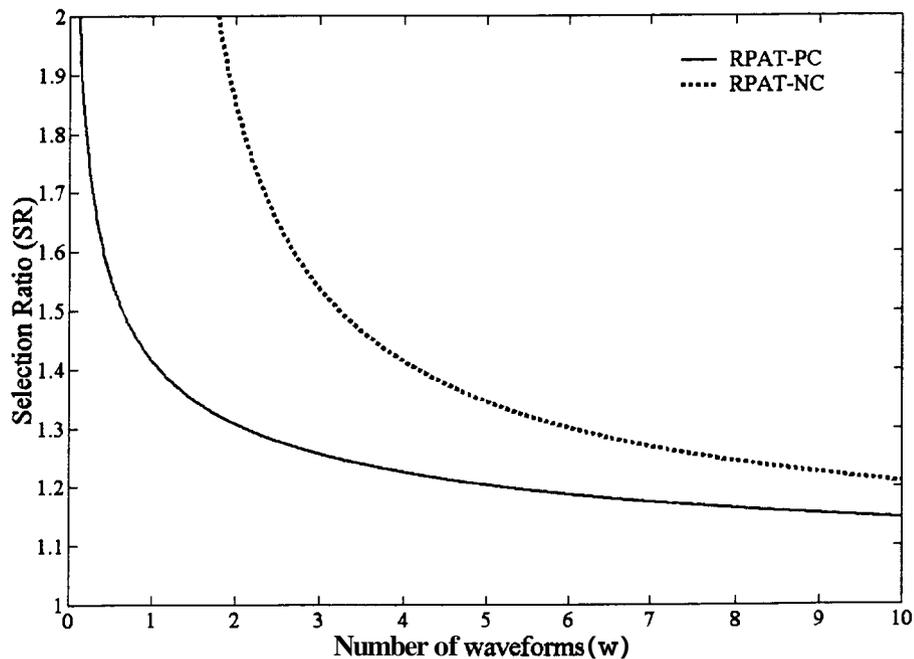

Figure 2-37 Selection Ratios versus number of waveforms for RPAT–NC and RPAT–PC.

Table 2-5

RPAT−NC	Modified RPAT−NC
When row select voltage is $+V_r$	No change
When row select voltage is $-V_r$	Shift both row and column waveforms by $+V_r$

RPAT−PC	Modified RPAT−PC
When row select voltage is $+V_r$	Shift both row and column waveforms by $+V_c$
When row select voltage is $-V_r$	Shift both row and column waveforms by $+V_r$

Typical addressing waveforms of modified row and column waveforms of RPAT-NC and RPAT-PC are shown in the Figure 2-38 and Figure 2-39. Hence, supply voltage for **RPATs** can be reduced, but the instantaneous voltage across any pixel in a display addressed with RPATs is zero during most of the time intervals and this may lead to the flicker when N is very large. This problem is over come by the addressing technique proposed by Ruckmongathan in the year 1996. This technique is based on the selecting all the rows at a time as in the case of active addressing referred to as Pseudo Random Binary Sequence (PRBS) technique [37].
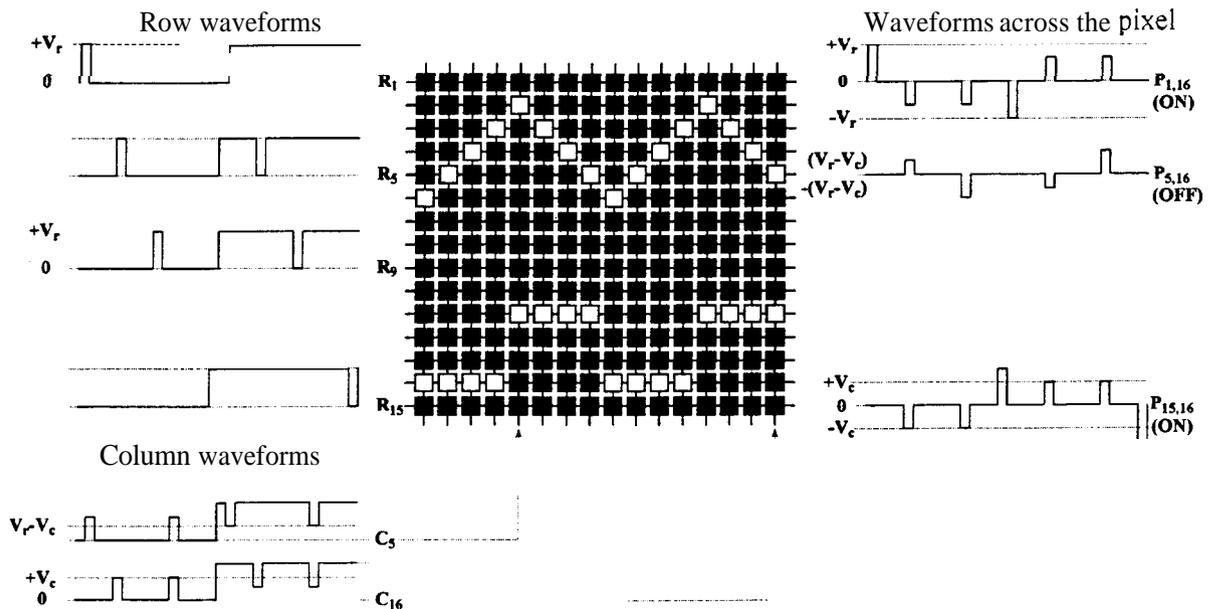

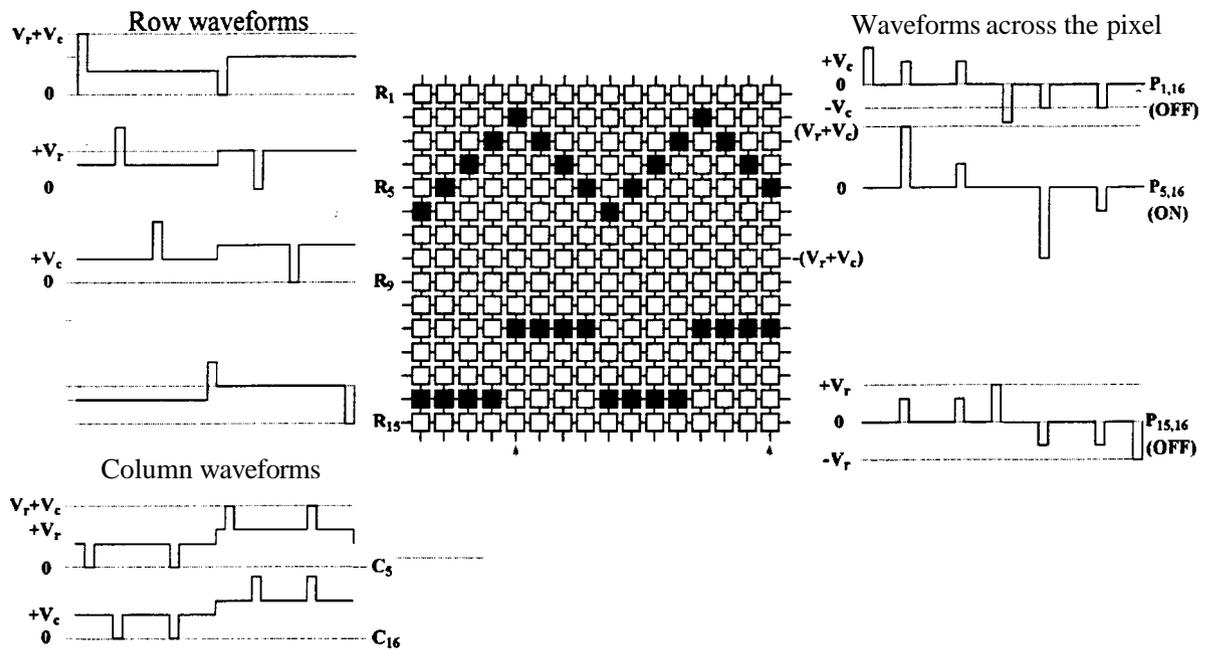**Figure 2-38 Typical addressing waveforms of modified RPAT−NC.**

Figure 2-39 Typical addressing waveforms of modified RPAT-PC .

2.8.2.2. *Pseudo Random Binary Sequence (PRBS) Technique*

Here the N rows in the matrix display are driven with waveforms corresponding to a set of orthogonal functions. Simple orthogonal functions derived from Walsh, Hadamard or PRBS are preferred than those derived from Sine and Cosine functions. These orthogonal functions have just two values +1 or −1. Hence, the generation of row and computation of column waveforms are simpler and easy for hardware implementation. The orthogonal functions derived from PRBS are preferred as compared to Walsh and Hadamard matrices. The main advantage is that the number of transitions in the row waveforms is almost constant. Also, they can be generated from a shift register with EX-OR or EX-NOR feedback or from a ROM storing one of the sequences. The pseudo random sequence used by Shanks and Holland for displaying single waveform is not orthogonal. It can be converted to orthogonal, and this has been used in PRBS technique [37]. The generation of pseudo random binary sequence and converting to its orthogonal form are given in Appendix B. The addressing waveforms applied to the matrix LCDs get distorted due to the resistance of the indium tin oxide and the capacitance of the pixels. Error in the rms voltage across the pixels due to distortion in the waveforms is same for all the pixels as the number of transitions are almost equal for PRBS. This will result in brightness uniformity of pixels. Frequency spectrum of these waveforms is also same since they are almost identical except for the shift in the time domain. This is the advantage of using PRBS as

row select pattern as compared to the row select pattern generated by Walsh or Hadamard matrices. Column waveforms are generated by taking the orthogonal transform of the data to be displayed. That is column voltage is the dot product between row select pattern and the data vector. The data assigned to the background pixel is zero, as in the case of RPATs. Here again, assigning +1 to the selected pixels results in lower rms voltage to the selected pixels as compared to the background pixels. This technique is referred to as PRBS−NC.
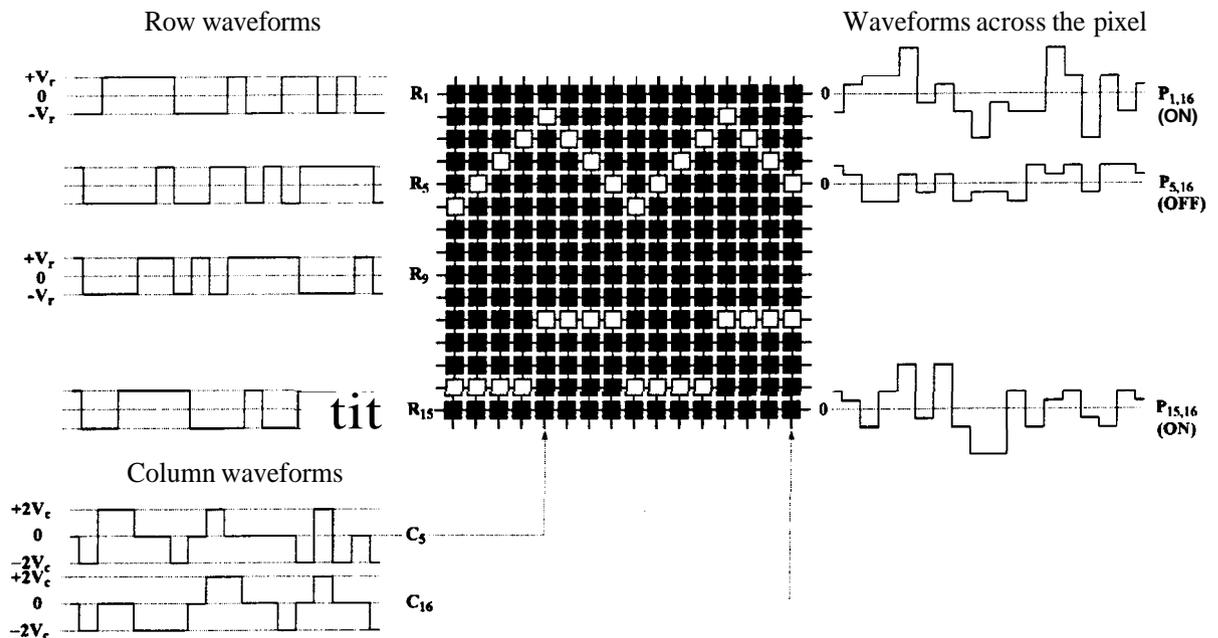

Figure 2-40 Typical addressing waveforms of PRBS−NC.

In a similar technique known as PRBS−PC, the selected pixels gets a higher rms voltage when the data assigned to the selected pixel is −1. A higher address duty factor in the PRBS techniques results in the suppression of flicker and frame response even for large values of N as in the case of active addressing [23] technique. Typical addressing waveforms of both PRBS−NC and PRBS−PC are as shown in the Figure 2-40 and Figure 2-41, respectively. Selection ratio is independent of the matrix size and is same as in the case of RPATs. Supply voltage for PRBS technique are independent of the matrix size and just depends on the number of waveforms to be displayed and it is lower than that of RPATs. Hence, large matrix displays with high resolution can be driven using these techniques. Here, number of voltage levels in the column waveform is equal to $(w+1)$. Hence, complexity of the column driver increases as compared to RPATs. In summary,

Selection ratios, supply voltage and the number voltage levels needed while displaying multiple waveforms for **RPATs** and **PRBSs** are tabulated in Table 2-6 for comparison.
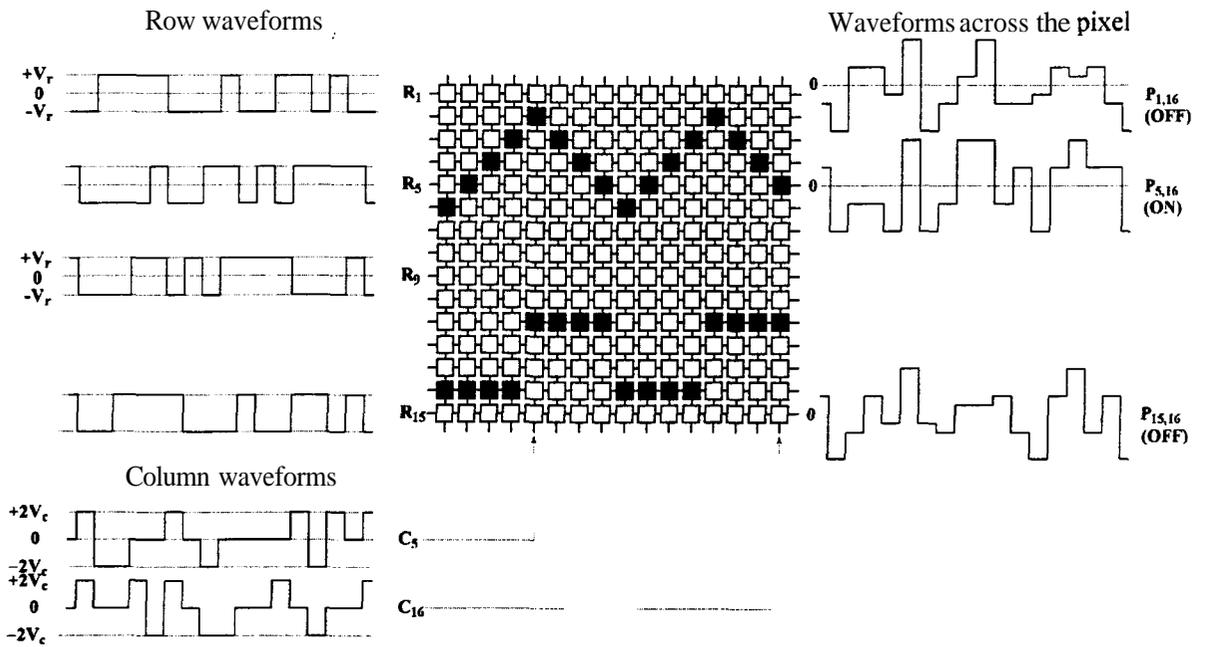
Row waveforms

Waveforms across the pixel

+V$_r$ 0 -V$_r$ R$_1$ P$_{1,16}$ (OFF)

R$_5$ P$_{5,16}$ (ON)

+V$_r$ 0 -V$_r$ R$_9$

R$_{15}$ P$_{15,16}$ (OFF)

Column waveforms

+2V$_c$ 0 -2V$_c$ +2V$_c$ 0 -2V$_c$ C$_5$ C$_{16}$

Figure 2-41 Typical addressing waveforms of PRBS-PC.

Table 2-6

Technique	Selection Ratio	Supply voltage	Number of voltage levels in the row waveforms	Number of voltage levels in the column waveforms
RPAT–PC (Modified)	$\sqrt{w}$	$\sqrt{\dfrac{N}{2w}}\left(\sqrt{w}+1\right) V_{th}$	**4**	**4**
RPAT–NC (Modified)	$\sqrt{\dfrac{\sqrt{w}}{\sqrt{w}-1}}$	$\sqrt{\dfrac{N}{2}}\ V_{sat}$	2	*4*
PRBS–PC	$\sqrt{\dfrac{\sqrt{w}+1}{\sqrt{w}}}$	$\sqrt{2w}\ V_{th}$	2	w + 1
PRBS–NC	$\sqrt{\dfrac{\sqrt{w}}{\sqrt{w}-1}}$	$\sqrt{2w}\ V_{sat}$	2	$w+1$