Chapter 3

3. Multi-Line Restricted Pattern Addressing Technique

Multi-Line Restricted Pattern Addressing Technique

3.1. Introduction

Liquid crystal displays are used in oscilloscope, ECGs and logic analyser to display waveforms, which are single valued functions of time. To display w waveforms only w pixels in each column carries the information. The rest of the pixels in each column are background pixels. Hence, the patterns while displaying waveforms are restricted as compared to the general patterns. To display waveforms with good resolution, matrix size should be large. As the matrix size increases, the selection ratio decreases. The two techniques to display multiple waveforms are restricted pattern addressing technique (RPAT)[36] and pseudo random binary sequence (PRBS) technique [37]. In both these techniques the selection ratio is independent of the matrix size and depends only on the number of waveforms to be displayed. Hence, it is possible to display multiple waveforms with good resolution in a large matrix LCD. Here, a technique for displaying multiple waveforms by scanning the display based on multi-line addressing is presented.

3.2. Technique

The N rows in a matrix are divided into N/s non-intersecting subgroups, each subgroups consisting of s rows. Only one subgroup is selected at a time while the rows in the unselected subgroups are grounded. The rows in the subgroup are selected with $+V_r$ or $-V_r$ corresponding to +1 or −1 in the row select pattern respectively. The row select patterns are derived from the orthogonal functions like Walsh, Hadamard or pseudo random binary sequence (PRBS). The generation of these orthogonal functions and their matrix representation are given in Appendix B. Let $O(i, j)$ be the element of the orthogonal matrix used to select the s rows in the selected subgroup. The value of i range from 1 to s and j ranges from 1 to q, wherein q is the number of columns in the orthogonal matrix. The columns of the orthogonal matrix are called row select patterns, and the jth row select pattern is represented as $O(1, j), O(2, j), O(3, j), \ldots\ldots\ldots, O(s, j)$. The data to be displayed in the selected subgroup is represented as data vector d_{ks+i} i.e., d_{ks+1}, d_{ks+2}, $d_{ks+3}, \ldots\ldots\ldots, d_{ks+s}$, where k ranges from 0 to $\left(\dfrac{N}{s} - 1\right)$ corresponding to

selected subgroup. Column voltage is the dot product of the row select pattern and the data vector. This is represented as

$$C_k(j) = \sum_{i=1}^{s} O(i, j) \cdot d_{ks+i}$$

(3. 1)

Where, $C_k(j)$ is the column voltage (normalized to V_c) for the jth row select pattern wherein $1 \le j \le q$. Similarly, the column voltage for all the columns in the matrix is determined independently. Both the row and column voltages are applied simultaneously to the matrix display for a time duration τ. The process is repeated with another row select pattern and the new row and column voltages are applied to the matrix display for the same duration τ. A cycle is complete when all the subgroups N/s are selected with all the row select pattern once. The display is refreshed continuously about 30–40Hz. Here, the display is scanned based on multi-line approach to display the restricted patterns. Hence, this technique is referred to as multi-line restricted pattern addressing technique.

The data of the pixels are assigned +1 or −1 corresponding to OFF and ON states respectively while displaying general patterns. Since the waveforms are single valued function of time, only w pixels in each column carry the information while displaying *w* waveforms. The rest of the $(N - w)$ pixels in each column are background pixels. The data for the background pixels are assigned to be zero. The data for the w pixels in each column can be assigned either +1 or −1. By assigning data as +1, these pixels get lower rms voltage as compared to the background pixels. In this case the waveforms appear bright against dark background. This is referred to as negative contrast (NC) mode, and the addressing technique is referred to as multi-line restricted pattern addressing technique−NC. Figure 3-1(a) shows two waveforms in negative contrast mode. Similarly, the data for w pixels in each column can be assigned −1. In this case these pixels will have higher rms voltage as compared to the background pixels. This results in positive contrast (PC) mode as shown in Figure 3-1(b) and the technique is called multi-line restricted pattern addressing technique−PC.
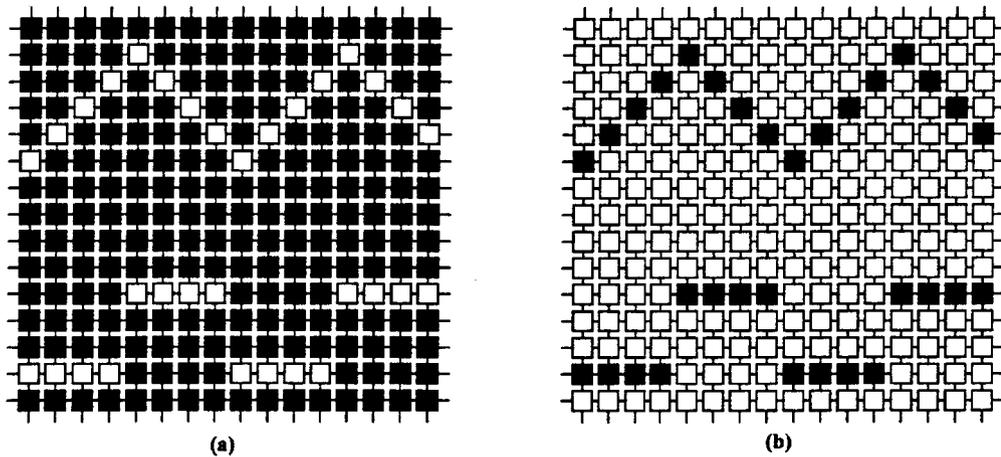
Figure 3-1 Passive matrix LCD displaying waveforms in two modes (a) negative contrast and (b) positive contrast.

In the multi-line restricted pattern addressing technique, number of voltage levels in the column waveforms depends on the number of waveforms present in the selected subgroups. Usually, the w pixels are distributed in different subgroups. In the worst case, all the w pixels may be present in one of the selected subgroup provided $s \geq w$. The w pixels may be distributed in other subgroups and all the pixels in the selected subgroup may be background pixels. The number of information carrying pixels in the selected subgroup varies from [0,1,2,....,w]. Hence, all the possible voltages **i.e.,** $0, \pm V_c, \pm 2V_c, ...\pm (w-1)V_c$ and $\pm wV_c$ are necessary. Thus the number of voltage levels in the column waveforms increases and it necessary to have (2w+1) voltage levels to display w waveforms. If the number of rows in each subgroup is less than the number of waveforms to be displayed **i.e.,** (s < w), then (2s+1) voltage levels are necessary in the column driver. The number of voltage levels in this case is less than (2w+1). Hence, the number of voltage levels in the column waveform is limited to (2s+1) when s rows are selected simultaneously to display w waveforms.

In applications like logic analyzer and **ECGs** the waveforms do not overlap with each other and are equally spaced. In this case the w pixels (**i.e.,** points on the waveforms) may be distributed in the subgroups by choosing a proper size for the subgroup. The number of voltage levels in the column waveforms can be reduced considerably by distributing the waveforms into different subgroups. The scanning of the matrix can be done in many ways. A subgroup may be selected with all the row select patterns once before selecting

another subgroup. This is illustrated in Figure 3-2 and the corresponding row select patterns are represented in the matrix form in Figure 3-3.
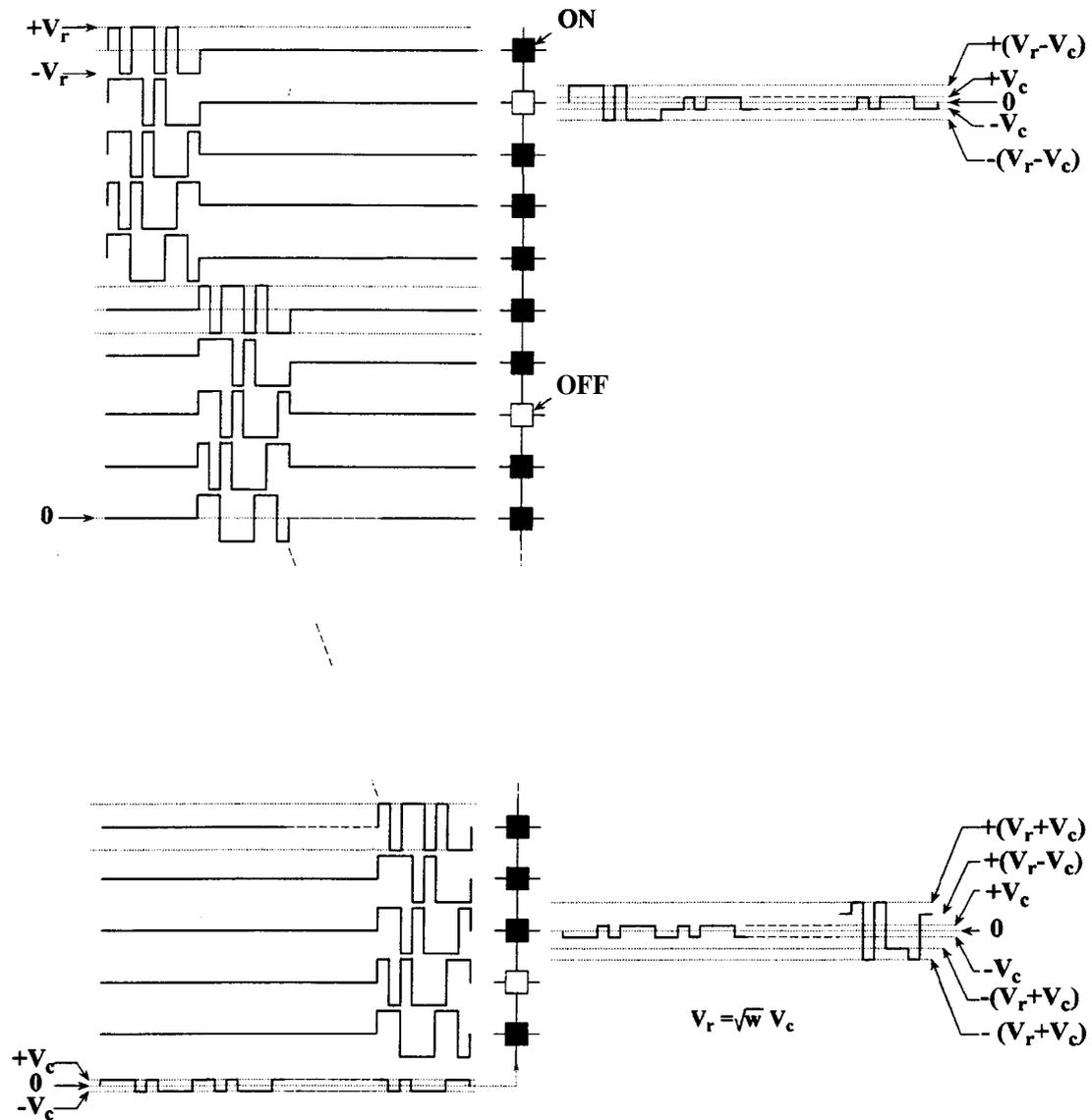
Figure 3-2 Typical addressing waveforms of multi-line restricted pattern addressing technique by selecting five rows at a time.

However, this method is not suitable for fast responding LCDs. Since the light transmission through OFF pixel increases due to clustering of the usually large amplitude row select pulses. This may lead to the frame response phenomena [15] (see section 2.4.6). In order to suppress the frame response in multiple line addressing technique, all the subgroups in the matrix LCD may be selected with one row select pattern once before changing to another row select pattern as shown in matrix of Figure 3-4. Good brightness uniformity of the pixel can be obtained by changing the row select pattern whenever a new subgroup is selected as shown in Figure 3-5.

```
⎡+1  -1  +1  +1  -1  +1  -1  -1   0   0   0   0   0   0   0   0   0   0   0   0   0   0   0   0⎤
⎢+1  +1  +1  -1  +1  -1  -1  -1   0   0   0   0   0   0   0   0   0   0   0   0   0   0   0   0⎥
⎢+1  +1  -1  +1  -1  -1  -1  +1   0   0.  0   0   0   0   0   0   0   0   0   0   0   0   0   0⎥
⎢+1  -1  +1  -1  -1  -1  +1  +1   0   0   0   0   0   0   0   0   0   0   0   0   0   0   0   0⎥
⎢+1  +1  -1  -1  -1  +1  +1  -1   0   0   0   0   0   0   0   0   0   0   0   0   0   0   0   0⎥
⎢ 0   0   0   0   0   0   0   0  +1  -1  +1  +1  -1  +1  -1  -1   0   0   0   0   0   0   0   0⎥
⎢ 0   0   0   0   0   0   0   0  +1  +1  +1  -1  +1  -1  -1  -1   0   0   0   0   0   0   0   0⎥
⎢ 0   0   0   0   0   0   0   0  +1  +1  -1  +1  -1  -1  -1  +1   0   0   0   0   0   0   0   0⎥
⎢ 0   0   0   0   0   0   0   0  +1  -1  +1  -1  -1  -1  +1  +1   0   0   0   0   0   0   0   0⎥
⎢ 0   0   0   0   0   0   0   0  +1  +1  -1  -1  -1  +1  +1  -1   0   0   0   0   0   0   0   0⎥
⎢ 0   0   0   0   0   0   0   0   0   0   0   0   0   0   0   0  +1  -1  +1  +1  -1  +1  -1  -1⎥
⎢ 0   0   0   0   0   0   0   0   0   0   0   0   0   0   0   0  +1  +1  +1  -1  +1  -1  -1  -1⎥
⎢ 0   0   0   0   0   0   0   0   0   0   0   0   0   0   0   0  +1  +1  -1  +1  -1  -1  -1  +1⎥
⎢ 0   0   0   0   0   0   0   0   0   0   0   0   0   0   0   0  +1  -1  +1  -1  -1  -1  +1  +1⎥
⎣ 0   0   0   0   0   0   0   0   0   0   0   0   0   0   0   0  +1  +1  -1  -1  -1  +1  +1  -1⎦
```

Figure 3-3 Row select matrix when row select pulses adjacent to each other for N = 15, s = 5.

```
⎡+1   0   0  -1   0   0  +1   0   0  +1   0   0  -1   0   0  +1   0   0  -1   0   0  -1   0   0⎤
⎢+1   0   0  +1   0   0  +1   0   0  -1   0   0  +1   0   0  -1   0   0  -1   0   0  -1   0   0⎥
⎢+1   0   0  +1   0   0  -1   0   0  +1   0   0  -1   0   0  -1   0   0  -1   0   0  +1   0   0⎥
⎢+1   0   0  -1   0   0  +1   0   0  -1   0   0  -1   0   0  -1   0   0  +1   0   0  +1   0   0⎥
⎢+1   0   0  +1   0   0  -1   0   0  -1   0   0  -1   0   0  +1   0   0  +1   0   0  -1   0   0⎥
⎢ 0  +1   0   0  -1   0   0  +1   0   0  +1   0   0  -1   0   0  +1   0   0  -1   0   0  -1   0⎥
⎢ 0  +1   0   0  +1   0   0  +1   0   0  -1   0   0  +1   0   0  -1   0   0  -1   0   0  -1   0⎥
⎢ 0  +1   0   0  +1   0   0  -1   0   0  +1   0   0  -1   0   0  -1   0   0  -1   0   0  +1   0⎥
⎢ 0  +1   0   0  -1   0   0  +1   0   0  -1   0   0  -1   0   0  -1   0   0  +1   0   0  +1   0⎥
⎢ 0  +1   0   0  +1   0   0  -1   0   0  -1   0   0  -1   0   0  +1   0   0  +1   0   0  -1   0⎥
⎢ 0   0  +1   0   0  -1   0   0  +1   0   0  +1   0   0  -1   0   0  +1   0   0  -1   0   0  -1⎥
⎢ 0   0  +1   0   0  +1   0   0  +1   0   0  -1   0   0  +1   0   0  -1   0   0  -1   0   0  -1⎥
⎢ 0   0  +1   0   0  +1   0   0  -1   0   0  +1   0   0  -1   0   0  -1   0   0  -1   0   0  +1⎥
⎢ 0   0  +1   0   0  -1   0   0  +1   0   0  -1   0   0  -1   0   0  -1   0   0  +1   0   0  +1⎥
⎣ 0   0  +1   0   0  +1   0   0  -1   0   0  -1   0   0  -1   0   0  +1   0   0  +1   0   0  -1⎦
```

Figure 3-4 Row select matrix when row select pulses are distributed in a cycle for N = 15, s = 5

```
⎡■■   ■   0  +1   0   0  -1   0   0  -1   0   0  -1   0   0  -1   0   0  +1   0   0  +1   0   0⎤
⎢■■   ■   0  -1   0   0  -1   0   0  +1   0   0  +1   0   0  -1   0   0  +1   0   0  -1   0   0⎥
⎢+1   0   0  +1   0   0  -1   0   0  +1   0   0  -1   0   0  +1   0   0  -1   0   0  -1   0   0⎥
⎢+1   0   0  -1   0   0  +1   0   0  -1   0   0  -1   0   0  +1   0   0  +1   0   0  -1   0   0⎥
⎢+1   0   0  -1   0   0  +1   0   0  +1   0   0  -1   0   0  -1   0   0  -1   0   0  +1   0   0⎥
⎢ 0  -1   0   0  -1   0   0  -1   0   0  +1   0   0  +1   0   0  +1   0   0  +1   0   0  -1   0⎥
⎢ 0  +1   0   0  +1   0   0  -1   0   0  +1   0   0  -1   0   0  +1   0   0  -1   0   0  -1   0⎥
⎢ 0  +1   0   0  -1   0   0  +1   0   0  -1   0   0  -1   0   0  +1   0   0  +1   0   0  -1   0⎥
⎢ 0  -1   0   0  -1   0   0  +1   0   0  +1   0   0  -1   0   0  +1   0   0  -1   0   0  +1   0⎥
⎢ 0  +1   0   0  -1   0   0  -1   0   0  -1   0   0  +1   0   0  +1   0   0  -1   0   0  +1   0⎥
⎢ 0   0  +1   0   0  +1   0   0  +1   0   0  +1   0   0  -1   0   0  -1   0   0  -1   0   0  -1⎥
⎢ 0   0  +1   0   0  -1   0   0  +1   0   0  -1   0   0  -1   0   0  +1   0   0  +1   0   0  -1⎥
⎢ 0   0  -1   0   0  -1   0   0  +1   0   0  +1   0   0  -1   0   0  +1   0   0  -1   0   0  +1⎥
⎢ 0   0  +1   0   0  -1   0   0  +1   0   0  -1   0   0  +1   0   0  -1   0   0  -1   0   0  +1⎥
⎣ 0   0  -1   0   0  +1   0   0  +1   0   0  -1   0   0  +1   0   0  +1   0   0  -1   0   0  -1⎦
```

Figure 3-5 Row select matrix when row select pulses are distributed in a cycle by selecting a subgroup with different row select pattern for N = 15, s = 5.

3.3. *Analysis*

A subgroup is selected at a time with voltages corresponding to a row select pattern. The voltages are $+V_r$ or $-V_r$ corresponding to -1 or $+1$ of the row select patterns, respectively. The row voltage is zero during the $\left(\dfrac{N}{s}-1\right)q$ time intervals when other rows are being selected. Where q is the total number of columns in the orthogonal matrix. The column voltage $C_k(j)$ (normalized to V_c), which is the dot product of the row select pattern and the data vector in the kth subgroup is given by,

$$C_k(j) = \sum_{i=1}^{s} O(i,j)d_{ks+i} \tag{3.2}$$

Where j ranges from 1 to q and k ranges from 0 to $\left(\dfrac{N}{s}-1\right)$. The voltage across any pixel is the difference between row and column voltages. The rms voltage across the ith pixel $[1 \le i \le s]$ in the kth subgroup $\left[0 \le k \le \left(\dfrac{N}{s}-1\right)\right]$ is given by

$$V_{ks+i}(rms) = \sqrt{\dfrac{\displaystyle\sum_{j=1}^{q}[O(i,j)V_r - C_k(j)V_c]^2 + \displaystyle\sum_{\substack{n=0 \\ n\neq k}}^{(\frac{N}{s}-1)}\sum_{j=1}^{q}[C_n(j)V_c]^2}{\dfrac{N}{s}\,q}} \tag{3.3}$$

$$V_{ks+i}(rms) = \sqrt{\dfrac{\displaystyle\sum_{j=1}^{q}\left[\left(O(i,j)V_r\right)^2 - 2\,O(i,j)V_rC_k(j)V_c\right] + \displaystyle\sum_{n=0}^{(N/s-1)}\sum_{j=1}^{q}[C_n(j)V_c]^2}{\dfrac{N}{s}\,q}}$$

Substituting the column voltage from equation **3.2** in the above expression, then

$$V_{ks+i}(rms) = \sqrt{\dfrac{V_r^2\displaystyle\sum_{j=1}^{q}[O(i,j)]^2 - 2V_rV_cd_{ks+i}\displaystyle\sum_{j=1}^{q}[O(i,j)]^2 + V_c^2\displaystyle\sum_{n=0}^{(N/s-1)}\sum_{i=1}^{s}[d_{ns+i}]^2\displaystyle\sum_{j=1}^{q}[O(i,j)]^2}{\dfrac{N}{s}\,q}}$$

From orthogonal condition, after simplification we get,

$$V_{ks+i}(rms) = \sqrt{\frac{V_r^2 q - 2V_r V_c d_{ks+i} q + V_c^2 q \sum\limits_{n=0}^{(N/s-1)} \sum\limits_{i=1}^{s} [d_{ns+i}]^2}{\dfrac{N}{s} q}} \qquad (3.4)$$

This is the general expression for the multi-line addressing technique. In order to display w waveforms in the matrix LCD, only w pixels in each column carry the information, and (N − w) pixels in each column are the background pixels. Data for the w information carrying pixels are assigned to be +1, while the remaining (N − w) background pixels are assigned to be 0. This results in negative contrast (**NC**) mode. If the $V_{ks+i}(rms)$ in equation (3.4) corresponds to a point on a waveform, then rms voltage across that **OFF** pixel (i.e., $d_{ks+i} = +1$) is given by

$$V_{off}(rms) = \sqrt{\frac{V_r^2 q - 2V_r V_c q + wV_c^2 q}{\left(\dfrac{N}{s}\right) q}}$$

$$V_{off}(rms) = \sqrt{\frac{V_r^2 - 2V_r V_c + wV_c^2}{\left(\dfrac{N}{s}\right)}} \qquad (3.5)$$

Similarly if the $V_{ks+i}(rms)$ corresponds to background pixel (i.e., $d_{ks+i} = 0$), then from equation (3.4), the rms voltage across the background pixel (i.e, **ON**) is

$$V_{on}(rms) = \sqrt{\frac{V_r^2 q + wV_c^2 q}{\left(\dfrac{N}{s}\right) q}}$$

$$V_{on}(rms) = \sqrt{\frac{V_r^2 + wV_c^2}{\left(\dfrac{N}{s}\right)}} \qquad (3.6)$$

The selection ratio defined as $\left(\dfrac{V_{on}}{V_{off}}\right)$ is maximum when $V_r = \sqrt{w}\ V_c$.

Thus the optimum selection ratio for multi-line restricted pattern addressing technique–NC mode is given by

$$SR = \sqrt{\frac{\sqrt{w}}{\sqrt{w}-1}}$$

(3.7)

This selection ratio is the same as that of **RPAT–NC[36]** and **PRBS–NC[37]**. Similarly by assigning data for the w pixels that are points on the waveform to be –1 for the positive contrast mode. Selection ratio for multi-line restricted pattern addressing technique–PC is given by

$$SR = \sqrt{\frac{\sqrt{w}+1}{\sqrt{w}}}$$

(3.8)

This is the same as that obtained for **RPAT–PC[36]** and **PRBS–PC[37]** techniques. Thus the selection ratios for restricted pattern addressing techniques are independent of the matrix size. The selection ratio is higher in the case of negative contrast as compared to positive contrast as shown in the Figure 3-6. In the same figure the selection ratio for a 64 row matrix while displaying general pattern is shown for a comparison.
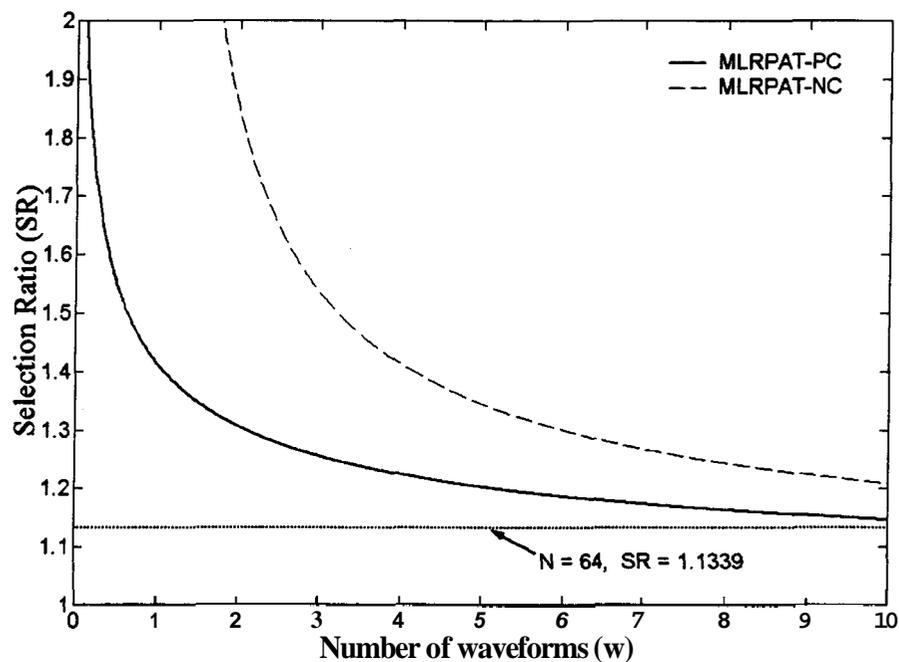
Figure 3-6 Comparison graph of selection ratios of multi-line restricted pattern addressing technique-Positive Contrast (MLRPAT-PC), multi-line restricted pattern addressing technique-Negative Contrast (MLRPAT-NC) with general pattern with N=64.

Supply Voltage Requirement of MLRPA–NC

The supply voltage (V_{sup}) for the driver is calculated by the maximum swing in the addressing waveforms that is

a) Case I

If ($s \leq \sqrt{w}$) then $\left(2\ V_r > 2\ s\ V_c\right)$, where $2V_r$ is the maximum swing in the row waveform and $2sV_c$ is the maximum swing in the column waveform, then the supply voltage is given by

$$V_{sup} = 2V_r$$

$$V_{sup} = 2\sqrt{w}\ V_c$$

Where $V_c = \sqrt{\dfrac{N}{2ws}}\ V_{sat}$ 　　　　　　　　　　　　　(3.9)

i.e., $V_{sup} = \sqrt{\dfrac{2N}{s}}\ V_{sat}$ 　　　　　　　　　　　　　(3.10)

b) Case II

If $\left(\sqrt{w} < s < w\right)$ then the maximum swing in the addressing waveform is $2sV_c$, thus the supply voltage is

$$V_{sup} = 2sV_c$$

$$V_{sup} = \sqrt{\dfrac{2Ns}{w}}\ V_{sat}$$ 　　　　　　　　　　　　　(3.11)

c) Case III

If ($s \geq w$) then the maximum swing in the addressing waveform is $2wV_c$, the supply voltage is given by

$$V_{sup} = 2wV_c$$

$$V_{sup} = \sqrt{\dfrac{2wN}{s}}\ V_{sat}$$ 　　　　　　　　　　　　　(3.12)

Figure 3-7 shows the comparison graph of supply voltage requirement for displaying restricted patterns for various values of N and w by selecting 8 rows at time.
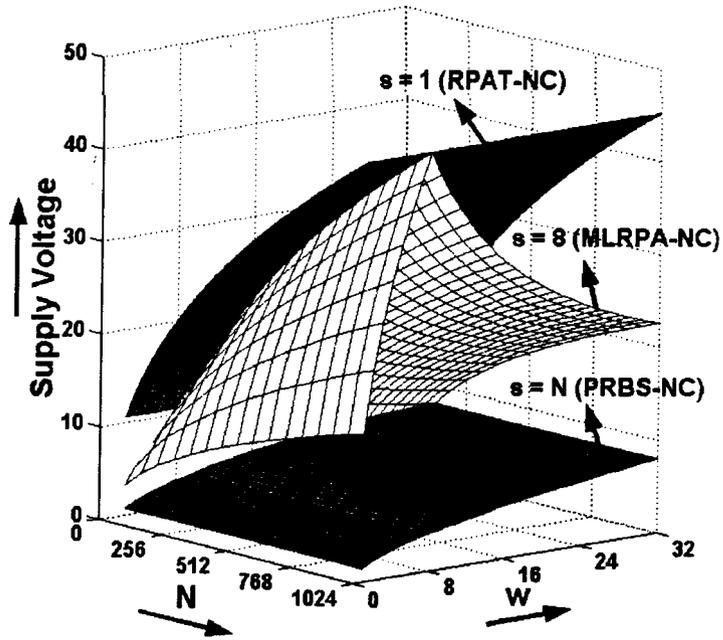
Figure 3-7 Supply voltage of the restricted pattern addressing techniques.

(a)

(b)

(c)

(d)
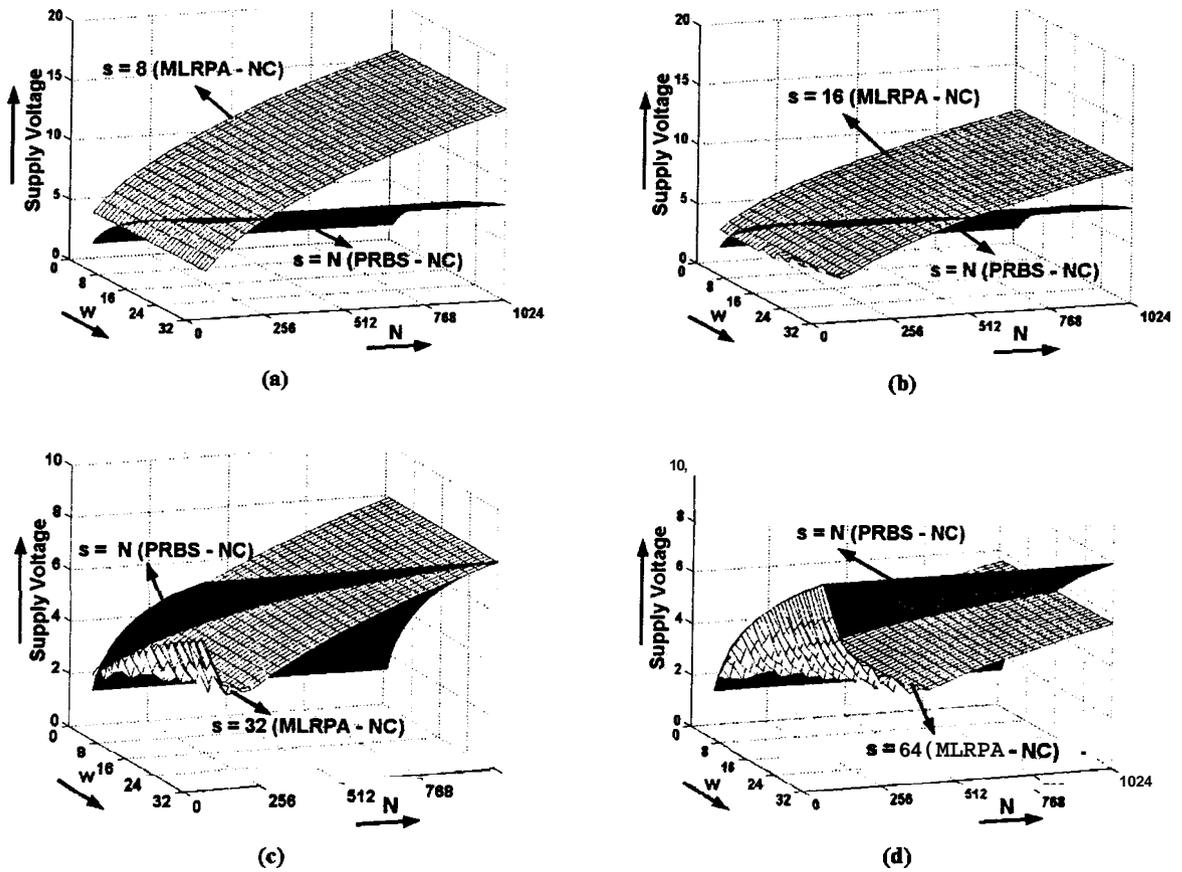
Figure 3-8 Comparison of Supply voltage requirement (normalised to V_{sat}) for displaying restricted pattern using MLRPA technique when (a) $s = 8$ (b) $s = 16$ (c) $s = 32$ and (d) s = 64 with that of PRBS.

Waveforms displayed in Logic analyzer and electrocardiograph (ECG) are non overlapping. In these applications the waveforms do not intersect and are equally spaced. In this case, the supply voltage and also the number of voltage levels in the column waveforms can be reduced. For example, Figure 3-8 shows the supply voltage requirement (normalised to V_{sat}) of multi-line restricted pattern addressing technique–NC in comparison with PRBS-NC for various values of s. The conditions for driving the matrix LCD with lower supply voltage and also with less number of voltage levels in the column waveforms are obtained by selecting appropriate subgroup size as discussed in the following paragraph.

Condition for a minimum supply voltage

The minimum supply voltage is achieved when the maximum swings in the row and column waveforms are equal. The maximum voltage swing in the row waveforms is $2\sqrt{w}\ V_c$. The maximum voltage swing in the column waveforms depends on the number of waveform present in the selected subgroups. If $w = \left(\dfrac{N}{s}\right)^2$, then maximum swings in the row and column waveforms are equal. That is $\left(\dfrac{N}{s}\right) = \sqrt{w}$, wherein $\sqrt{w}$ is not an integer in general for all the values of w. Thus, the minimum supply voltage can be obtained when the number of subgroups $(S) = Int\left|\sqrt{w}\right|$. In this case the minimum supply voltage (V_{sup}) is given by

$$V_{sup} = 2x\ V_c. \qquad \text{Where, } x = Znt\left|\sqrt{w}\right|$$

From equation (3.9) $V_c = \sqrt{\dfrac{N}{2ws}}\ V_{sat}$

$$\text{i.e., } V_{sup} = 2x\sqrt{\dfrac{x}{2w}}\ V_{sat} \qquad\qquad (3.13)$$

The supply voltage (V_{sup}) in this case is a minimum and also it is independent of the matrix size. The number of voltage levels in the column waveforms are equal to $(x+1)$. Which is very much less than that of the PRBS technique.

II. *Condition for minimum number of voltage levels in the column waveform*

The number of subgroups can be made equal to the number of waveforms to be displayed, i.e., $\dfrac{N}{s}$ = w. Then there will be only one waveforms in each subgroup. This results in just two voltage levels in the column waveforms. Supply voltage $\left(V_{sup}\right)$ in this case is given by,

$$V_{sup} = 2V_r = 2\sqrt{w}\sqrt{\frac{N}{2ws}}\ V_{sat}$$

$$V_{sup} = \sqrt{2w}\ V_{sat} \qquad\qquad\qquad (3.14)$$

The supply voltage here again is independent of matrix size, and is the same as that of PRBS technique. But number of voltage levels in the column waveforms is just two as compared to (w + 1) in PRBS technique.

For example consider a 64x64 matrix LCD to display 4 waveforms. Figure 3-9 shows the number of voltage levels in the column waveforms for displaying four waveforms for four different subgroup sizes (s). The number of voltage levels in the column waveforms is minimum when 16 rows are selected at a time. In this case only one waveform will be present in each subgroup and just two voltage levels are adequate in the column waveforms. When $s = 32$ (i.e, $\left(\dfrac{N}{s}\right)^2$ = w), two waveforms will be present in each subgroups. Then maximum voltage swing in the column waveforms is $2\sqrt{w}\ V_c$, which is same as that of maximum voltage swing in the row waveform (i.e., $2V_r$). The supply voltage is minimum in this case and the number of voltage levels in the column waveforms is three i.e., $\left(\dfrac{N}{s} + 1\right)$. Table 3-1(a) and (b) summarizes the number of voltage levels in the column waveform as well as the supply voltage requirement of Multi-Line Restricted Pattern Addressing – Negative Contrast (MLRPA–NC) in comparison with that of RPAT–NC and PRBS–NC techniques for the case of non overlapping waveforms. Table 3-2 gives the value of *s* leading to a good reduction in the supply voltage as well as the number of voltage levels in the column waveform for various values of N and w as compared with PRBS–NC technique. Hence, by using multi-line restricted pattern

addressing technique good reduction in number of voltage levels in the column waveform and also the supply voltage is possible. The reduction in the number of voltage levels has a significant impact on the hardware complexity of the column driver. To demonstrate this technique a controller has been designed to display four waveforms. Here, both overlapping and non-overlapping waveforms are considered. The design and implementation of a controller to display multiple waveforms are discussed in the next section.
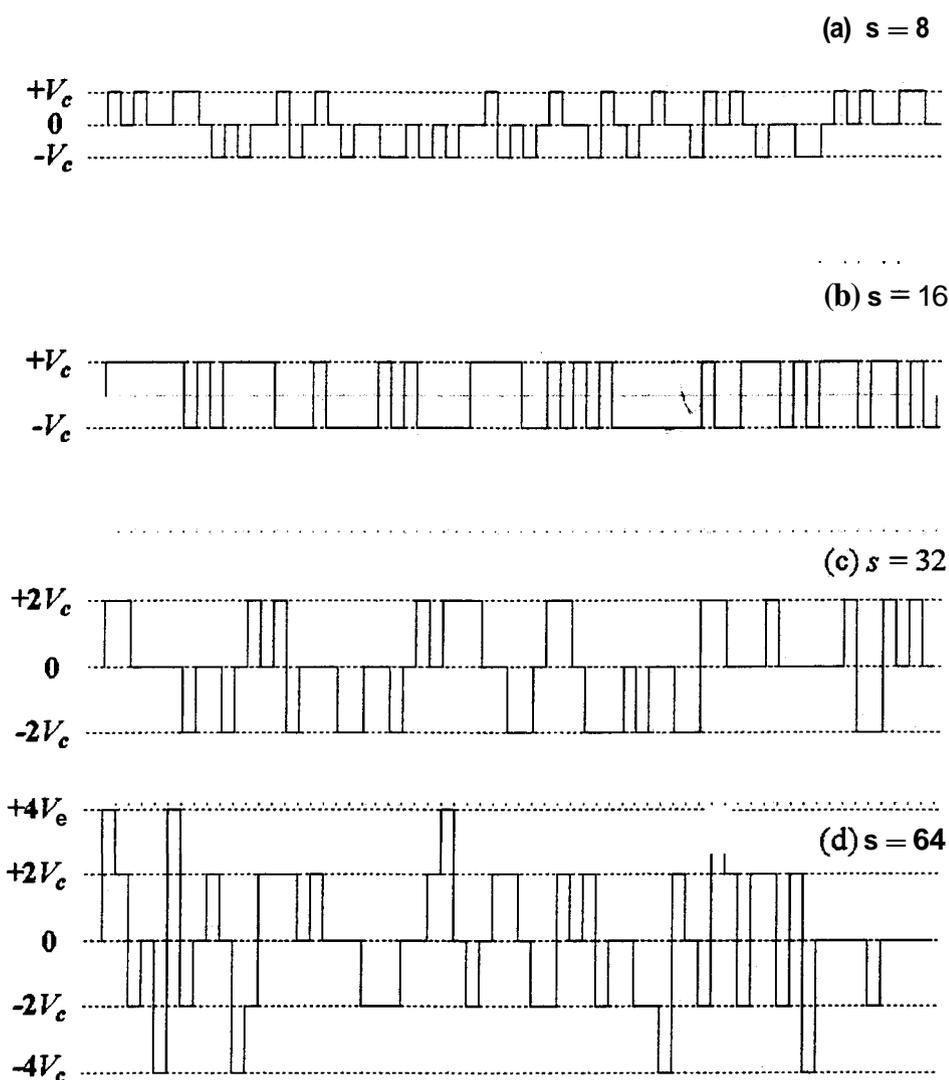
Figure 3-9 Typical column waveforms of a 64x64 matrix LCD, while scanning the display by selecting (a) s = 8,(b) s=16, (c) s =32, and (d) s =64 to display four non-overlapping waveforms.

Table 3-1(a)

N	w	s	MLRPA-NC Technique		PRBS-NC Technique		RPAT-NC
			No. of voltage levels in the column waveform	Supply voltage (normalised to V_{sat})	No. of voltage levels in the column waveform	Supply voltage (normalised to V_{sat})	No. of voltage Levels = 4
							Supply voltage (normalised to V_{sat})
64	4	8	3	4.0000	5	2.8284	5.6569
		16	2	2.8284			
		32	3	2.0000			
128	4	8	3	5.6569	5	2.8284	8.0000
		16	3	4.0000			
		32	2	2.8284			
		64	3	2.0000			
	8	8	3	5.6569	9	4.0000	
		16	2	4.0000			
		32	3	2.8284			
		64	5	2.8284			
256	4	8	3	8.0000	5	2.8284	11.3137
		16	3	5.6569			
		32	3	4.0000			
		64	2	2.8284			
		128	3	2.0000			
	8	8	3	8.0000	9	4.0000	
		16	3	5.6569			
		32	2	4.0000			
		64	3	2.8284			
		128	5	2.8284			
	16	8	3	8.0000	17	5.6569	
		16	2	5.6569			
		32	3	4.0000			
		64	5	2.8284			
		128	9	4.0000			

Table 3-1(b)

| N | w | s | MLRPA-NC Technique | | PRBS-NC Technique | | RPAT-NC |
| | | | No. of voltage levels in the column waveform | Supply voltage (normalised to V_{sat}) | No. of voltage levels in the column waveform | Supply voltage (normalised to V_{sat}) | No. of voltage Levels = 4 |
							Supply voltage (normalised to V_{sat})
512	4	8	3	11.3137	5	2.8284	16.0000
		16	3	8.0000			
		32	3	5.6569			
		64	3	4.0000			
		128	2	2.8284			
		256	3	2.0000			
	8	8	3	11.3137	9	4.0000	
		16	3	8.0000			
		32	3	5.6569			
		64	2	4.0000			
		128	3	2.8284			
		256	5	2.8284			
	16	8	3	11.3137	17	5.6569	
		16	3	8.0000			
		32	2	5.6569			
		64	3	4.0000			
		128	5	2.8284			
		256	9	4.0000			
	32	8	3	11.3137	33	8.0000	
		16	2	8.0000			
		32	3	5.6569			
		64	5	4.0000			
		128	9	4.0000			
		256	17	5.6569			

Table 3-2

N	W	s	$\dfrac{V_{sup}(MLRPA - NC)}{V_{sup}(PRBS - NC)} \times 100$	No. of voltage level required $\dfrac{MLRPAT - NC}{PRBS - NC}$
64	4	32	70.71	$3/5$
128	4	64	70.71	$3/5$
	8	32	70.71	$3/9$
		64	70.71	$5/9$
256	4	128	70.71	$3/5$
	8	64	_70.71	X
		128	70.71	X
	16	32	70.71	$3/17$
		64	50.00	$5/17$
		128	70.71	$9/17$
512	4	256	70.71	$3/5$
	8	128	70.71	$3/9$
		256	70.71	$5/9$
	16	64	70.71	$3/17$
		128	50.00	$5/17$
		256	70.71	$9/17$
	32	32	70.71	$3/33$
		64	50.00	$5/33$
		128	50.00	$9/33$
		256	70.71	$17/33$

3.4. Design and implementation

The design of a LCD controller for displaying multiple waveforms based on multi-line addressing technique is implemented using Complex Programmable Logic Device (CPLD). CPLDs are available with different architectures, from different vendors. The controller has been implemented using Altera's device EPM7128ELC-20. The various blocks required for the implementation of the multi-line restricted pattern addressing technique are shown in the Figure 3-10.
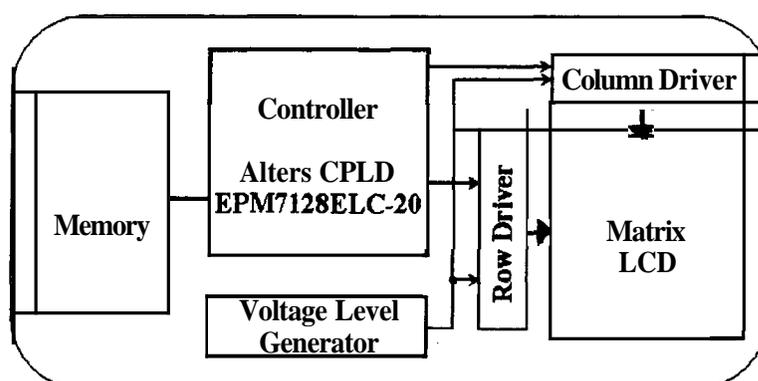
Figure 3-10 Simple block diagram of the display system.

A detailed block diagram of the display system to display multiple waveforms based on multi-line addressing is as shown in Figure 3-11. Here, data for the waveform to be displayed is stored in the waveform memory. The address to read data from waveform memory is generated from the control unit. Column signal generator generates the column data for each column from the row select pattern and the data from the waveform memory. Subgroup sequencer generates the sequence in which subgroups are selected. Voltage level generator generates the voltage levels for the row and column drivers. The control logic generates all the timing signals and synchronizes the flow of data in some of these blocks. In order to demonstrate the technique design of the controller is restricted to display 4 waveforms with both overlapping and non-overlapping types. Two different controllers have been designed one for selecting 8 rows at a time and another with 16 rows at a time. This is to show the reduction in the hardware complexity of the column driver for displaying four non-overlapping waveforms in a **64x64** matrix LCD by selecting 16 rows at a time. The different row select pattern for example one derived from Walsh functions, Hadamard matrix and PRBS are stored in the row select pattern memory to study the brightness uniformity of the multi-line restricted pattern addressing technique.

The row select pattern is generated internally in CPLD from the Rademacher function while selecting 16 rows at a time.. All the blocks except the waveform memory, voltage level generator, column driver and row driver shown in the Figure 3-11 have been integrated into a single chip (see Figure 3-10). The design and implementation of various blocks are discussed in detail in the next following sections.
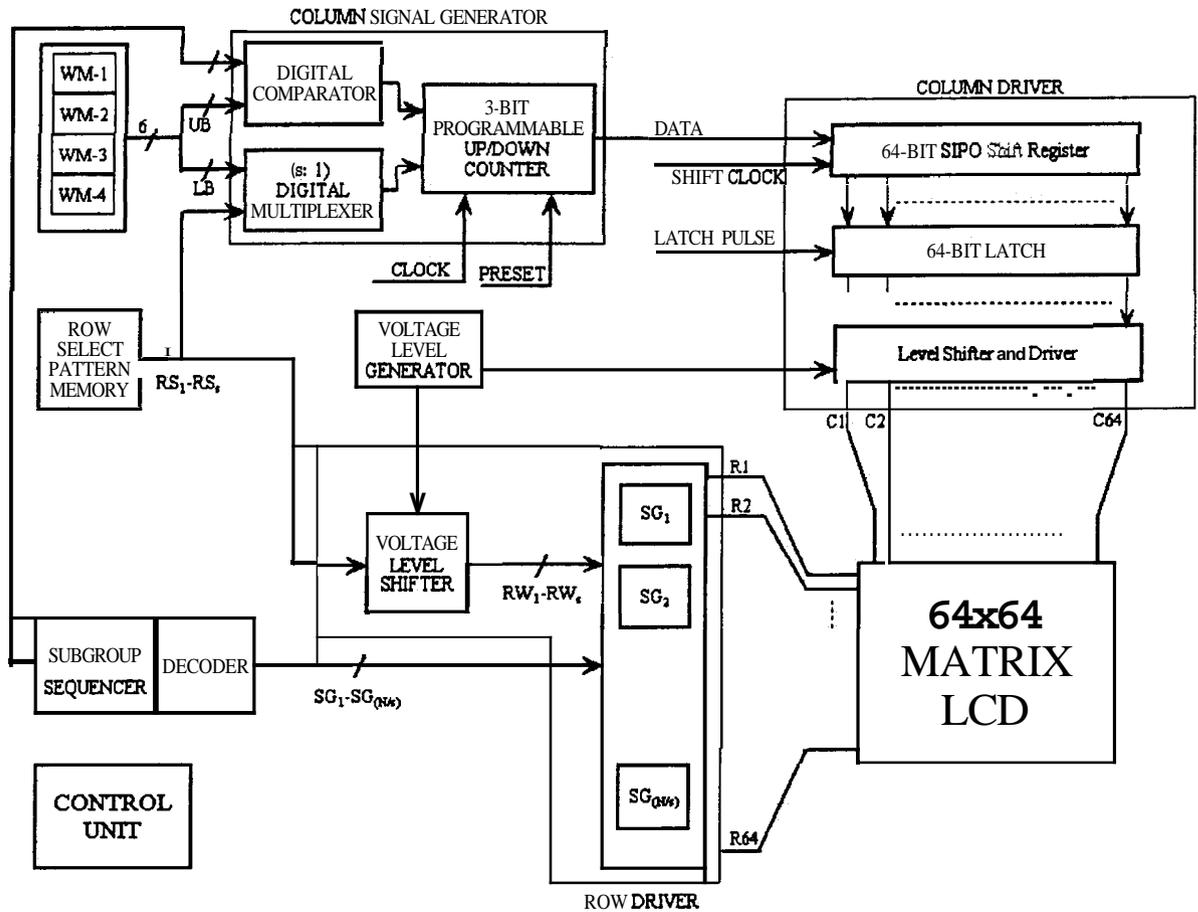
Figure 3-11 Detailed block diagram of a display using the multi-line restricted pattern addressing technique.

3.4.1. Row Select Pattern Generator

The row select pattern generator generates the s-bit row select patterns for selecting a subgroup. Row select patterns can be generated using flip-flops and logic gates or lookup table (LUT) method. Both the methods are demonstrated in two different controllers to display four waveforms using multi-line restricted pattern addressing technique. Lookup table method is used to generate row select pattern while selecting 8 rows at a time. Row select pattern is generated onboard while selecting 16 rows at a time. In the lookup table method all the row select patterns are stored in the memory. Here, different orthogonal

functions derived from Hadamard matrices, Walsh functions and Pseudo random binary sequence are used to select the subgroups. The generation of these orthogonal matrices and its matrix representation are given in Appendix B. The elements of these matrices take just +1 or –1 and they can be stored in the memory as 0 and 1 instead of +1 and –1, respectively. Any one of these orthogonal matrices is selected as row select pattern by using appropriate address to the memory. The starting locations in which these orthogonal matrices are stored are selected using the dipswitch provided onboard.

The Walsh functions are used as row select patterns while scanning the display by selecting 16 rows at a time. The Walsh functions are generated using a set of Rademacher functions. Rademacher functions are easy to generate, that is p functions can be generated using p flip-flops in a binary counter. For example, Walsh functions are generated by using EX-OR operation with Rademacher functions as shown in Figure 3-13. This method is called Harmuth's array generator [74]. There are other methods like Besslich array generator and unit-pulse Walsh function generator [74]. But, Harmuth's array generator is simple as compared to other methods. The hardware complexity in this technique is low. It requires less number of flip-flops and fewer logic gates. The generation of Walsh functions from the Rademacher function is as follows. To generate i^{th} Walsh function, where $1 \leq i \leq 2^p$, represent i in its binary number as

$i = b_{p-1}2^{p-1} + b_{p-2}2^{p-2},........+ b_1 2^1 + b_0 2^0$, where $b_j = 0$ or 1. Its binary code is written as $\left(b_{p-1}b_{p-2}....b_1 b_0\right)$. The equivalent gray code for this is represented as $\left(g_{p-1}g_{p-2}.....g_1 g_0\right)$, again $g_j = 0$ or 1. Then the Walsh function WAL(i,t) is given by

$$WAL(i,t) = \sum_{j=0}^{p-1} g_j RAD(j,t) \tag{3.15}$$

Here, the Rademacher function is represented as 0 and 1 instead of +1 and –1, respectively. The summations for the Rademacher functions are expressed as modulo 2 additions and can be obtained using Ex-OR gate operation. For example four Rademacher functions Rad(1,t), Rad(2,t), Rad(3,t) and Rad(4,t) are generated using a 4-bit counter as shown in the Figure 3-12.
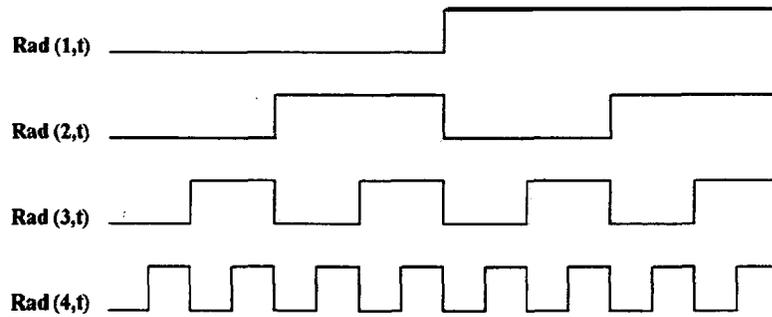
Figure 3-12 Typical waveforms of the Rademacher function generated form a four bit binary counter.

To generate a Walsh function WAL(12,t), first express 12 in binary code as 1100 and its gray equivalent is 1010. The first and the third bits are zero, the WAL(12,t) is expressed as

$$WAL(12,t) = RAD(4,t) \oplus RAD(2,t).$$
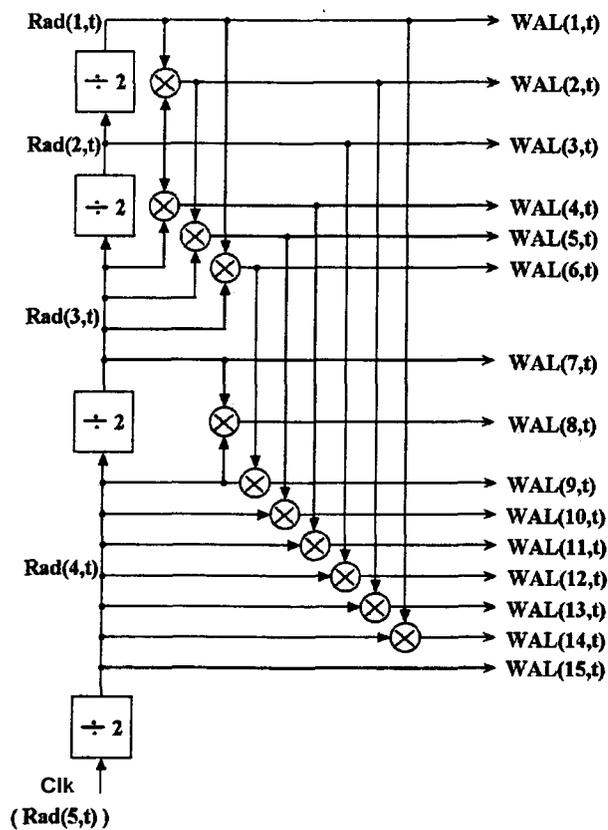
Figure 3-13 Typical schematic diagram of the Walsh function generator using Rademacher functions.

In the Figure 3-13 only 15 Walsh functions WAL(1,t) to WAL(15,t) are shown. The WAL(0,t) is a dc term and it is always one. After 16 clock pulses the entire cycle repeats. The logical values of the functions generated are 1 and 0, corresponding to the −1 and +1

of the Walsh functions. The resultant Walsh functions generated by the circuit in Figure 3-13 are shown in Figure 3-14.
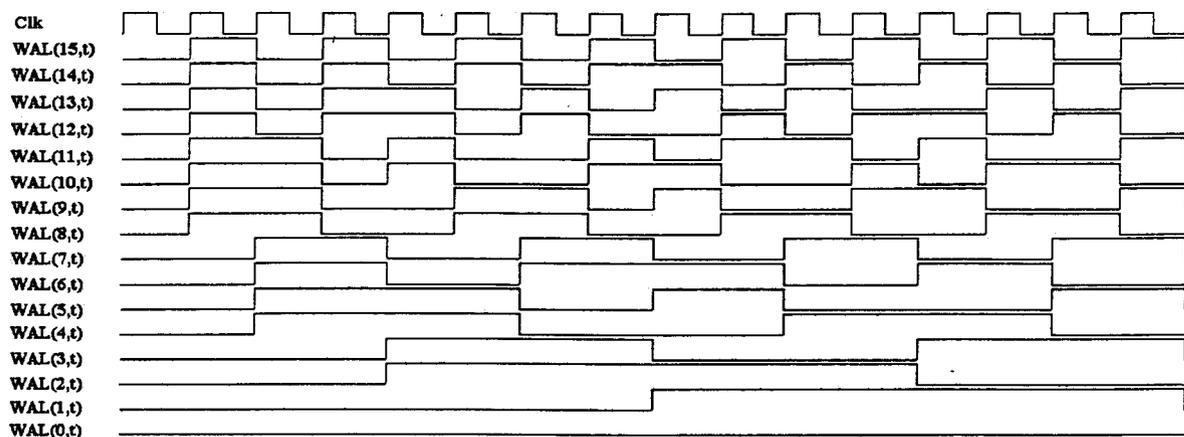
Figure 3-14 Walsh functions generated from a set of Rademacher functions.

3.4.2. Subgroup Sequencer

The subgroup sequencer determines the order in which the subgroups are selected. A subgroup sequencer is basically a ring counter of length (N/s) or a $1:(N/s)$ decoder as shown in the schematic diagram of a row driver (see Figure 3-22).

Selectina 8 rows at a time:

A 3-bit counter is used as a subgroup index to select one of the 8 subgroups. Using 3-to-8 decoder, 8 decoded outputs (SG1, SG2, ...SG8) are generated corresponding to the subgroups in the row driver. The subgroup index and the corresponding decoded outputs are shown in Table 3-3.

Table 3-3

Subgroup Index			SG1	SG2	SG3	SG4	SG5	SG6	SG7	SG8
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	1

Selecting 16 rows at a time:

Four subgroups are selected one after the other using 4 decoded outputs of a **2-bit** counter used as a subgroup index. Using 2-to-4 decoder, 4 outputs (**SG1**, SG2, SG3 and SG4) are used to select the subgroups in the row driver card. Table 3-4 shows the subgroup index and the corresponding decoded outputs to select the subgroups.

Table 3-4

Subgroup Index		SG1	SG2	SG3	SG4
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

3.4.3. Waveform Memory

The analog waveforms after sampling and quantization are stored in the waveform memory as shown in the Figure 3-15. $R(=\log_2 N)$ bits are necessary to display the waveform to the maximum resolution possible in a display with N rows. Hence, $N \times M$ matrix **LCD** requires $R \times M$ bits for storing a single waveform. To store w waveforms, w memory blocks (**i.e., WM1**, WM2,......WMw) are necessary as shown in the Figure 3-15. The memory requirement is generally low while using waveform memory rather than bit mapped memory. For example in a 256x256 matrix **LCD** the size of the bit-mapped memory is 65,536 bits. However one needs just 16,384 bits for storing 8 waveforms with 8-bit resolution. Since, the number of waveforms to be displayed is lower than the number of rows in matrix display (**i.e.**, w << N), the number of time intervals to compute the column data is more when bit mapped memory is used. But when the waveform memory is used w time intervals are necessary for each column data generation. The time necessary for column data generation can be reduced while using waveform memory. Hence, it is preferable to use sampled data directly without generating a bit mapped image of the pixels. Generation of the column data using sampled data directly is explained in detail in column signal generator (CSG) section (3.4.4).
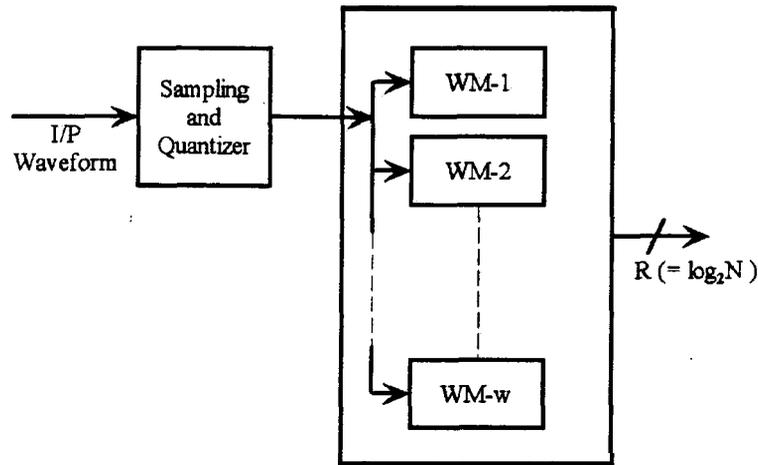
Figure 3-15 Typical block diagram of the waveform memory.

To demonstrate the technique, a 64x64 matrix **LCD** is used to display four waveforms. For each waveform 64 sample data points are required. The four waveforms sample data are stored in the EPROM, **2732A (4k×8)** in four consecutive memory locations as shown in Figure 3-16.
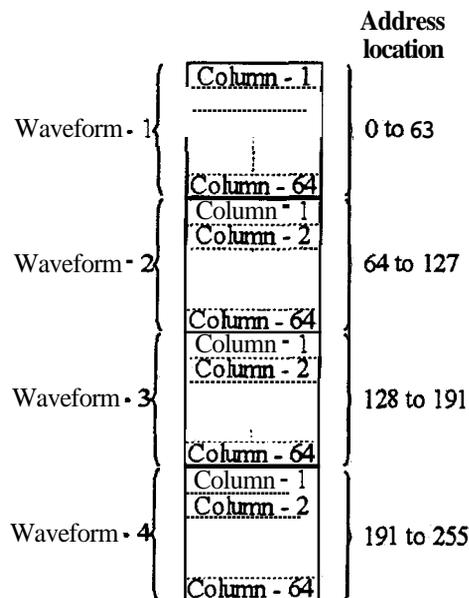
Figure 3-16 Memory allocation while storing four waveforms in EPROM.

Here, $\log_2 64$ bits are required to display the waveform to a maximum resolution possible on the 64 rows matrix display. In EPROM, **2732A** 8-bits can be stored in each memory location. Out of 8-bits, only 6 bits has the data and the remaining 2-bits are not used. To generate the column data for each column, 4 data points from the memory corresponding to the four waveforms are used. The 8-bit address (**Wmad[7..0]**) is generated using a 8-bit

counter. Two bits from the **LSB** are used as higher address lines of the memory (**Wmad[7..6]**) corresponds to the four waveform memory blocks and 6-bits (**Wmad[5..0]**) are used to address the waveform data corresponding to the 64 columns.

3.4.4. Column Signal Generator (CSG)

In a display when w waveforms are being displayed, only w pixels in each column carry the information and rest (N–w) pixels are background pixels. The data for the background pixels are assigned to be zero and hence it is not necessary to consider them while generating the column data. Only the w sampled data points are necessary to compute the column data for each column.

The block diagram of the CSG for **multi-line** restricted pattern addressing technique is shown in the Figure 3-17. It consists of three blocks (i) Digital comparator, (ii) Digital multiplexer and (iii) **Up/Down** binary Counter. Column signal generator computes the dot product of the row select pattern and the data in the selected subgroup. In general s is an integer less than N. However for a simple design s is chosen to be integer power of 2 ($s = 2^i$, where $i = 1, 2, ...$ etc.).
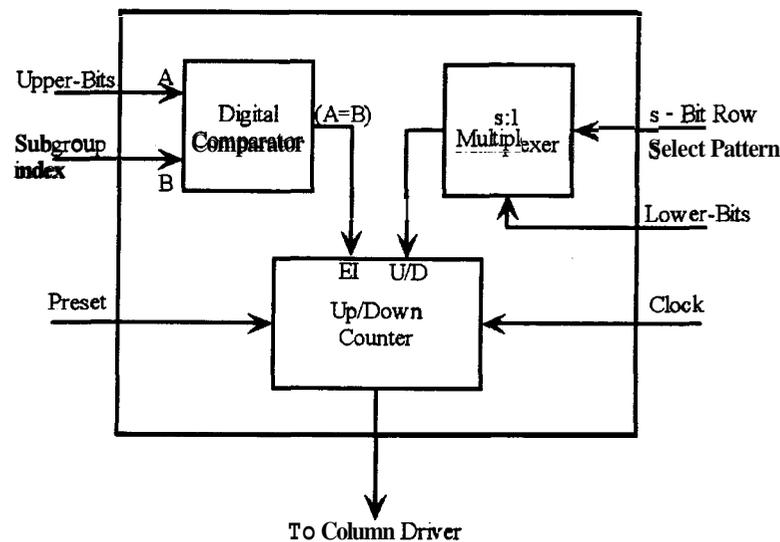
Figure 3-17 Block diagram of the column signal generator.

Every sample in the waveform memory consists of R-bits. The lower log&)-bits (LB) indicates the row in a subgroup which is an OFF (ON) pixel. The rest of $[R-\log_2(s)]$ bits are the Upper-Bits (UB) and indicates the subgroup number in which the OFF (ON) pixel is located as shown in Figure 3-18.
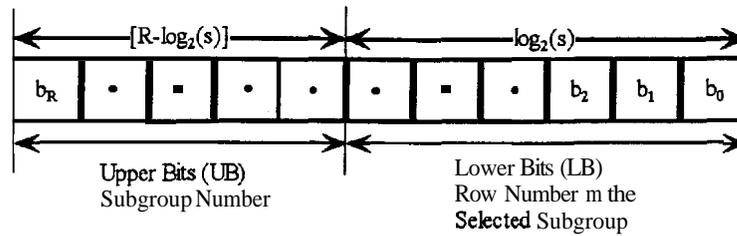
Figure 3-18 Bit allocation of the waveform sampled data used for column data generation.

The UB of the sampled data from a waveform memory is first compared with address of the selected subgroup. In this comparison a true indicates that an OFF (or ON in the case of positive contrast) pixel (which is a point on the waveform) lies in the subgroup. Once this comparison is true the LB of sample is used to get the corresponding element in the row select pattern by using a s:1 digital multiplexer. The output from this s:1 multiplexer is used as a control input to count up or down as shown in the Figure 3-17. Up/Down binary counter is used to compute the dot product between the row select pattern and the data. Initially the counter is preseted to its mid-state. For example a 3-bit binary counter is preset to 011 state before computing the dot product for each column in the selected subgroup. In case the comparison between UB of the sampled data with the address of the selected subgroup is false, then all the pixels in the corresponding subgroup of a column under consideration are background pixels. Since the data for background pixels is 0, the value of the dot product is zero and the counter value is left intact. It is important to note that the choice of a preset state of the counter is arbitrary. In fact all one needs to ensure is that the counter is preset to any one state and the dot product is assigned to be zero for that state. Once this is done rest of the counter states are assigned the appropriate dot product values. Table 3-5 shows the counter states and the corresponding voltage level in the column waveform when the preset states are chosen to be 011 and 000.

The comparator output is used to enable the counter. The output from the digital multiplexer is used to control the up or down mode of the programmable counter. For a given row select pattern w clock pulses are provided to compute the column data from w sampled data corresponding to w waveforms for each column. After computing the column data using w clock pulses, column data is shifted into the column driver card.

Table 3-5

Column voltage Level (preset = 011)	Counter state	Column voltage Level (preset = 000)
$-3V_c$	0 0 0	V_0
$-2V_c$	0 0 1	$+V_c$
$-V_c$	0 1 0	$+2V_c$
V_0	0 1 1	$+3V_c$
$+V_c$	1 0 0	Not used
$+2V_c$	1 0 1	$-3V_c$
$+3V_c$	1 1 0	$-2V_c$
Not used	1 1 1	$-V_c$

The counter is again preset to the initial value. Column data for the rest of the columns are computed by repeating the process and are shifted in to the column driver for driving the matrix LCD. Hence $(w \times M)$ time intervals are necessary to generate all the column data for each row select pattern. It is important to note that the time necessary to generate these column data depends on the number of column in the display as well as on the number of waveforms being displayed (w) and is independent of N or s.
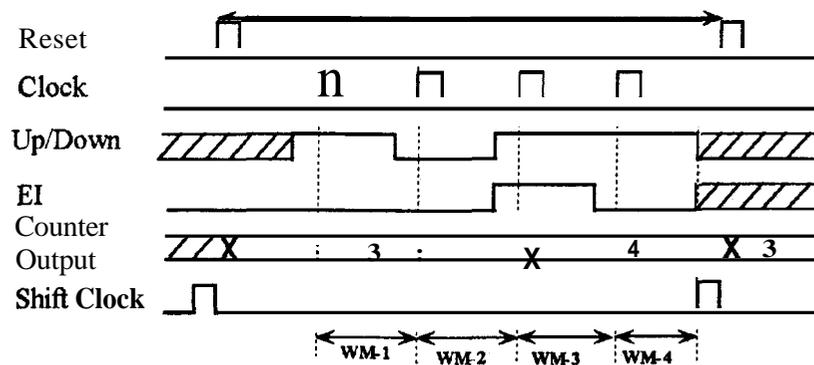
Figure 3-19 Typical timing diagram of the CSG to compute the column data.

Waveforms in Figure 3-19 shows the sequence of operation in CSG for displaying 4 waveforms using a 3-bit counter. The initial state of the counter corresponds to the column voltage level V_0 as shown in the Table 3-5. This state is left undisturbed whenever there is

no match between the UB and the subgroup address. The column signal generator is implemented using a s : 1multiplexer, a UB-bit comparator and a 3-bit **Up/Down** binary counter. The counter outputs are used to generate dot product of the row select pattern and the data in a selected subgroup of a column.

The 6-bit data (**Data[5..0]**) from the data memory is divided into two parts as UB and **LB**. While selecting 8 rows at a time, the three bits from LSB (**Data[2..0]**) are used as LB and the remaining three bits (**Data[5..3]**) are used as UB. When 16 rows are selected at a time, four bits from LSB (**Data[3..0]**) are used as LB and the other two bits are used as UB (**Data[5..4]**). The UB indicates the subgroup number in which the sampled data point is located. The LB gives the corresponding row in the selected subgroup. While selecting 8 rows at a time, a 3-bit comparator and a **8:1** digital multiplexer are used. For selecting 16 rows at a time, a 2-bit comparator and a **16:1** digital multiplexer are used. The **Wmad_clk** is used as a clock for the 8-bit counter to generate the address lines for reading the waveform sampled data from the data memory. At every rising edge of this clock, the address lines are changed as shown in the Figure 3-20. The sampled data is stable between the two rising edges of the **Wmad_clk.** The falling edge of the **Wmad_clk** is used as the clock for the 3-bit **Up/Down** counter. The counter is enabled only when there is a match between the subgroup index and the UB. This comparison is done before the falling edge of the **Wmad_clk** using the comparator. The comparator output goes high only when the UB and subgroup index matches. If the comparator output is high it means the sampled data point belongs to the selected subgroup. The output from the multiplexer is used to control the up or down mode of the programmable counter. The multiplexer sends the one bit row select pattern corresponding to the sampled data points at the time of selection using LB. If the comparator output is low, then counter is disable and the counter output will remain same. At the end of four **Wmad_clk,** four waveform sampled data points are selected and the dot product output from the counter is shifted to the column driver using the rising edge of the shift clock (**Shift_clk**). After shifting the column data the counter is preset to its initial state using the preset pulse as shown in the Figure 3-20. The entire process is repeated for the next column and all the 64 column data are generated and shifted to the column driver card.
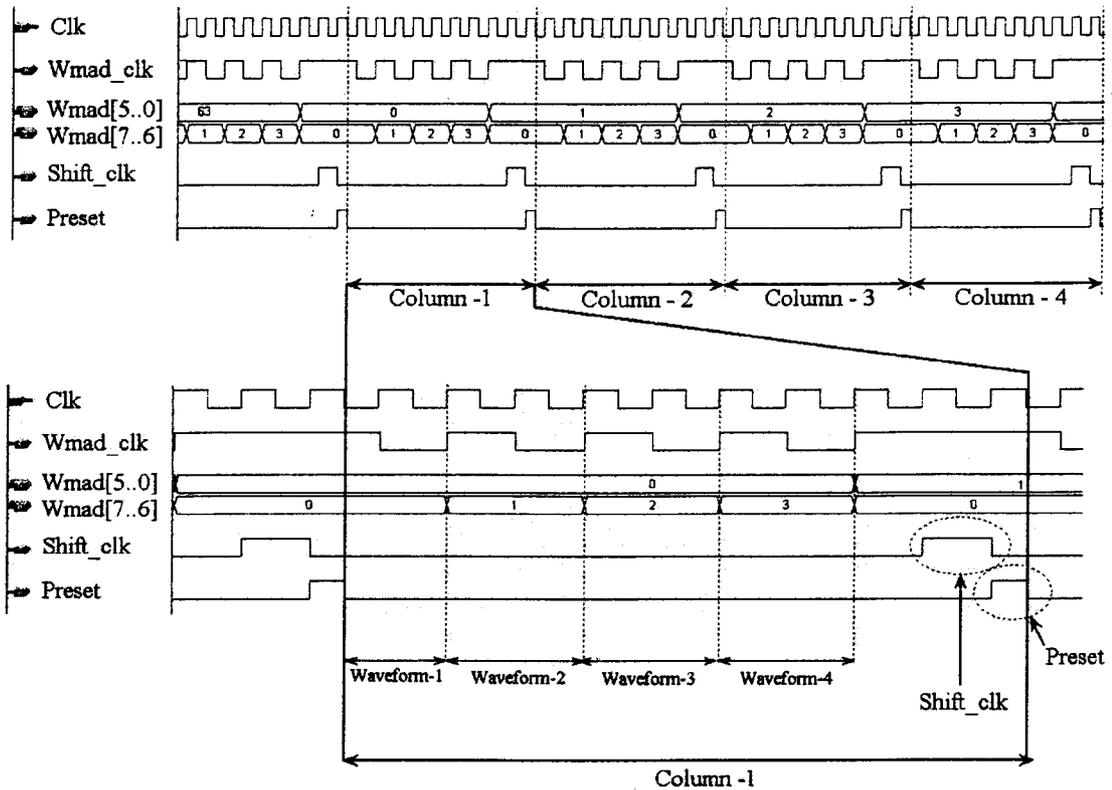
Figure 3-20 Timing and control signals to compute the column data for each column.

3.4.5. Voltage Level Generator

The voltage levels for row and column drivers are generated using voltage level generator (VLG). It is a simple voltage divider network as shown in the Figure 3-21.

$$V_r = \sqrt{w}\ V_c$$

$$w = 4,\ V_r = 2\ V_c$$
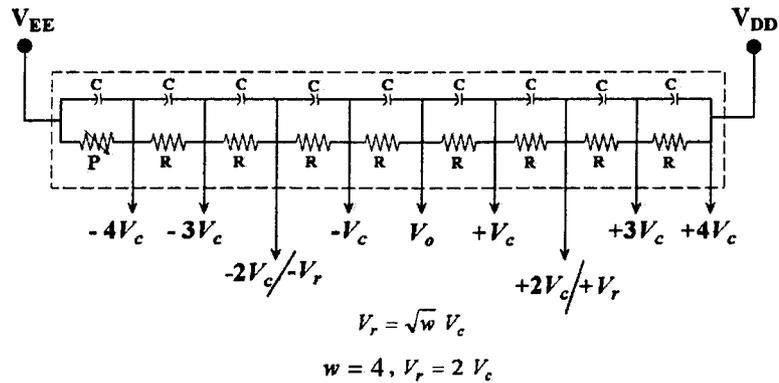
Figure 3-21 Voltage divider network used for generating voltage levels for the row and column driver.

Capacitor (C) is used to reduce the distortion of the drive waveforms at the voltage switching time. The potentiometer (P) is used to change the absolute value of the voltage

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level for row and column waveforms without affecting their ratios. The relative amplitudes of the row and column voltage levels depend on the technique and it is generated by a proper choice of the resistor values. To display four waveforms for overlapping case in general all the voltage levels i.e, 0, ±Vc, ±2Vc, ±3Vc and ±4Vc are necessary for the column waveforms. Figure 3-21 shows the VLG used for generating row and column voltage levels for displaying four waveforms.

3.4.6. *Row Driver*

In multi-line addressing techniques the row waveforms have three voltage levels. Two voltage levels $+V_r$ and $-V_r$ to select the rows in a selected subgroup while V_0 for the unselected rows. The detail schematic diagram of the row driver card is shown in Figure 3-22. Row driver is implemented using CD4053 triple, 2:1analog multiplexer/demultiplexer. The s-bit row select patterns +1 and −1 (i.e., logic 0 and logic 1) are level shifted to row voltage levels $-V_r$ and $+V_r$, respectively using s 2:1 analog multiplexers. The outputs from the s 2:1 multiplexers i.e., RW-1,RW-2….RW-s and V_o from the voltage level generator are connected to each subgroup blocks. The s multiplexers are grouped together and are controlled using a common control input from the subgroup sequencer. Subgroup sequencer generates the (%)outputs [SG1,SG2,.......,SG(N/s)] to control the sequence in which the subgroups are selected. Only one out of SG1...SG(N/s) will be high at any instant of time (see Table 3-3 and Table 3-4). The output from the corresponding subgroup will produce the voltage levels $+V_r$ or $-V_r$ depending on the row select patterns −1 or +1, respectively. The rest of the (N − s) outputs from the other subgroups are at the voltage levels V_o. While selecting 8 rows at a time, eight 2:1 analog multiplexer are used as voltage level selectors and eight 2:1 analog multiplexers are grouped together in each subgroup blocks and selected from the subgroup sequencer [SG1,SG2,......SG8]. Similarly for selecting 16 rows at a time, sixteen 2:1 analog multiplexers are used in voltage level selector. Instead of grouping eight 2:1 multiplexer, in this case sixteen 2:1 multiplexers are grouped and four subgroups are controlled by SG1, SG2, SG3 and SG4.
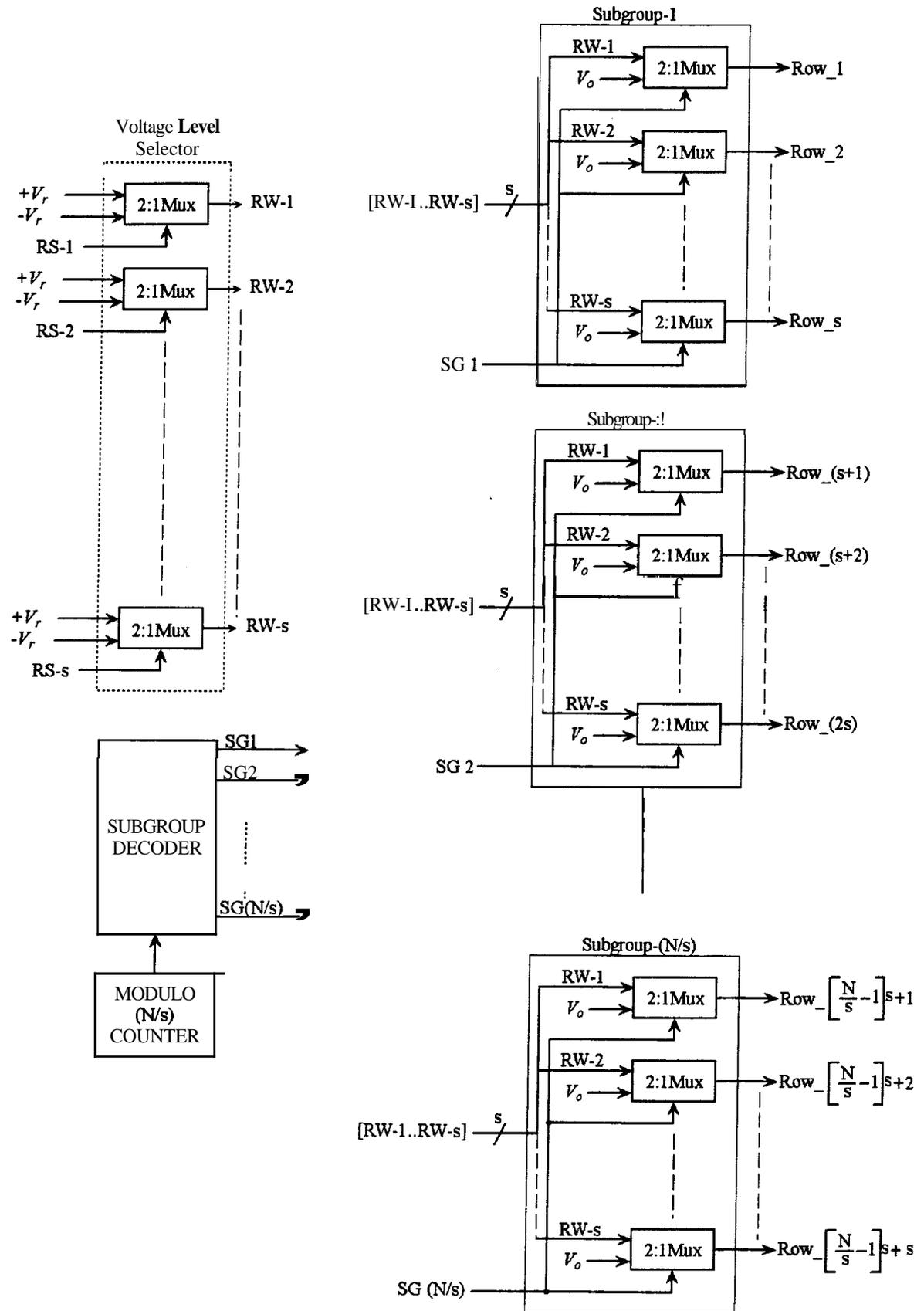
Figure 3-22 Schematic block diagram of the row driver.

3.4.7. Column Driver

In applications like Oscilloscope displays all the waveforms may appear in the same subgroup. Then, $(w+1)$ voltage levels are used to generate the column waveform for displaying w waveforms. In this case column driver should be capable of generating $(w+1)$ voltage levels. Actually one can use the commercial drivers, which are available to generate voltage levels in the column waveform. But the connector's pitch is very small and hence it is difficult to handle. The standard driver that is used to drive matrix LCD line by line gives only two voltage levels at any instant of time. Here, column driver card has been designed for driving up to 8 voltage levels using a shift register with latch and a **8:1** analog multiplexer. Figure 3-23 shows the schematic of the column driver for generating 8 levels with 64 output lines. Where, $X(n), Y(n)$ and $Z(n)$ are the three bit column data, SLK is the shift clock and the LP is the latch pulse. $\dot{V}_{0-7}$ are the column voltage amplitudes from the voltage level generator to 8:1 analog multiplexers.
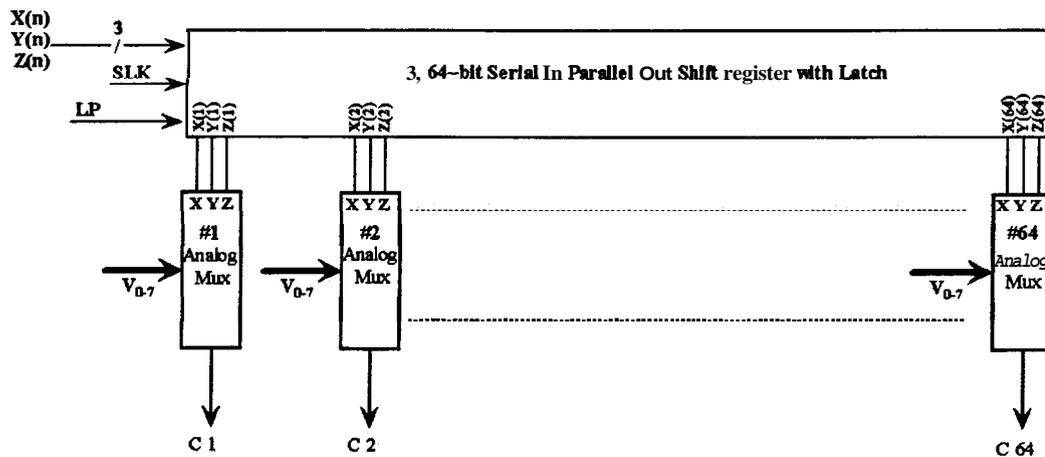
Figure 3-23 Schematic diagram of the column driver to generate 8 voltage levels.

Column driver is implemented using standard LCD driver SED 1180 and a **8:1** analog multiplexer (CD 4051) for each column output as shown in the Figure 3-24. Here, SED 1180 is used as serial in parallel out **(SIPO)** shift register with latch. SED 1180 has 64-bit shift register. The data is shifted into the shift register using falling edge of the shift clock (SLK). The data from the shift register is moved into the 64-bit latch on the falling edge of the latch pulse (LP). At any instant of time only two voltage levels are available at the outputs depending on the data (0 or 1) stored in the latch. The 3-bit column data $(X(n), Y(n)$ and $Z(n))$ from the column signal generator is shifted in to the three SED 1180

using common shift clock (**SLK**). The three bit column data are taken parallel to the 8:1 multiplexer (CD **4051**) using a latch pulse (LP). The column driver card shown in Figure **3-24** is used for displaying overlapping waveforms.
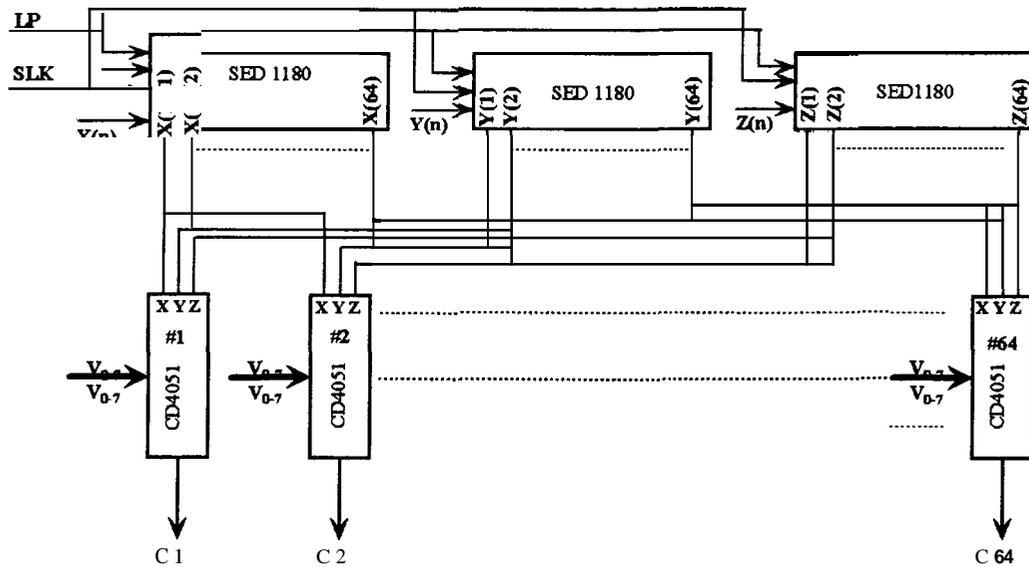
Figure 3-24 Schematic of the column driver using SED1180 and CD4051 to generate 8 voltage levels.

To display four non overlapping waveforms in a **64x64** matrix display by selecting 16 rows at a time, only two voltage levels are necessary in the column waveform. This is because, only one waveform is being displayed in each subgroup. In this case one bit column data from **CSG** is shifted to column driver.

To Column Electrodes
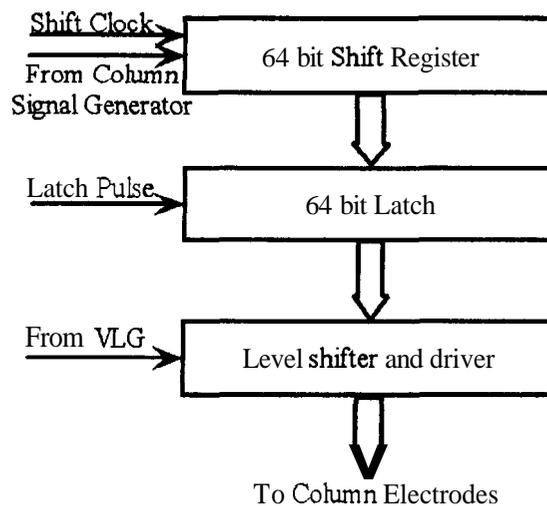
Figure 3-25 Schematic of the column driver to generate two voltage levels.

The block diagram of a column driver necessary in this case is as shown in Figure 3-25. It consists of 64-bit serial in parallel out shift register, 64-bit latch and a level shifter with driver. This will simplify the column driver necessary for displaying four waveforms. A standard LCD driver can be used as column driver. In this case the standard column driver SED 1180 is used.

3.4.8. Control Logic

This block comprises of generation of address for the waveform memory and row select pattern memory. Timing and control circuit to synchronize the flow of signals to scan the display. All the necessary timing signals such as column data shift clock, subgroup sequencer to select the appropriate subgroup and latch pulse for both the column and row drivers are generated.

a)   Shift Clock

The column data from the column signal generator is shifted to the column driver using a shift clock pulse (SLK) for each column.

b)   Preset Pulse

After shifting the column data the counter in the CSG is preset every time to its initial value using the preset pulse.

c)   Latch pulse

After shifting all the 64 column data to the column driver card, both the column voltage and row voltage are latched to the matrix display using a latch pulse (LP).

All the control signals were first simulated using Altera MAX-plus II software. The timing sequence between two latch pulses is shown in Figure 3-26. The industry standard Joint Test Action Group (JTAG) interface for programming or configuring mode is available in MAX 7000S series CPLDs. The ByteBlaster with a parallel port interfaces to the parallel port of a PC and the CPLD. After verifying the simulated data, the code is downloaded from the PC's parallel port through the ByteBlaster to the CPLD via the JTAG pins in the CPLD. The controller has been successfully implemented for selecting 8 and 16

rows at a time. The four waveforms are displayed using a **64x64** matrix **LCD** for both overlapping and non-overlapping cases.
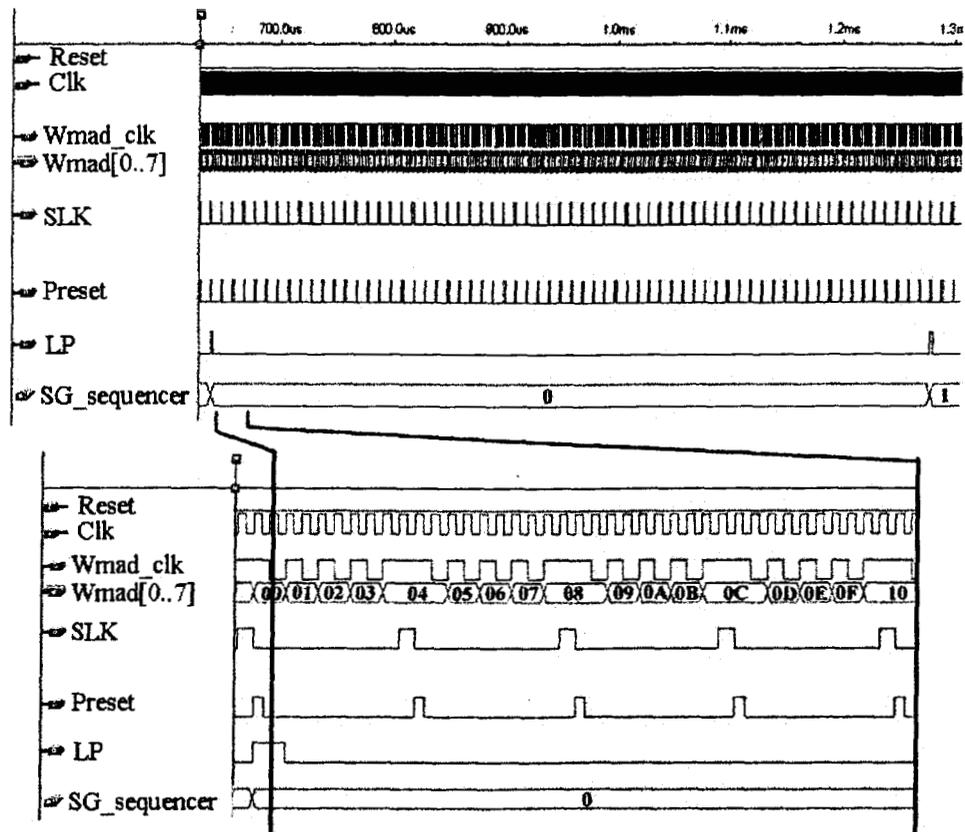
Figure 3-26 Timing and control signals generated between the two latch pulse showing shift clock, Preset and EPROM address.

Reset	Power on reset
Clk	Master clock to generate all necessary control signals
Wmad_clk	Clock for the waveform memory address generator counter
Wmad[7..0]	8-bit waveform memory address for reading the waveforms pixel information
SLK	Shift clock to shift the column data to column driver card (SED 1180)
Preset	To preset the CSG counter value after every CSG operation
LP	To latch all the row and column data in the display driver
SG_sequence	To select the subgroup sequentially one after the other to scan the display

3.5. Results and Discussion

The addressing technique discussed in this chapter has been implemented using a 64x64 matrix TN LCD. Photograph 3-1 shows the picture of displaying four waveforms by selecting 8 rows at a time using multi-line restricted pattern addressing technique. As one can see in the Photograph 3-1 the waveforms are overlapping in one of the subgroup. The typical addressing waveforms applied to the row and column of the matrix LCD as well as the waveform across the ON and OFF pixels are captured using Tektronix digital storage oscilloscope TDS 220. The number of voltage levels in the column waveforms depends on the number of waveforms present in the selected subgroup. Figure 3-27 shows the row and column waveforms while selecting 8 rows at a time when overlapping waveforms are displayed. The row and column waveforms shown in Figure 3-27(a) and (b) are one of the OFF and ON pixels, respectively. These waveforms are captured when four waveforms shown in Photograph 3-1 were displayed. Figure 3-27(a) and (b) shows the five voltage levels (i.e., $+2V_c, +V_c, V_o, -V_c$ and $-2V_c$) in the column waveform. In this case for a particular column two waveforms are present in a column of a selected subgroup. Figure 3-27(c) and (d) shows the resultant waveforms across the OFF and ON pixels respectively.
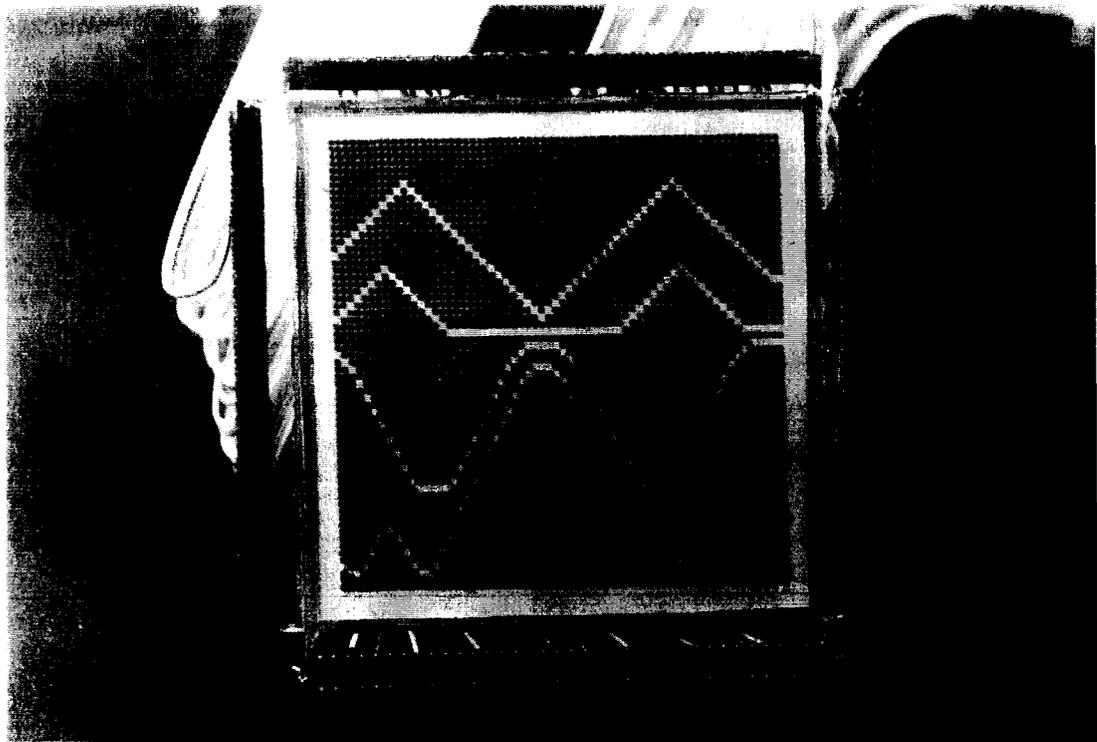
Photograph 3-1 A 64x64 matrix TN LCD displaying four waveforms by selecting 8 rows at a time.
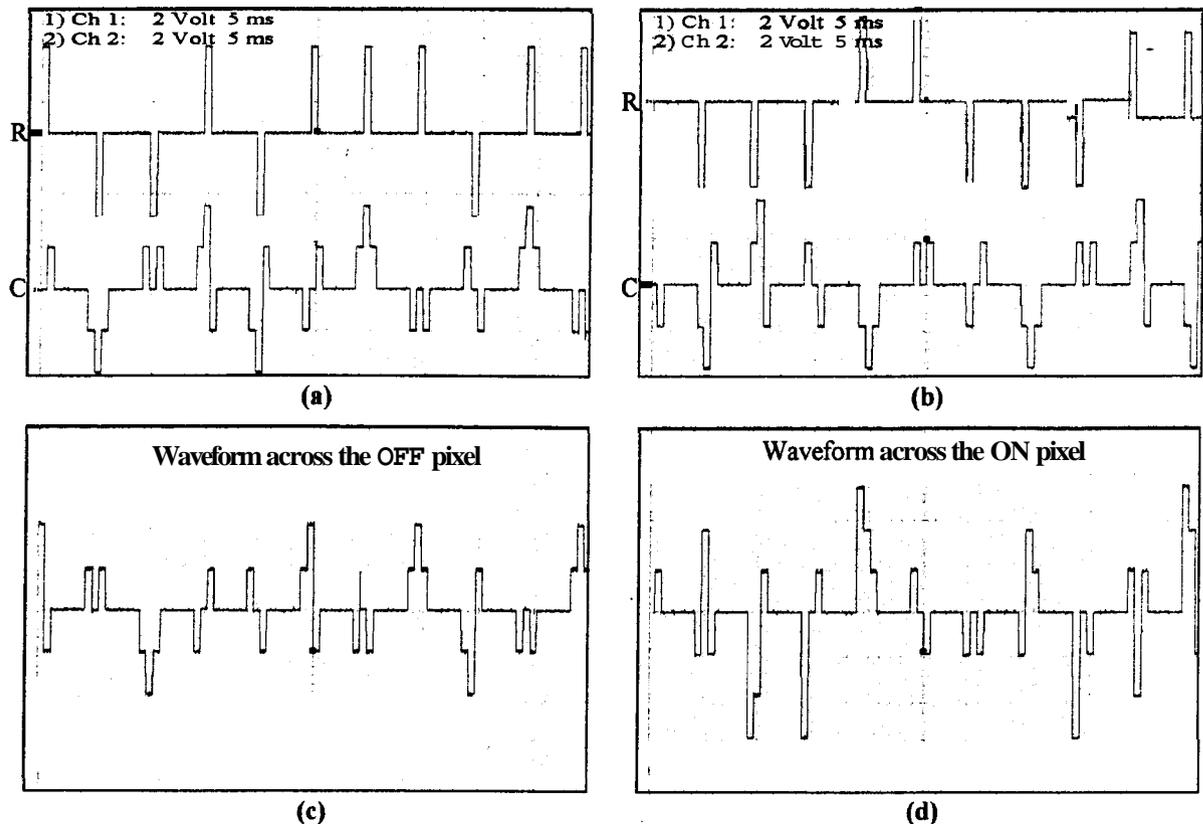
Figure 3-27 Typical addressing waveforms of 64x64 matrix addressed using multi-line restricted pattern addressing technique by selecting **8 rows at a time. (a)** row and column waveforms of an OFF pixel, **(b)** row and column waveforms of an ON pixel **(c)** and **(d)** resultant waveforms across the OFF and ON pixels respectively.

Photograph 3-2 shows the picture of displaying four waveforms by selecting 8 rows at a time using multi-line restricted pattern addressing technique. Here, waveforms are equally spaced to each other and only one waveform may be present in a subgroup. In this case only three voltage levels (i.e., $+V_c$, V_o and $-V_c$) in the column waveform are necessary. Figure **3-28(a)** and (b) shows one of the row and column waveforms for OFF and ON pixels, respectively. Figures **3.29(c)** and (d) shows the resultant waveforms across the OFF and ON pixels. Photograph 3-3 shows the 64x64 matrix **LCD** displaying four waveforms by selecting 16 rows at a time. Here again the waveforms are equally spaced and only one waveform is present in each subgroup. Hence, only two voltage levels $+V_c$ and $-V_c$ in the column waveforms are necessary to display four waveforms. Figure 3-29 (a) shows one of the row and column waveforms of an OFF pixel and Figure **3-29(b)** shows the row and column waveforms of an ON pixel. Figure 3-29 (c) and (d) shows the resultant waveform across the OFF and ON pixels respectively.

Photograph 3-2 A 64x64 matrix TN LCD displaying four non overlapping waveforms by selecting 8 rows at a time.

(a)

(b)

Waveform across the OFF pixel

(c)

Waveform across the ON pixel

(d)
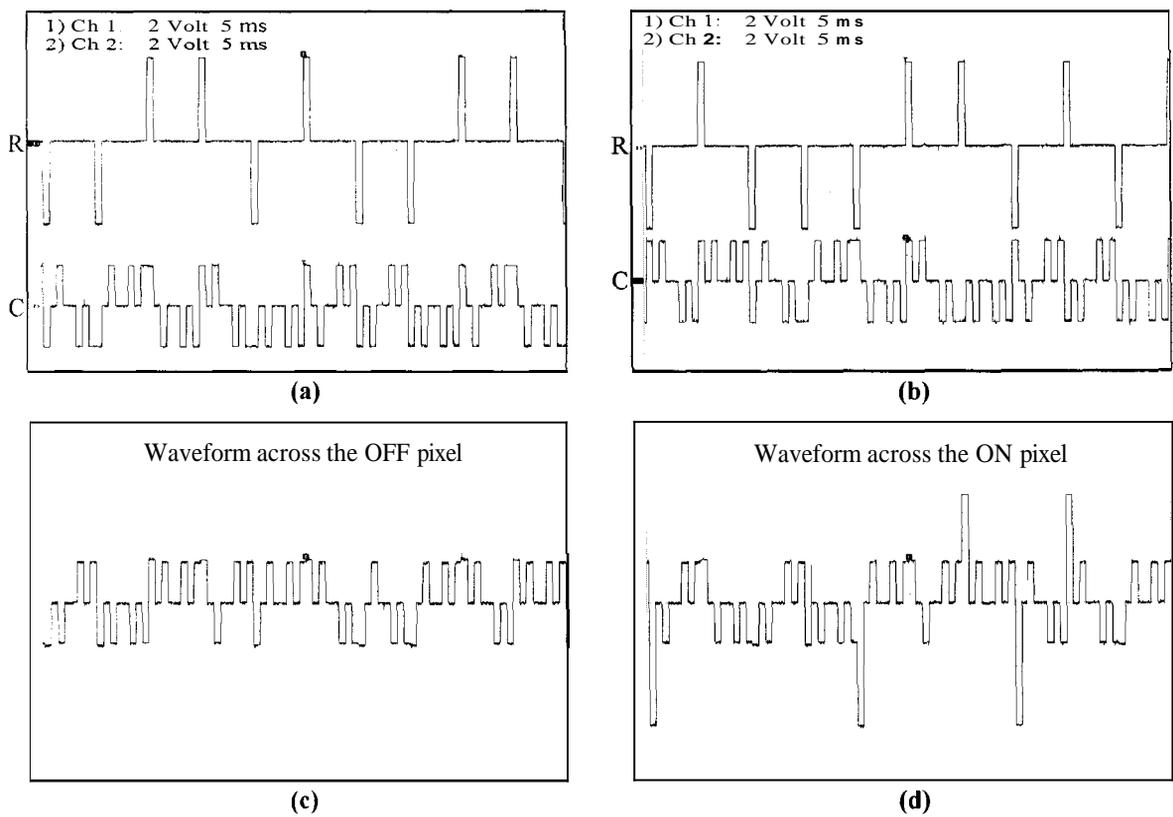
Figure 3-28 Typical addressing waveforms of 64x64 matrix displaying four waveforms by selecting 8 rows at a time. **(a)row** and column waveforms of an OFF pixel, (b) the row and column waveforms of an ON pixel (c) and (d) resultant waveforms across the OFF and ON pixels respectively.
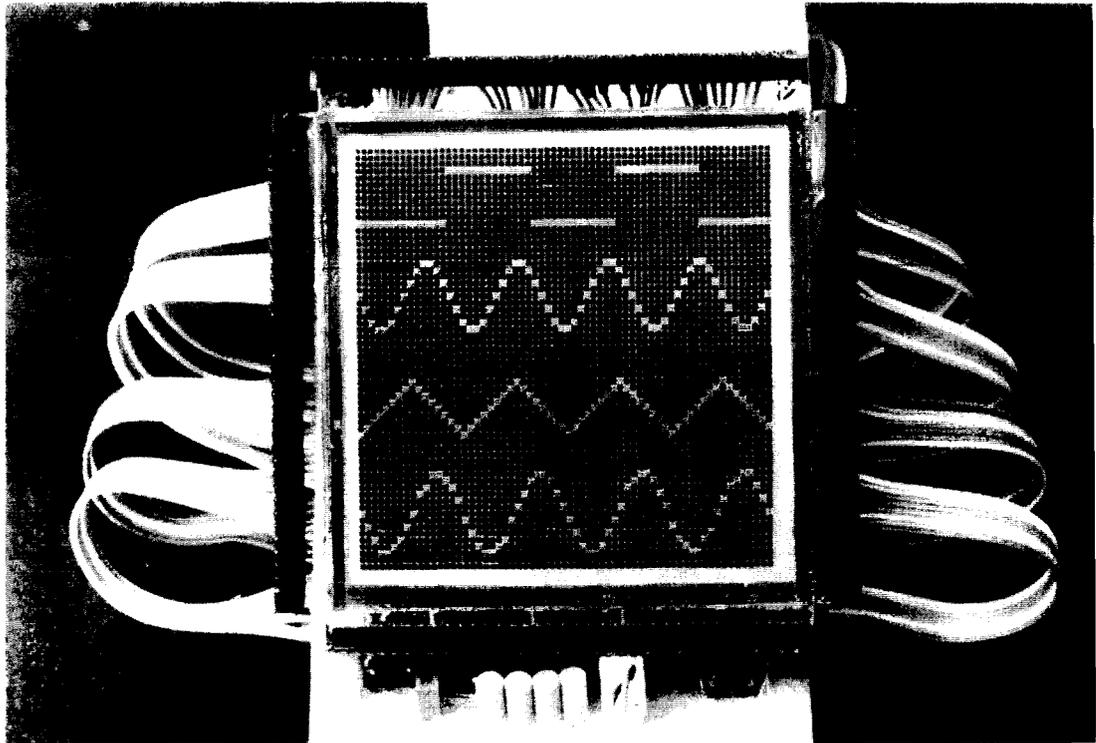
Photograph 3-3 A 64x64 matrix TN LCD displaying four waveforms selecting 16 rows at a time.

(a)

(b)

Waveform across the OFF pixel

Waveform across the ON pixel

(c)

(d)
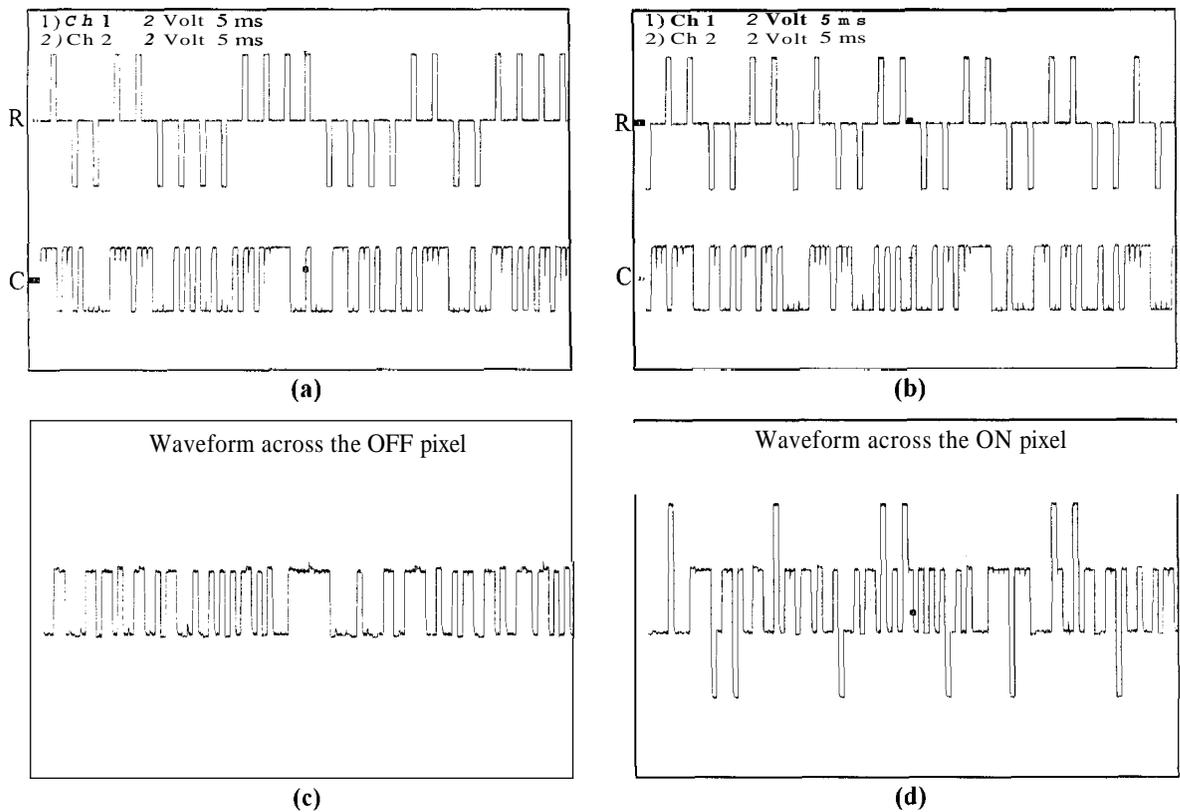
Figure 3-29 Typical addressing waveforms of 64x64 matrix addressed using multi-line restricted pattern addressing technique by selecting 16 rows at a time. (a) row and column waveforms of an OFF pixel, (b) row and column waveforms of an ON pixel (c) and (d) resultant waveforms across the OFF and ON pixels respectively.
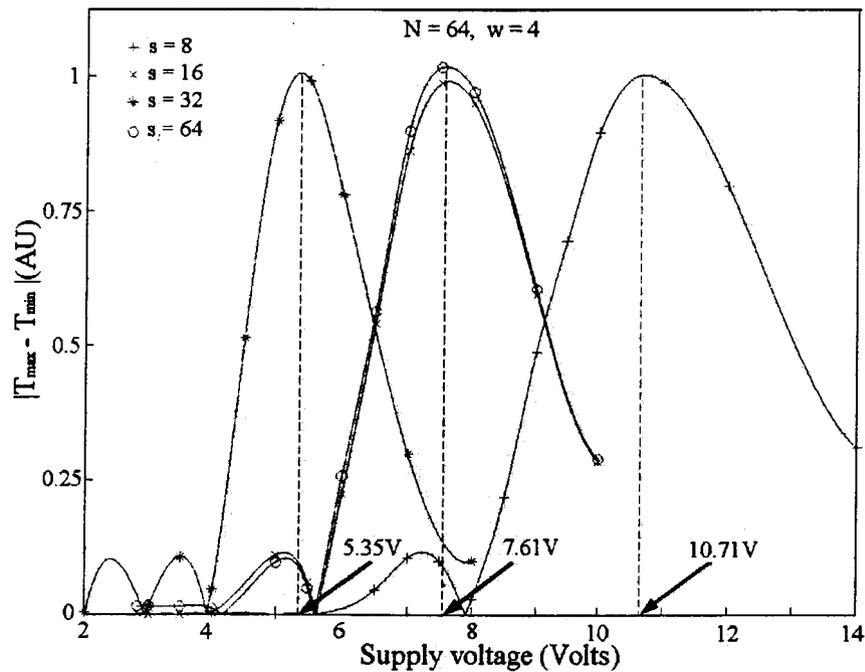
Figure 3-30 Supply voltage requirement for different subgroup sizes for displaying four waveforms in a 64x64 matrix LCD.

Saturation voltage for the liquid crystal mixture used was measured using single pixel electro-optic setup (see Chapter 4, section 4.8). The V_{90} (voltage at 90% of the maximum transmission) for the liquid crystal mixture is 2.66 volts. Supply voltage (V_{sup}) for the driver is calculated and measured for different values of subgroup size for displaying four waveforms. Row and column waveforms are generated using the waveform generator WFG 500. Figure 3-30 shows the result of the experimentally determined supply voltage requirement for different subgroup sizes. The transmission across the single pixel is measured and the supply voltage is noted for the maximum contrast (i.e, maximum transmission difference between the ON and OFF pixels). The actual supply voltage requirement for drive electronics is compared from the theoretical values that are tabulated in Table 3-1. The results agree within 1% of the measured value in case of 64x64 matrix LCD while displaying 4 waveforms as indicated by arrows in the Figure 3-30. While selecting 16 rows at a time, supply voltage requirement is equal to that of PRBS-NC technique for displaying four waveforms. In this case, the number of subgroups is equal to the number of waveforms to be displayed. The supply voltage is minimum when the maximum swing in the row waveform is equal to the maximum swing in the column

waveform. The minimum supply voltage requirement as predicted theoretically is verified for $s = 32$.
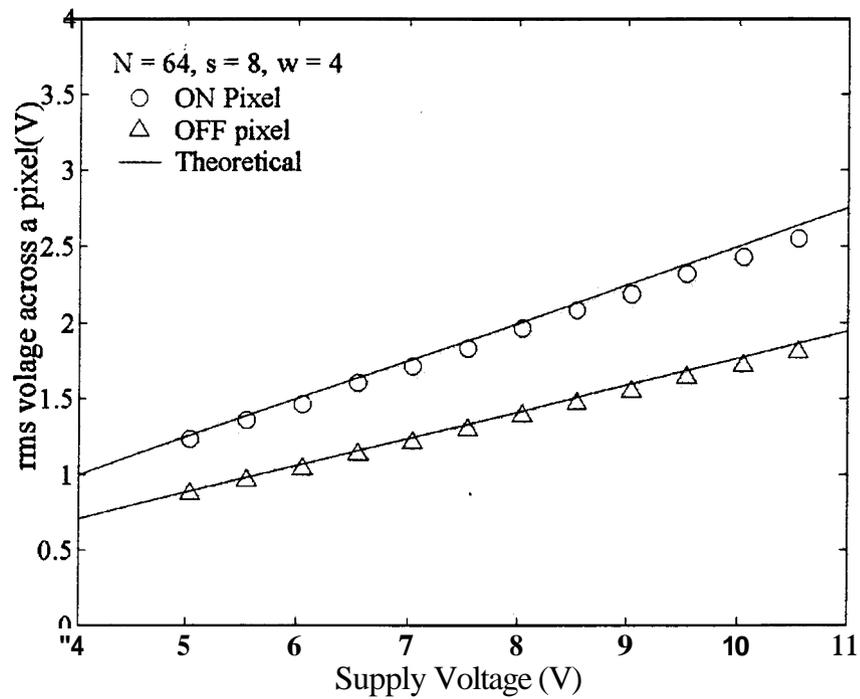
Figure 3-31 The rms voltage variation across the ON and OFF pixels with supply voltage when N = 64, $s = 8$ and $w = 4$.
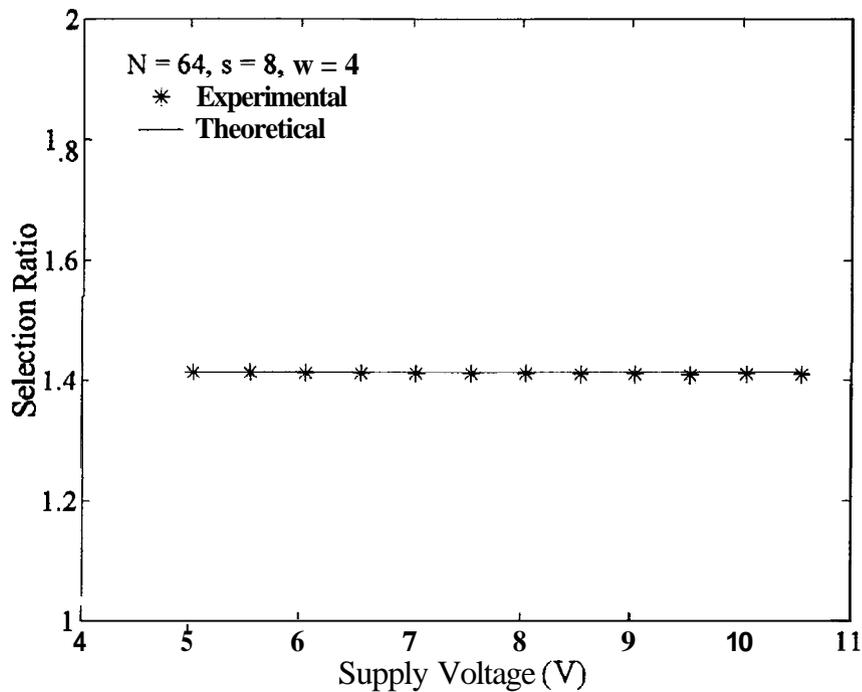
Figure 3-32 Selection ratio versus Supply voltage while displaying four waveforms.
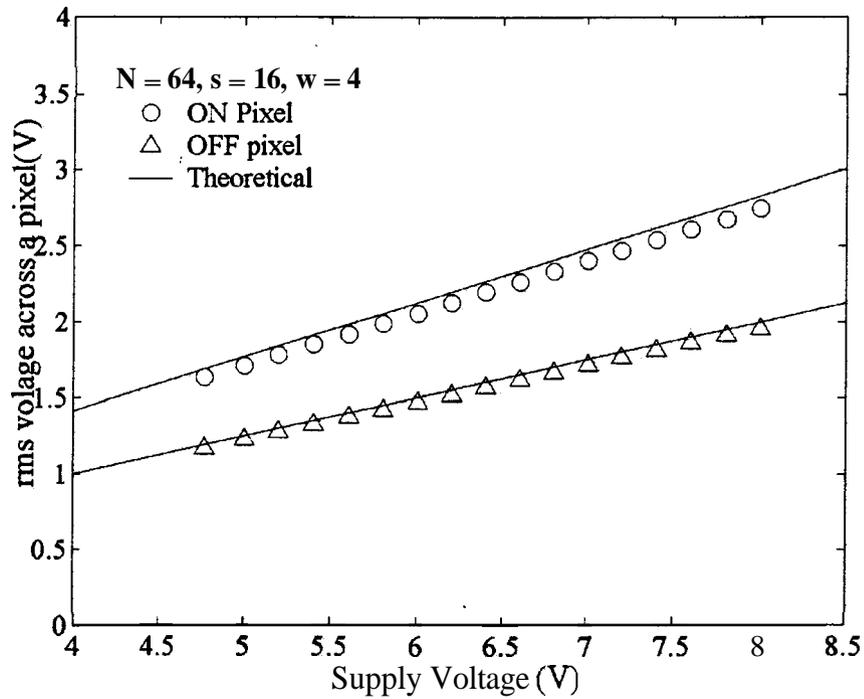
Figure 3-33 The rms voltage variation across the ON and OFF pixels with supply voltage when N = 64, s = 16 and w = 4.
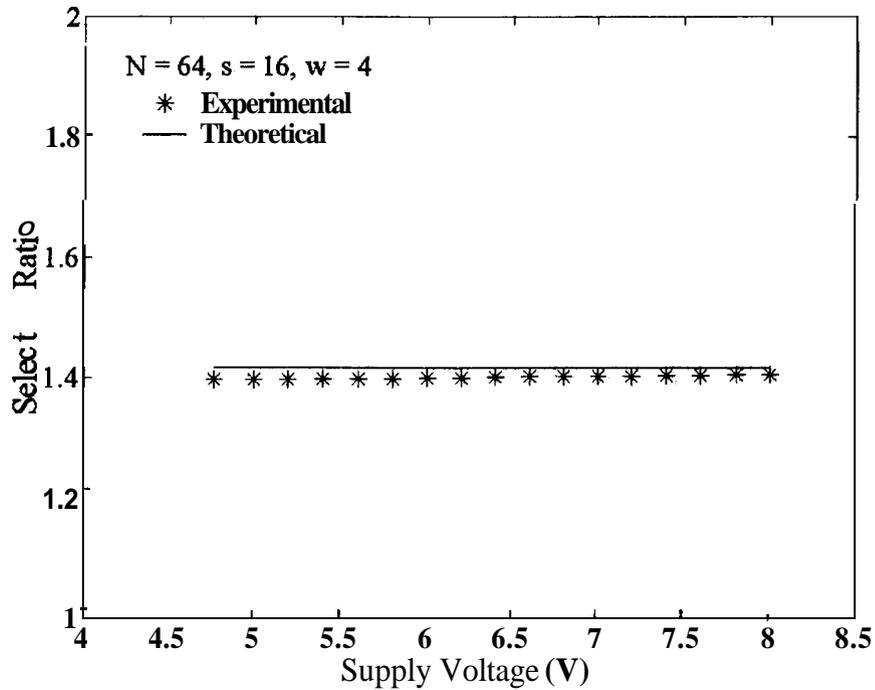
Figure 3-34 Selection ratio versus Supply voltage while displaying four waveforms.

The rms voltage across the ON and OFF pixels were measured using HP3467A, a logging multimeter. The rms voltage across the ON and OFF pixels versus supply voltage while

selecting 8 and 16 rows at a time for displaying 4 waveforms are plotted in Figure 3-31 and Figure 3-33, respectively. Optimum selection ratio (SR) for multi-line restricted pattern addressing technique of negative contrast mode is given by SR = ———— (from equation 3.7), where w is the number of waveforms being displayed. Figure 3-32 and Figure 3-34 shows the plot of the selection ratio measured versus various values of supply voltage for $s = 8$ and $s = 16$, respectively. The selection ratio obtained from measurements is less by 1.5% of the theoretical value.

In order to study the brightness uniformity of the pixels, the frequency spectrum of the waveform across the pixels with different orthogonal functions to select the subgroups were studied. The orthogonal matrix for selecting the subgroups is derived from PRBS and Walsh functions. The data for row and column waveforms for a 64x64 matrix to display four waveforms were computed using $MATLAB^{®}$. Two different subgroups size were considered for displaying four waveforms, i.e., $s = 8$ and $s = 16$. In both the cases the row select pattern generated from Walsh and PRBS are considered. The actual waveforms were generated using WFG-500. The Anritsu spectrum analyzer MS420K was used to capture the frequency spectrum. Spectrum analyzer was controlled by a computer with GPIB interface using C-program.

Figure 3-35 shows the magnitude response and the total power distribution across one of the ON and OFF pixel. Here, row select patterns are generated from the PRBS for the case of selecting 8 and 16 rows at a time. Figure 3-36 shows the magnitude response and the total power distribution when row select patterns are generated from the Walsh functions while selecting 8 and 16 rows at a time across the ON and OFF pixel. From the Figure 3-35 and Figure 3-36, it is clear that 99% of the total power is distributed within the frequency range of 3kHz in both the cases. The magnitude spectrum was taken for all the different row waveforms in the case of PRBS and Walsh functions while selecting 8 and 16 rows at a time. From these spectrums it is clear that while scanning the display using PRBS, the spectrum across the all the pixels looks very similar. Figure 3-37 and Figure 3-39 shows the spectrum of waveforms across the pixel while selecting 8 and 16 rows at a time respectively when row select patterns are derived from PRBS. Similarly, Figure 3-38 and Figure 3-40 shows the spectrum while selecting 8 and 16 rows at a time respectively

when row select patterns are derived from Walsh functions. Total power distribution in both cases **PRBS** and Walsh are same. The magnitude spectrum differs slightly from-one row to another. This is because the number of transitions for the case **PRBS** is almost same for all the row waveforms as compared to one derived from Walsh functions.
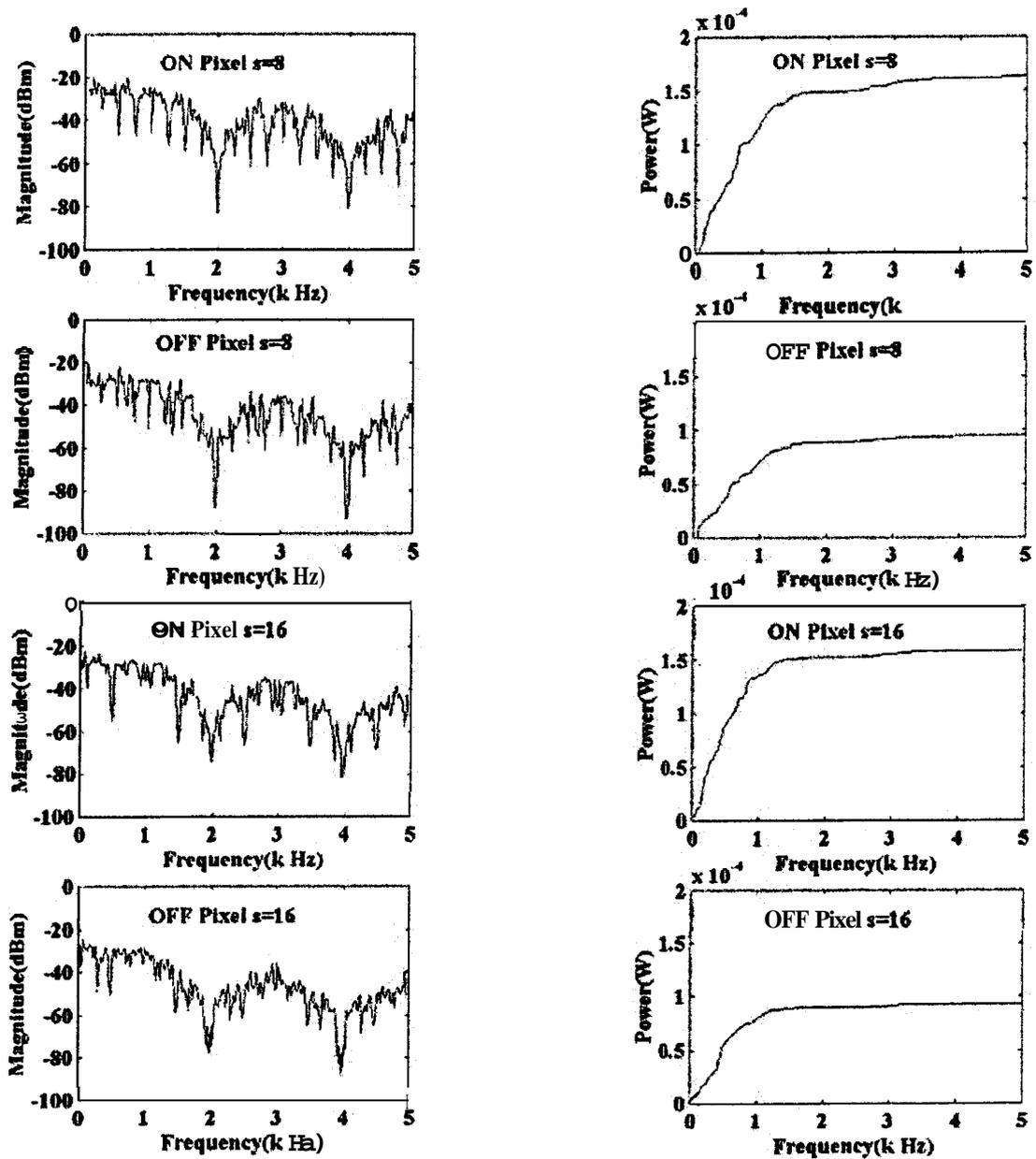
Figure 3-35 Magnitude and total power distribution across the ON and OFF pixels for the case of PRBS as row select pattern while selecting 8 and 16 rows at a time for a 64x64 matrix LCD to display 4 waveforms.
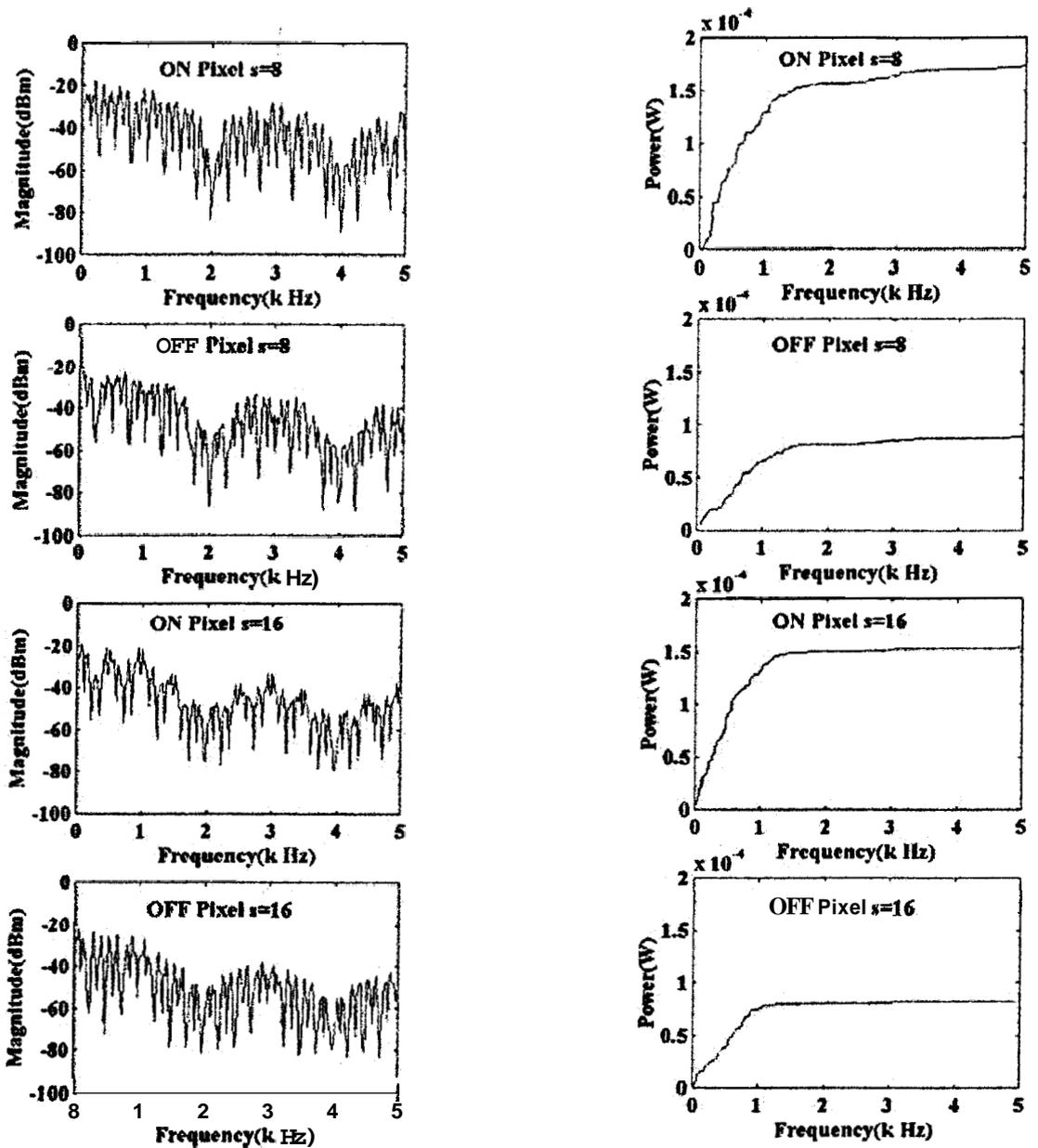
Figure 3-36 Magnitude and total power distribution across the ON and OFF pixels when row select pattern is derived from the Walsh functions while selecting 8 and 16 rows at a time for a 64x64 matrix LCD to display 4 waveforms.
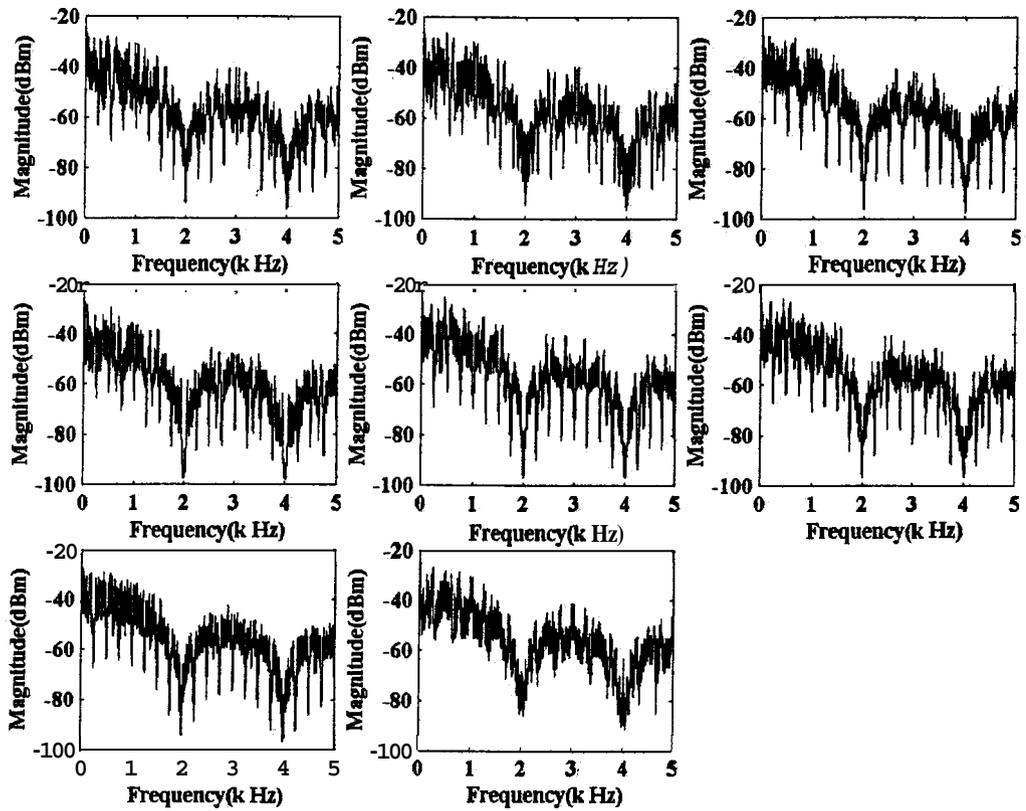
Figure 3-37 The magnitude spectrum of waveforms across the pixels while selecting 8 rows at a time when row select patterns are derived from PRBS.
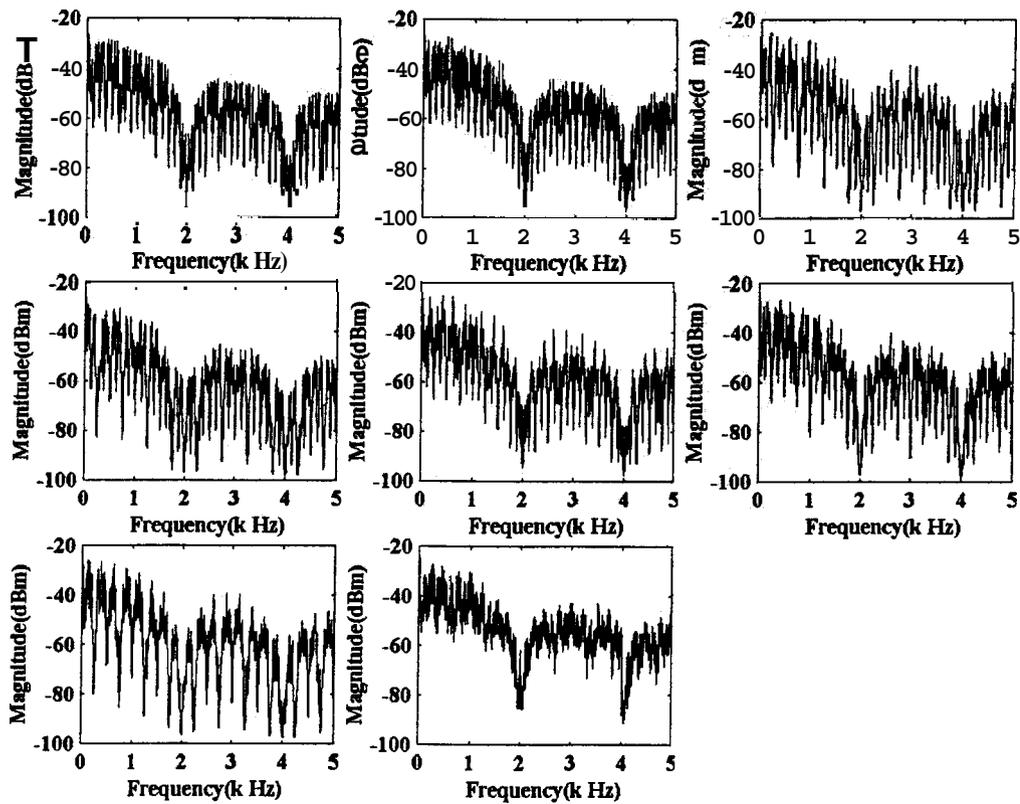
Figure 3-38 The magnitude spectrum of waveforms across the pixels while selecting 8 rows at a time when row select patterns are derived from Walsh functions.
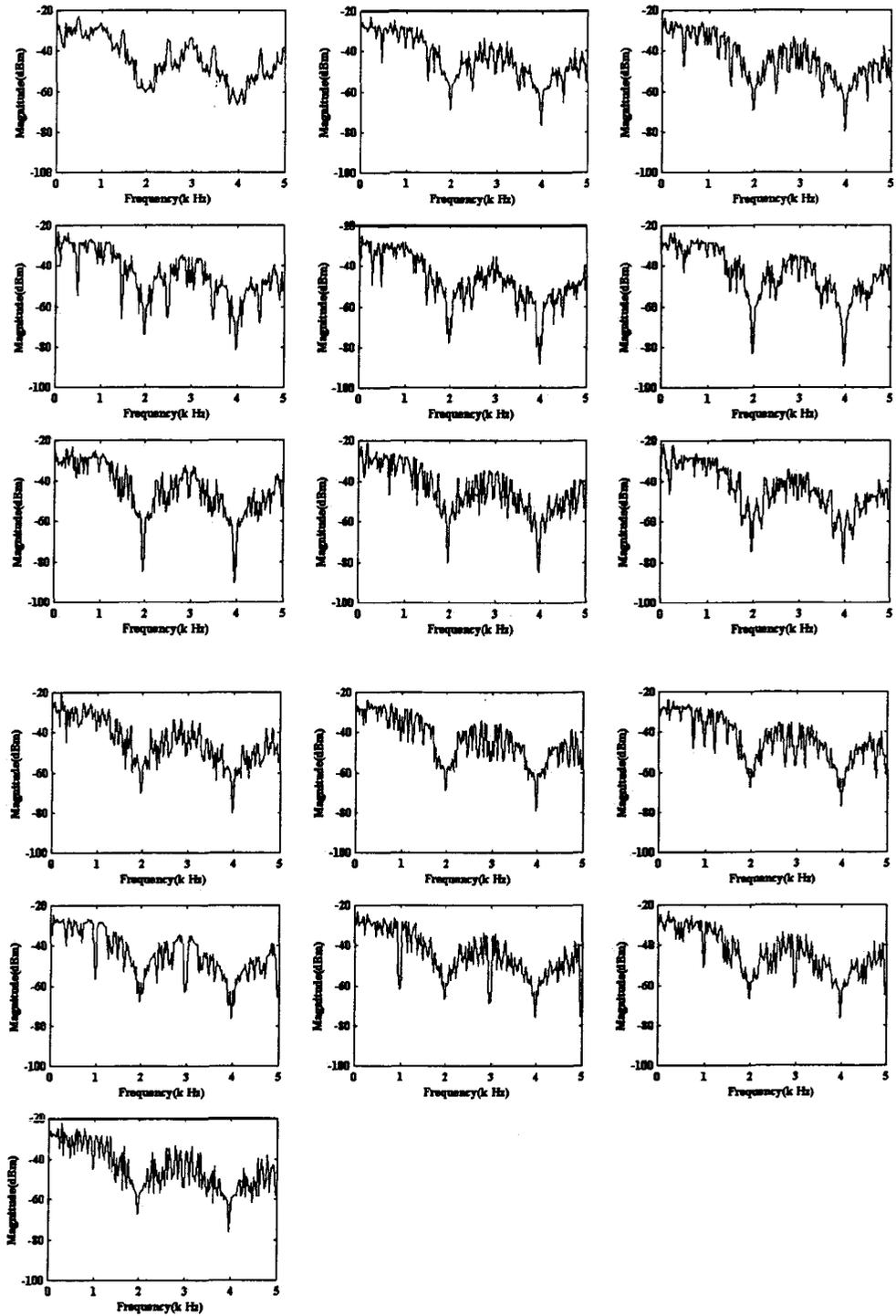
Figure 3-39 The magnitude spectrum of waveforms across the pixels while selecting 16 rows at a time when row select patterns are derived from PRBS.
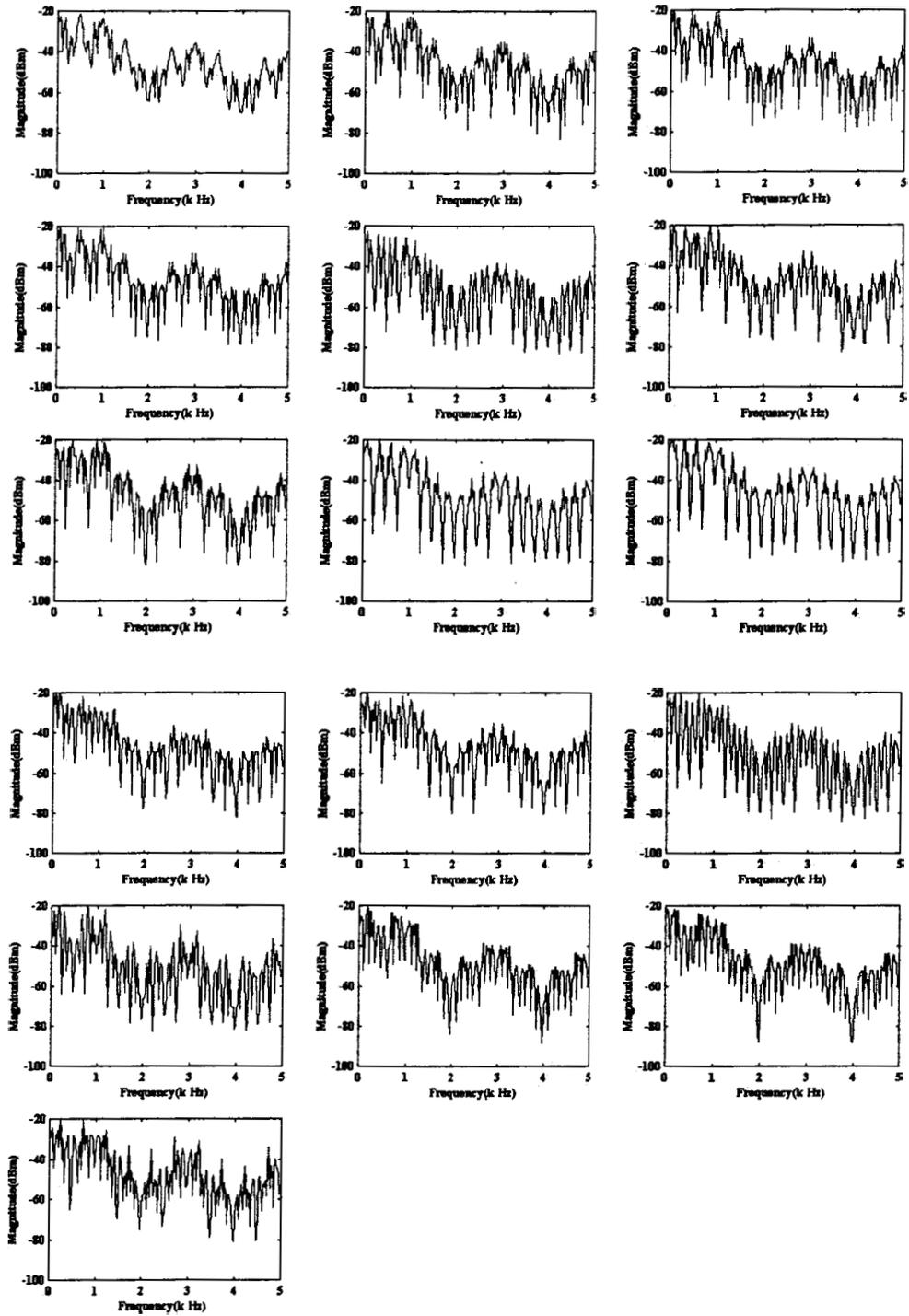
Figure 3-40 **The magnitude spectrum of waveforms across the pixels while selecting 8 rows at a time when row select patterns are derived from Walsh functions.**