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GENERALIZED ADDRESSING TECHNIQUE FOR RMS RESPONDING MATRIX LCDS

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Abstract

The paper describes a new addressing technique in which more than one address line is selected simultaneously. It requires a lower supply voltage and gives better brightness uniformity of pixels as compared to the conventional techniques.

Introduction

The analysis of scanning limitations of root-mean-square (rms) responding Liquid Crystal Displays (LCDs) by Alt and Pleshko [1] is an important milestone in the addressing of matrix LCDs. The Alt and Pleshko Technique (APT) achieves a maximum selection ratio, V_{ON}/V_{OFF} . The modified addressing waveforms proposed by Kawakami et al. [2] has the same selection ratio, but requires a lower supply voltage as compared to that of APT. This technique is widely used due to its low supply voltage requirement and will be referred to as Improved Alt and Pleshko Technique (IAPT). Both APT and IAPT are based on line-by-line selection of the address lines (rows) in a matrix LCD. The Binary Addressing Technique (BAT) and the Hybrid Addressing Technique (HAT) proposed earlier [3,4] are based on selecting more than one address line at a given instant of time. However, the selection ratio of these techniques is lower than that of APT. A generalized addressing technique proposed here has the same selection ratio as that of APT yet, requires a lower supply voltage and achieves a better brightness uniformity of pixels as compared to APT as well as IAPT.

Technique

The N rows to be multiplexed in a display are divided into (N/ℓ) non-intersecting subgroups, each consisting of ℓ address lines. The data to be displayed in the selected subgroup in any one of the columns is an ℓ -bit word represented by,

$$d_{k\ell+1}, d_{k\ell+2}, \dots, d_{k\ell+\ell}; d_{k\ell+j} = 0 \text{ or } 1 \quad (1)$$

wherein, logic 0 and logic 1 represent the OFF and ON pixels respectively. The row-select pattern is again an ℓ -bit word represented by,

$$a_{k\ell+1}, a_{k\ell+2}, \dots, a_{k\ell+\ell}; a_{k\ell+j} = 0 \text{ or } 1 \quad (2)$$

The value of k ranges from 0 to $[(N/\ell) - 1]$ corresponding to the selected subgroups.

The various steps involved in this technique are given below:

- i) One sub-group is selected at a time for addressing ;
- ii) An ℓ -bit word is chosen as the row-select pattern ;
- iii) The row-select voltages are $-V_r$ for logic 0 and $+V_r$ for logic 1, while the $(N - \ell)$ unselected rows are grounded ;

iv) The row-select and the data patterns in the selected subgroup are compared bit-by-bit using digital comparators, viz., exclusive-OR gates ;

v) The number of mismatches i between these two patterns is determined by counting the number of exclusive-OR gates with logic 1 output.

The steps (iv) and (v) can be summarized as follows:

$$i = \sum_{j=0}^{\ell} a_{k\ell+j} \oplus d_{k\ell+j} \quad (3)$$

vi) The column voltage is chosen to be V_j , if the number of mismatches is i ;

vii) The column voltage for each column in the matrix is determined independently by repeating the steps (iv) - (vi) ;

viii) Both the row and column voltages are applied simultaneously to the matrix display for a time duration T ;

ix) A new row-select pattern is chosen and the column voltages are determined using steps (iv) - (vi). The new row and column voltages are applied to the display for an equal duration of time at the end of T ;

x) A cycle is completed when all the subgroups ($= N/\ell$) are selected with all the 2^ℓ row-select patterns once ;

xi) The display is refreshed by repeating this cycle continuously.

The time duration T should be small as compared to the response time of the display, in order to ensure the rms behavior of the display. This technique is similar to HAT [4] except for the choice of the column voltages and will be referred to as Improved Hybrid Addressing Technique (IHAT). The IHAT has the following freedom in the choice of the row-select sequence and the subgroup selection as given below:-

- The sequence in which the 2^ℓ row-select patterns are applied to the subgroup can be in any order, viz., natural binary, gray code or random.
- A subgroup can be selected with 2^j row-select patterns consecutively before selecting the next subgroup. Here j can range from 0 to ℓ .
- The order in which the subgroups are selected can also be changed as long as all the subgroups are selected with all the 2^ℓ row-select patterns.

The rms voltages across similar pixels are equal in all the cases discussed above, but the frequency components are different in each case. One of these combinations can be chosen as the addressing sequence in order to achieve a good brightness uniformity of pixels in the display.

The column voltage V_i for the various values ℓ and i are given in table 1. The column voltages here are normalized to V_0 . Addressing waveforms of IHAT with $\ell = 2$ and 3 are shown in Fig.1 and 2 respectively, as typical examples. The natural dc-free operation of IHAT is evident from the waveforms across the pixels illustrated in Fig.1.

Table 1
Column voltages of IHAT for various ℓ and i

ℓ	Column voltages corresponding to the number of mismatches (i)							
	0	1	2	3	4	5	6	7
2	-1	0	+1	-	-	-	-	-
3	-1	$-\frac{1}{3}$	$+\frac{1}{3}$	+1	-	-	-	-
4	-1	$-\frac{1}{2}$	0	$+\frac{1}{2}$	+1	-	-	-
5	-1	$-\frac{2}{5}$	$-\frac{1}{5}$	$+\frac{1}{5}$	$+\frac{2}{5}$	+1	-	-
6	-1	$-\frac{4}{6}$	$-\frac{2}{6}$	0	$+\frac{2}{6}$	$+\frac{4}{6}$	+1	-
7	-1	$-\frac{5}{7}$	$-\frac{3}{7}$	$-\frac{1}{7}$	$+\frac{1}{7}$	$+\frac{3}{7}$	$+\frac{5}{7}$	+1

Analysis

Consider the row-select patterns with i mismatches. The number of ℓ -bit row-select patterns which differ from an ℓ -bit data pattern by i -bits is given by

$$C_i = \frac{\ell!}{i!(\ell-i)!} \quad (4)$$

Let the sign of the column voltage be in-phase with $-V_r$, the row-select voltage corresponding to logic 0. The magnitude of the instantaneous voltage across the pixel will be either $|V_r + V_i|$ or $|V_r - V_i|$ in the selected rows and $|V_i|$ in the unselected rows. In general the voltage across a pixel should be as low as possible for an OFF pixel and as high as possible for an ON pixel, in order to achieve a high selection ratio. Hence the voltage $|V_r + V_i|$ is favourable for an ON pixel and unfavourable for an OFF pixel. Similarly the voltage $|V_r - V_i|$ is favourable for an OFF pixel and unfavourable for an ON pixel. The number of mismatches gives the number of unfavourable voltages in the selected rows in a column. The total number of mismatches (iC_i) in C_i row-select patterns considered are equally distributed over the ℓ pixels in the selected rows. Hence the number of unfavourable voltages per pixel (B_i) when the number of mismatches is i can be obtained as given below.

$$B_i = \frac{iC_i}{\ell} = \frac{i(\ell-1)!}{i!(\ell-i)!} \quad (5)$$

The number of times a pixel gets a favourable voltage during the C_i time intervals considered is

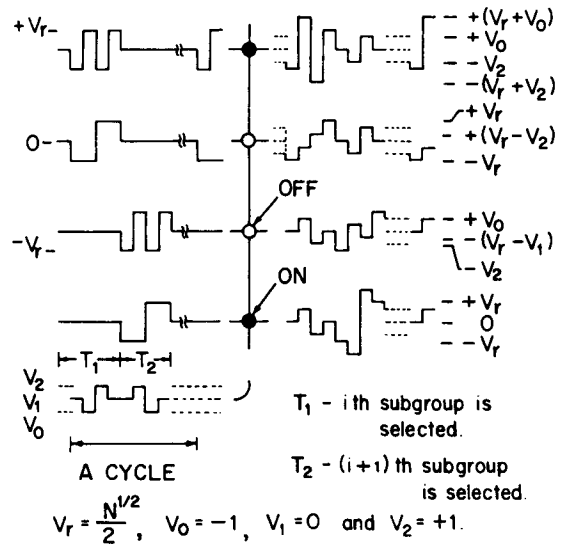


Fig.1. Typical addressing waveforms of IHAT, when $\ell=2$.

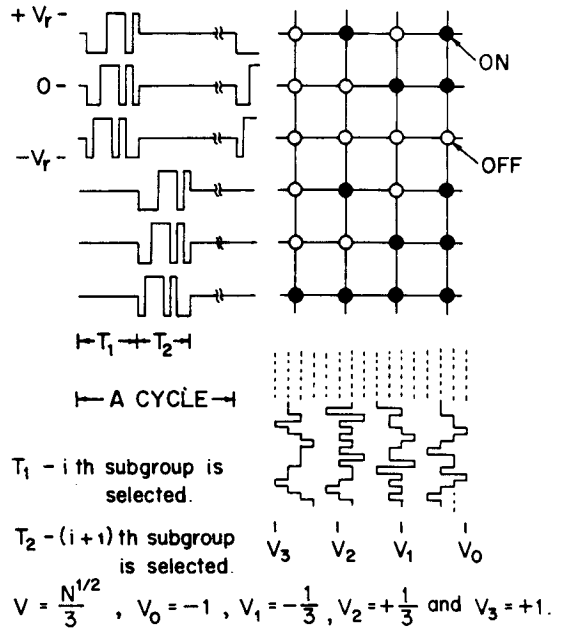


Fig.2. Typical addressing waveforms of IHAT, when $\ell=3$.

$$A_i = (C_i - B_i) = \frac{(\ell - 1)!}{i! (\ell - i - 1)!} \quad (6)$$

The expression for the rms voltages across ON and OFF pixels are arrived at using the above statistics. The summation here ranges from 0 to ℓ , since the number of mismatches can range from 0 to ℓ .

$$V_{ON} \text{ (rms)} = \left[\frac{S_1 + S_2 + S_3}{S_4} \right]^{1/2} \quad (7)$$

$$V_{OFF} \text{ (rms)} = \left[\frac{S_5 + S_6 + S_3}{S_4} \right]^{1/2} \quad (8)$$

wherein

$$S_1 = \sum_{i=0}^{\ell} A_i (V_r + V_i)^2; \quad S_2 = \sum_{i=0}^{\ell} B_i (V_r - V_i)^2;$$

$$S_3 = \left(\frac{N}{\ell} - 1\right) \sum_{i=0}^{\ell} (A_i + B_i) V_i^2; \quad S_4 = 2^{\ell} \left(\frac{N}{\ell}\right);$$

$$S_5 = \sum_{i=0}^{\ell} A_i (V_r - V_i)^2; \quad \text{and} \quad S_6 = \sum_{i=0}^{\ell} B_i (V_r + V_i)^2.$$

The ratio (V_{ON}/V_{OFF}) should be a maximum in order to achieve a good contrast in the display. The selection ratio is of the form

$$\frac{V_{ON}}{V_{OFF}} = \left[\frac{f_1 + f_2}{f_1 - f_2} \right]^{1/2} \quad (9)$$

wherein

$$f_1 = \sum_{i=0}^{\ell} (A_i + B_i) V_r^2 + \frac{N}{\ell} \sum_{i=0}^{\ell} (A_i + B_i) V_i^2;$$

$$\text{and} \quad f_2 = 2 \sum_{i=0}^{\ell} (A_i - B_i) V_r V_i$$

The selection ratio is a maximum for the following conditions

$$V_r = \frac{N^{1/2}}{\ell} V_0 \quad (10)$$

and

$$V_i = \left(\frac{\ell - 2i}{\ell}\right) V_0 \quad (11)$$

wherein V_0 is the column voltage corresponding to zero mismatches. Table 1 gives the amplitudes of the column voltages (V_i) normalized to V_0 for various values of ℓ .

The maximum selection ratio is obtained by substituting these values in eqn.(9) and is given by

$$R = \frac{V_{ON}}{V_{OFF}} = \left[\frac{N^{1/2} + 1}{N^{1/2} - 1} \right]^{1/2} \quad (12)$$

The selection ratio here is the same as that of APT and IAPT. This is the maximum value possible for any addressing technique as shown by Kmetz and Nehring [5]. The rms voltages across ON and OFF pixels when the selection ratio is a maximum are as follows

$$V_{ON} \text{ (rms)} = \left[\frac{2(N + N^{1/2})}{N\ell} \right]^{1/2} V_0 \quad (13)$$

$$V_{OFF} \text{ (rms)} = \left[\frac{2(N - N^{1/2})}{N\ell} \right]^{1/2} V_0 \quad (14)$$

The supply voltage requirement (V_s) is determined by the maximum swing in the addressing waveforms. The amplitudes of the row-select voltage (V_r) is lower than V_0 for $N < \ell^2$, the same as V_0 for $N = \ell^2$ and greater than V_0 for $N > \ell^2$. Amplitudes of the column voltages for $i > 0$ are however lower than or equal to V_0 . The supply voltage requirement of IHAT for the two ranges are as follows

$$V_s \text{ (IHAT)} = 2V_0 = \left[\frac{4\ell}{2(1 - N^{-1/2})} \right]^{1/2} V_{th} \text{ for } N \leq \ell^2 \quad \dots(15)$$

and

$$V_s \text{ (IHAT)} = 2V_r = \left[\frac{4(N/\ell)}{2(1 - N^{-1/2})} \right]^{1/2} V_{th} \text{ for } N \geq \ell^2 \quad \dots(16)$$

The supply voltage of APT is reproduced here for comparison

$$V_s \text{ (APT)} = \left[\frac{4N}{2(1 - N^{-1/2})} \right]^{1/2} V_{th} \quad (17)$$

The supply voltage requirement of IHAT is compared with that of APT using the ratio given below

$$\frac{V_s \text{ (IHAT)}}{V_s \text{ (APT)}} = \begin{cases} (\ell/N)^{1/2} & \text{for } N \leq \ell^2 \\ (1/\ell)^{1/2} & \text{for } N \geq \ell^2 \end{cases} \quad (18)$$

This ratio is independent of N when $N \geq \ell^2$. The supply voltage requirement of IAPT is also reproduced below for a comparison

$$V_s \text{ (IAPT)} = \frac{(N^{1/2} + 1)}{[2(1 - N^{-1/2})]^{1/2}} \quad (19)$$

The supply voltage requirement of IHAT is compared with that of IAPT using the following ratio

$$\frac{V_s(\text{IHAT})}{V_s(\text{IAPT})} = \begin{cases} \frac{2\ell^{1/2}}{(N^{1/2} + 1)} & \text{for } N \leq \ell^2 \\ \frac{2(N/\ell)^{1/2}}{(N^{1/2} + 1)} & \text{for } N \geq \ell^2 \end{cases} \quad (20)$$

The supply voltage requirement of IHAT is compared with that of IAPT and APT for various values of ℓ in Figs.3 and 4. The supply voltage requirement of IHAT is a minimum for $N = \ell^2$ and is lower than that of IAPT for a wide range of N when ℓ is greater than 3. The Table 2 gives the possible values of ℓ for different values of N , leading to a good reduction in the supply voltage requirement. From this table it is evident that $\ell = 7$ is quite adequate for a good reduction in the supply voltage even when N is a few thousand address lines.

Table 2

Possible values of ℓ , for different N leading to a good reduction in the supply voltage requirement

N	ℓ	$\frac{V_s(\text{IHAT})}{V_s(\text{IAPT})} \times 100\%$ V_{th} constant	n_c	No. of time intervals in a cycle (IHAT)/IAPT
4	2	94.28	3	1
9	3	86.60	5	4/3
12	3,4	89.60	7,8	4/3,8/4
16	4	80.00	5	8/4
20	4,5	81.73	8,9	8/4,16/5
25	5	74.54	7	16/5
30	5,6	75.63	9,10	16/5,32/6
36	6	69.99	7	32/6
42	6,7	70.74	10,11	32/6,64/7
49	7	66.14	9	64/7
70	7	67.52	11	64/7
140	7	69.70	11	64/7
280	7	71.33	11	64/7
560	7	72.59	11	64/7
1120	7	73.40	11	64/7
2240	7	74.03	11	64/7
4480	7	74.48	11	64/7

Discussion

IHAT requires N to be an integral multiple of ℓ . This condition is imposed only to reduce the number of time intervals to complete a cycle. Displays which do not meet this condition can also be addressed with IHAT by adopting any one of the following approaches:

- Additional dummy rows (not connected to the display) can be introduced to satisfy the addressing requirement, or
- Subgroups can be overlapped; after selecting ℓ -rows a new subgroup can be formed by dropping one row and adding a new row to the subgroup. Here the number of time intervals to complete a cycle increases by a factor ℓ as compared to the case with non-intersecting subgroups.

The IHAT is well suited for addressing matrix displays based on both twisted nematic and super-twisted birefringence effects (SBE) for the following reasons:

- A considerable reduction in the supply voltage requirement, especially for large values of N (Applications like displays in lap-top computers).
- Good brightness uniformity of pixels.
- Natural dc-free operation.
- Higher duty cycle as compared to APT and IAPT.

However the above advantages are obtained at the cost of the following factors:

- The hardware complexity of the drivers depends on ℓ . The number of voltage levels in the column waveforms is $(\ell + 1)$ as compared to 4 in the case of IAPT.
- Increase in the number of time intervals to complete a cycle by a factor $(2^{(\ell-1)}/\ell)$ as compared to IAPT.

The hardware complexity of IHAT increases with ℓ , since $(\ell + 1)$ analog switches are required in each column driver to generate the column waveforms with $(\ell + 1)$ voltage levels. The number of voltage levels in the column waveform (n_c) can be restricted by grouping the number of mismatches (i) and assigning a column voltage for each group. This reduction in hardware leads to a lower selection ratio as in HAT. Wherein n_c is just 2. [4]

The special cases of IHAT with the value of n_c restricted to 3 when ℓ is even and 4 when ℓ is odd are referred to as IHAT-S3 and IHAT-S4 respectively [6]. The selection ratio of these techniques can be compared with that of APT using N_{eq} , which gives the number of lines to be multiplexed with APT to get the same selection ratio as the technique being compared [7].

The N_{eq} of these techniques are given below:

- (256 $N/175$) for HAT with $\ell = 7$
- (88 $N/75$) for IHAT-S3 with $\ell = 6$
- (232 $N/215$) for IHAT-S4 with $\ell = 7$

A trade-off between hardware complexity, supply voltage requirement and selection ratio is possible in the case of SBE-Displays with steep electro-optic characteristics.

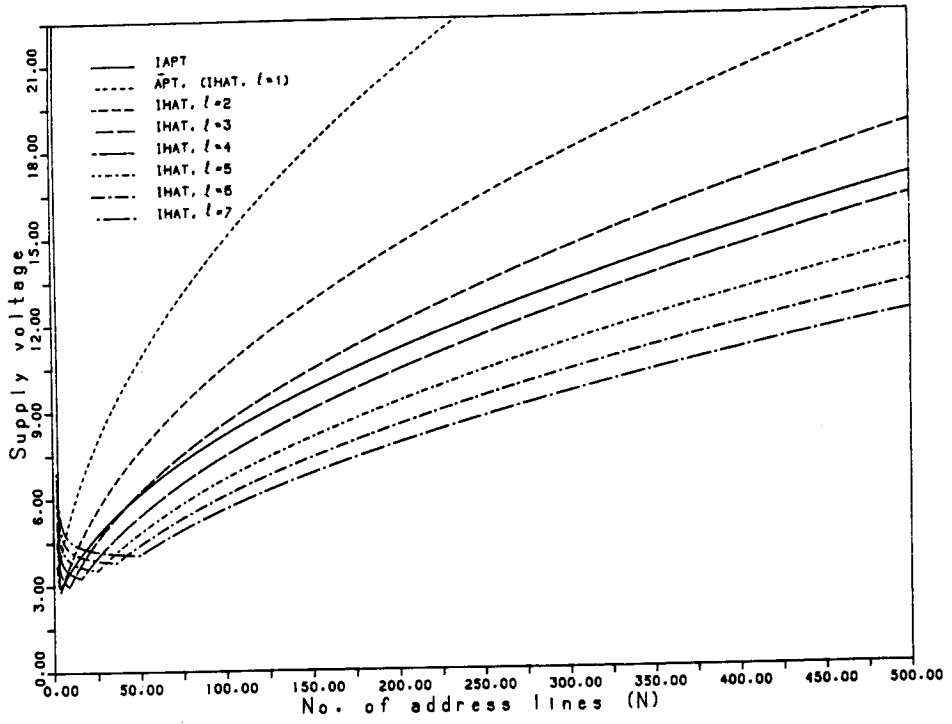


Fig. 3. Supply voltage (normalized to V_{th}) vs. N for both IHAT and IAPT.

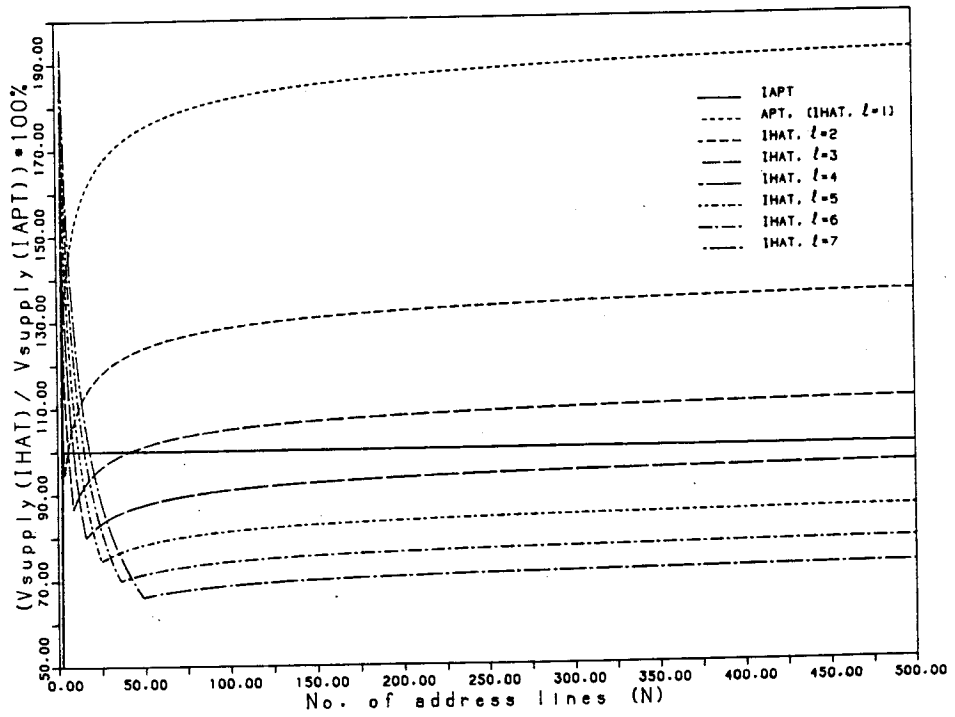


Fig. 4. A comparison of supply voltage requirement of IHAT with that of IAPT.

Results

The photographs of a 64 x 64 matrix TNLCD addressed with IHAT ($N=63$ and $\ell=7$) are shown in Fig.5. The brightness uniformity of pixels in this display is found to be good. The voltages across the ON and OFF pixels were measured using HP 3467 A, a logging multimeter capable of measuring true-rms voltages. The measured value of selection ratio agrees with the theoretical value within $\pm 1\%$. The supply voltage requirement here is only 67.13% of that required in the case of IAPT.

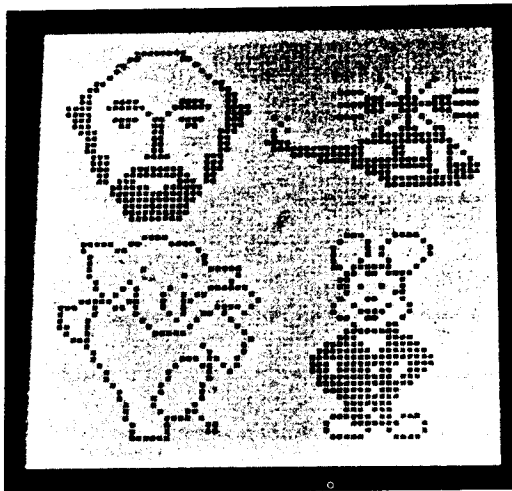
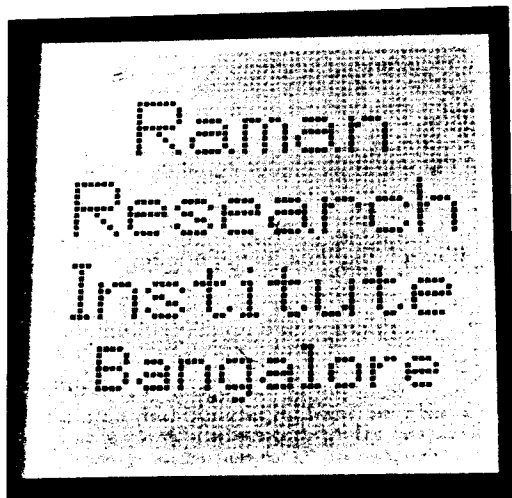


Fig.5. Photographs of a display addressed with IHAT.

Conclusion

The IHAT proposed here is a generalised form of APT, wherein the number of selected rows at a given instant of time is a variable ℓ as compared to one in the case of APT. Several new addressing techniques can also be treated as special cases of IHAT as given below:

- BAT [3,6]; when $\ell = N$ and $n_c = 2$
- HAT [4,6]; when ℓ is odd and $n_c = 2$
- IHAT-S3 [6]; when ℓ is even and $n_c = 3$
- IHAT-S4 [6]; when ℓ is odd and $n_c = 4$

Good reduction in the supply voltage requirement (especially when N is large) and good brightness uniformity of pixels can be achieved by using IHAT for matrix displays with rms response.

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